HARRIS

PRELIMINARY

HC-5552/53
HC-5554/57

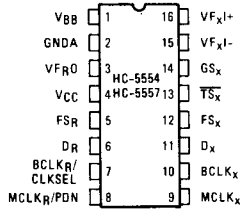
Monolithic CMOS Serial Interface COFIDEC Family

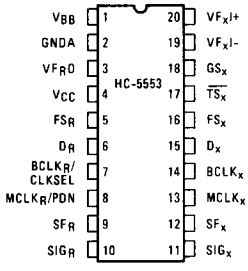
Features

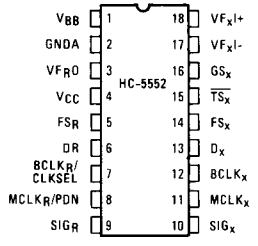
- Complete CODEC/FILTER (COFIDEC) Family
- HC-5552 - μ-Law with Short Frame Signaling (18 Pin)
- HC-5553 - μ-Law with Both Short and Long Frame Signaling (20 Pin)
- HC-5554 - μ-Law without Signaling (16 Pin)
- HC-5557 - μ-Law (16 Pin)
- Low Operation Power (60mW Typical)
- Low Standby Power (1mW Typical)
- $\pm$5V Power Supplies
- Meets or Exceed all D3/D4 and CCITT Specifications
- TTL or CMOS Compatible Digital Interfaces
- PCM Data Serial Input/Output
- Synchronous or Asynchronous Operation
- Automatic Power-Down

Pinouts

TOP VIEW







DUAL-IN-LINE PACKAGE

Description

The CODEC/FILTER (COFIDEC) family includes A-Law and μ-Law monolithic CODEC/FILTERS implemented with double-poly CMOS technology.

The transmit side of the device consists of:

- an amplifier with external gain adjustment
- an RC active prefilter to eliminate high frequency noise
- a switched capacitor band-pass filter including a notch filter at 55Hz to reject signals below 200Hz and above 3400Hz
- a change redistribution coder which samples and encodes filtered signal in the companded μ-Law or A-Law PCM format
- a precision voltage reference
- an internal auto-zero network to cancel the transmit offset

The receive side of the device consists of:

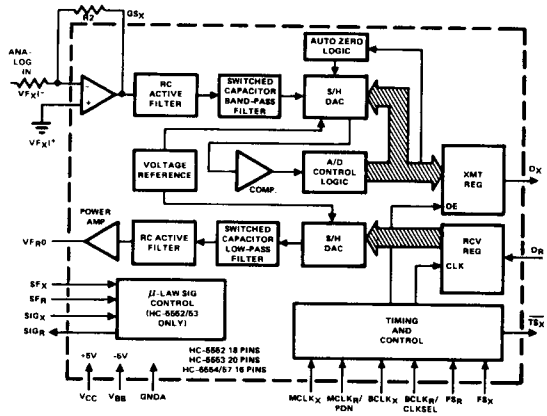
- an expanding decoder (A-Law or μ-Law) to reconstruct the analog signal
- a switched-capacitor low-pass filter which corrects for the sinx/x response of the decoder output and rejects signals above 3400Hz
- an RC active filter followed by a single ended power amplifier able to drive a 600X load
- a precision voltage reference

The PCM word is transmitted/received in a serial format compatible with industry standard.

The device is operated with two (transmit and receive) master clocks (1.536MHz, 1.544MHz or 2.048MHz) which may be asynchronous.

Also required are transmit and receive bit clock which may vary from 64KHz to 2.048MHz and transmit and receive frame sync pulses.

Functional Diagram



Pin Description

HC-5552 PIN #	HC-5553 PIN #	HC-5554 HC-5557 PIN #	NAME	FUNCTION
1	1	1	V_{BB}	Negative Power Supply V_{BB} = -5V ±5%.
2	2	2	GNPA	Ground Analog Ground. All signals are referenced to this pin.
3	3	3	VF_RO	Analog Output of the Receiver Filter.
4	4	4	V_{CC}	Positive Power Supply V_{CC} = +5V ±5.
5	5	5	FS_R	Receive Frame Sync Pulse. An 8KHz pulse train which enables the PCM word to be shifted into the receiver register.
6	6	6	D_R	Receive Data Input. The receiver register clocks in D_R input with bit clock falling edge following an FS_R rising edge.
7	7	7	$BCLK_R$ & CLKSEL	Bit Clock which shifts D_R data into the receiver register. May vary from 64KHz to 2.048MHz. Alternately may be a clock selection in synchronous mode. See Table 1 in Functional Description for synchronous operation.
8	8	8	$MCLK_R$ & PDN	Receive Master Clock must be 1.536, 1.544 or 2.084MHz. May be asynchronous with $MCLK_X$ and $BCLK_R$. If $MCLK_R$ is low, the COFIDEC operates in synchronous mode. If $MCLK_R$ is tied high, the COFIDEC is powered down.
	9		SF_R	When high during FS_R, SF_R indicates a receive signaling frame in long frame mode.
9	10		SIG_R	The signaling bit appears at this output after each receive signaling frame.
10	11		SIG_X	Signaling Data Input. This input is inserted in place of LSB or PCM word during signaling frame.
	12		SF_X	When high during FS_X, SF_X indicates a transmit signaling frame in long frame mode.
11	13	9	$MCLK_X$	Transmit Master Clock. Must be 1.536, 1.544 or 2.048MHz. May be asynchronous with $MCLK_R$. See table 1 in Functional Description for synchronous operation.
12	14	10	$BCLK_X$	Bit Clock. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
13	15	11	D_X	Three-State PCM data output enabled by FS_X.
14	16	12	FS_X	Transmit Frame Sync Pulse. An 8KHz pulse train which enables the PCM word to be shifted out through D_X with $BCLK_X$.
15	17	13	$\overline{TS_X}$	Open drain output. Pulled down durning time slot.
16	18	14	GS_X	Analog output of transmit amplifier. Used to set the gain.
17	19	15	VF_XI-	Inverting input of transmit amplifier.
18	20	16	VF_XI+	Non inverting input of transmit amplifier.

Power Up/Power Down

The COFIDEC is automatically placed into the power-down mode when V_{CC} and V_{BB} are applied to the circuit. All the analog blocks are de-activated and the D_X and VF_RO outputs are in their high impedance state.

When a low level or a clock is applied on $MCLK_R$, the COFIDEC powers up.

During the first two frames, the D_X output is in the high impedance state. To compensate rapidly for the offset of the transmit section, the auto-zero circuit is in quick capture mode during the first 512 frames and the input of the low pass filter is set to zero during the first 256 frames.

When a high level is applied on $MCLK_R$, the device goes into power down mode.

Transmit Section

The input of the transmit section is an operational amplifier whose gain can be externally adjusted. This amplifier exhibits low noise, wide bandwidth and low offset voltage (1mV typical). The input amplifier drives an anti-aliasing RC active filter. The switched capacitor band-pass filter is split into a 5th order elliptic low-pass filter and a 3rd order elliptic high-pass filter which includes a 55Hz notch filter to guarantee excellent line (50 or 60Hz) rejection. The structure of each filter is fully differential so that their performance is not affected by parasitic elements.

The A/D converter is of a companding type according to A (HC-5557) or μ (HC-5552/53/54) coding laws.

Receive Section

The receive section includes an expanding D/A converter according to A (HC-5557) or μ (HC-552/53/54) coding laws. The decoder is followed by a 5th order switched capacitor low-pass filter and an RC active filter.

As for the transmit part, the filters are fully differential. The output amplifier has a unity gain and can drive a 600Ω/500pF load.

Seperately trimmed voltage references are provided for transmit and receive sections respectively. Clocking circuits and internal power supplies are also fully independent. This arrangement greatly reduces crosstalk between the transmit and receive blocks and improves performance.

Synchronous Operation

A low level on $MCLK_R$ input presets the circuit into synchronous mode. In this case, $MCLK_X$ and $BCLK_X$ are used for both transmit and receive sections, and $BCLK_R$ is used as a master clock select. A high level or open circuit selects the normal frequency and a low level selects the alternate frequency (See Table 1 below).

TABLE 1.

BCLKR/CLKSEL	HC-5557	HC-5552/53/54
Clock	2.048MHz	1.544/1.536MHz
Low	1.536/1.544MHz	2.048MHz
High or Open	2.048MHz	1.536/1.544MHz

The bit clock $BCLK_X$ may vary from 64KHz to 2.048MHz provided that $BCLK_X$ is synchronous with $MCLK_X$. For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse of each frame.

Asynchronous Operation

Two asynchronous modes are allowed with excellent transmission performance:

1º/ $MCLK_R$ is fully independent of $MCLK_X$ and must be 2.048MHz for HC-5557 (A law) and 1.544 or 1.536MHz for HC-5552/53/54 (μ law) (freq $MCLK_X$ = freq $MCLK_R$ ± 50ppm).

2º/ If required, $MCLK_X$ can also be used as a master clock for both transmit and receive sections ($MCLK_X$ input connected externally to $MCLK_R$ input).

In both modes, $BCLK_X$ and $BCLK_R$ may operate from 64KHz to 2.048MHz. $BCLK_X$ must be synchronous with $MCLK_X$, but $BCLK_R$ may be asynchronous with $MCLK_R$ (freq $BCLK_R$ = freq $MCLK_R$ ± 50ppm).

The degradation of the signal to total distortion ration under all permitted asynchronous conditions does not exceed 0.5dB as compared to the same measurement made with fully synchronous clocks.

Data Acquisition and Transmission

In both short and long frame operation, when FS_X is high, the first $BCLK_X$ rising edge enables the D_X buffer and shifts the sign bit out. The other bits are shifted out with the 7 following rising edges of $BCLK_X$. The falling edge of the 8th $BCLK_X$ pulse disables the D_X buffer.

Similarly, when FS_R is high, the first $BCLK_R$ rising edge enables the PCM word to be latched in from D_R input with the 8 following falling edges of $BCLK_R$.

Detection of Short or Long Frame Operation

A long frame of short frame operation is detected by sensing FS_X on the 3rd rising edge of $BCLK_X$ after FS_X low to high transition. At this time, if a high level is sensed on FS_X, a long frame operation is detected.

Upon power up a short frame operation is assumed.

Signaling

In transmission, the signaling bit provided by SIG_X input is latched by the 8th $BCLK_X$ rising edge after FS_X low to high transition and inseted in place of the LSB of the PCM word during the frame.

In reception, the signaling bit is extracted from the PCM word (LSB) in the receive register and transferred to SIG_R output. The data at SIG_R output will be held until next signaling frame. At the same time the decoder compensates for the loss of the LSB by setting the LSB to 1/2 to minimize noise and distortion.

* In SHORT frame, the COFIDEC senses a signaling frame when FS_X (FS_R) is still high during the 1st falling edge of $BCLK_X$ ($BCLK_R$) after FS_X (FS_R) low to high transition.
* In LONG frame, the frame sync pulses FS_X and FS_R are 3 or more bit clock periods long. A signaling frame is identified from SF_X and SF_R for transmit and receive sections respectively. SF_X (SF_R) must be high for 3 or more $BCLK_X$ ($BCLK_R$) periods for a signaling frame and stay low for a non signaling frame.

NOTE: Transmit and Receive Sections must be both in LONG frame or both in SHORT frame.

HC-5553 can be used for both short and long frame signaling. For short frame use, SF_X and SF_R should be tied low or left open circuit.

HC-5552 is intended for short frame application only. Signaling is not possible with HC-5554 or HC-5557.

Absolute Maximum Ratings

V_{CC} to GND .....-0.3V to +7V
V_{BB} to GND .....+0.3V to -7V
Voltage at any Digital
Input or Output .....V_{CC} +0.3V to GND -0.3V
Voltage at any Analog
Input or Output .....V_{CC} +0.3V to V_{BB} -0.3V

Operating Temperature Range.....-25°C to +80°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (Soldering 10 seconds) .....+300°C

Electrical Characteristics

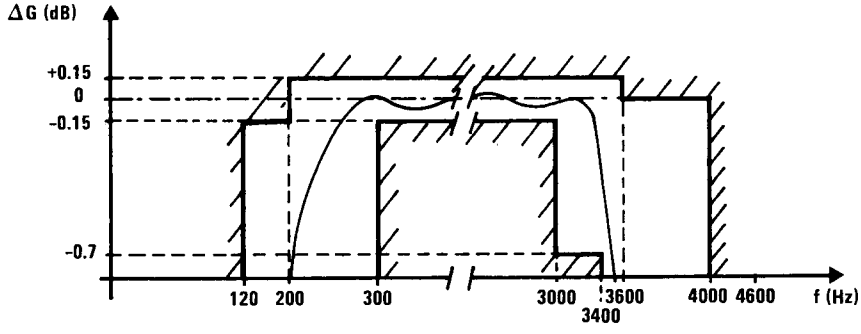
Unless otherwise specified: V_{CC} = 5.0V ± 5%, V_{BB} -5V ± 5%, GND = 0V T_A = +0°C to +70°C: typical characteristics specified at V_{CC} = 5.0V, V_{BB} = 5.0V, T_A = +25°C; all signals are referenced to GND.

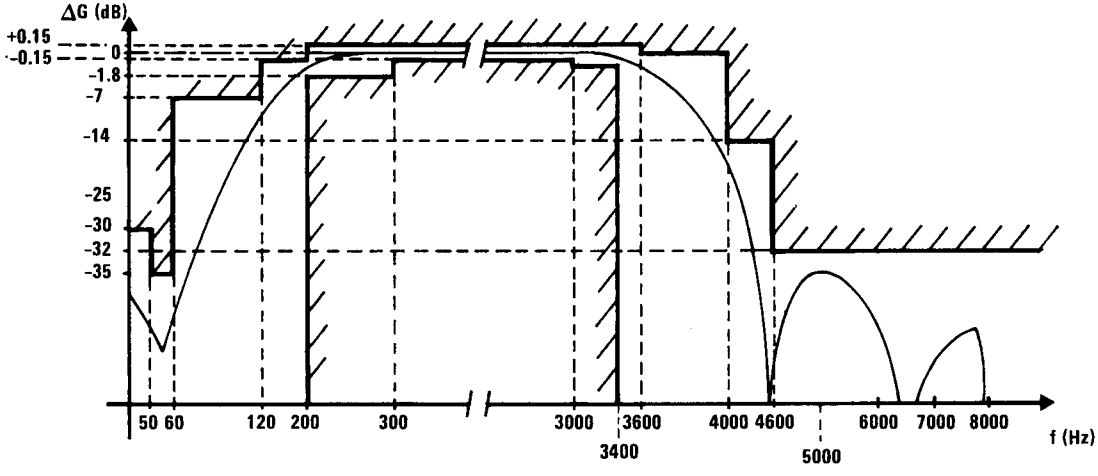
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Interface						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L = 5.0mA SIG_R, I_L = 1.0mA $\overline{TS}_X$, I_L = 3.2mA, Open Drain			0.4 0.4 0.4	V V V
V_{OH}	Output High Voltage	D_X, I_L = -5.0mA SIG_R, I_L = -1.0mA	2.4 2.4			V V
I_{IL}	Input Low Current (Note 1)	GND≤V_{IN}≤V_{IL}, All Digital Inputs	-10		10	µA
I_{IH}	Input High Current (Note 1)	$V_{IH} \leq V_{IN} \leq V_{CC}$	-10		10	µA
I_{OZ}	Output Current in High Impedance State	D_X, GND ≤ V_O ≤ V_{CC}	-10		10	µA
Analog Interface with Transmit Input Amplifier (All Devices)						
I_IXA	Input Leakage Current	-2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	-200		200	nA
R_IXA	Input Resistance	-2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Level	GS_XR_L = 10kΩ	±2.8	±4.2		V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		-20	1	20	mV
$V_{CM}XA$	Common-Mode Voltage		-2.5		+2.5	V
CMRRXA	Common-Mode Rejection Ratio		60	80		dB
PSRRXA	Power Supply Rejection Ratio		60	70		dB
Analog Interface with Receive Filter (All Devices)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		-100		100	mV
Power Dissipation (All Devices)						
I_{CCO}	Power-Down Current			0.15	.5	mA
I_{BBO}	Power-Down Current			0.05	0.3	mA
I_{CC1}	Active Current			6	9	mA
I_{BB1}	Active Current			6	9	mA

NOTE: 1). SFX, SFR: Internal pull down (2 µ A typical)
BCLR: Internal pull up (2 µ A typical)

Transmission Characteristics (Continued) Unless otherwise specified: T_A = +0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GND = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmit Section Transfer Characteristics						
G_{XR}	Transmit Gain Relative to Gain at 820Hz (0dBm0)	f = 50Hz — 60Hz			-35	dB
		f = 60Hz — 120Hz			-7	dB
		f = 120Hz — 200Hz			-0.15	dB
		f = 200Hz — 300Hz	-1.8		+0.15	dB
		f = 300Hz — 3000Hz	-0.15		+0.15	dB
		f = 3000Hz — 3400Hz	-0.7		+0.15	dB
		f = 3400Hz — 3600Hz			+0.15	dB
		f = 3600Hz — 4000Hz			0	dB
		f = 4000Hz — 4600Hz			-14	dB
		f = 4600Hz and Up			-32	dB



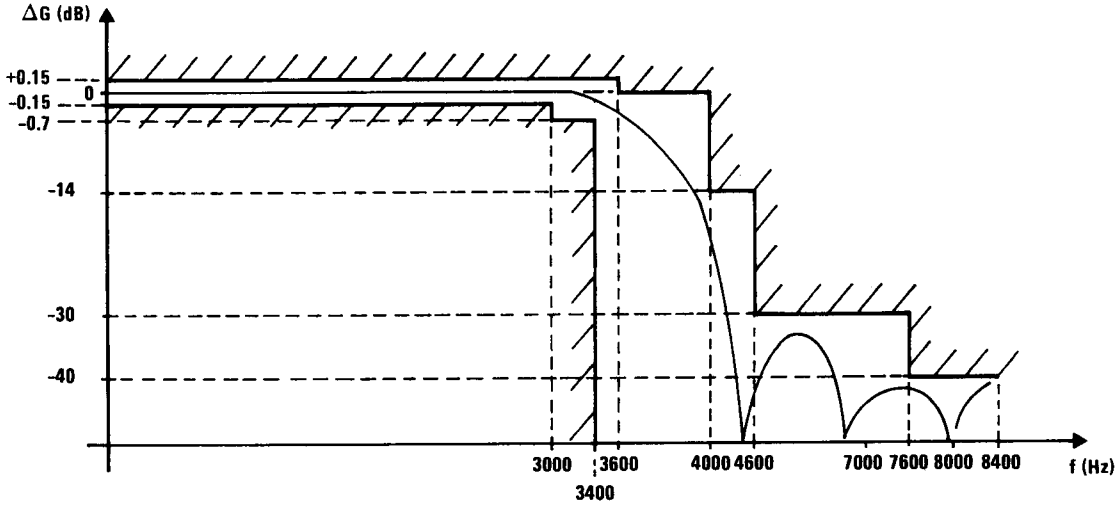


Transmission Characteristics (Continued) Unless otherwise specified: T_A = +0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GND = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Amplitude Response						
	Absolute Levels	Nominal 0dB0 levels is 4dBm (600Ω) 0dBm0 (All devices)		1.2277		Vrms
	Maximum Overload Levels	HC-5552, HC-5553, HC-5554 (3.17dBm0) HC-5557 (3.14dBm0)		2.501 2.492		V_{DC} V_{DC}
G_{XA}	Transmit Gain, Absolute	T_A = +25°C, V_{CC} = 5V, V_{BB} = -5V Input at GS_X = 0dBm0 at 1020Hz	0.15		0.15	dB
G_{XATV}	Absolute Transmit Gain Variation with Temperature and Supply Voltage	T_A = +0°C to +70°C V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%			±0.15	dB
G_{XRL}	Transmit Gain Variations with level	Sinusoidal Test Method Reference Level = -10dBm0 VF_XI+ = -40dBm0 to +3dBm0 VF_XI+ = -50dBm0 to -40dBm0 VF_XI+ = -55dBm0 to -50dBm0	 0.2 -0.4 -1.2		 0.2 0.4 1.2	 dB dB dB
GRA	Receive Gain, Absolute	T_A = +25°C, V_{CC} = 5V, V_{BB} = -5V Input = Digital Code Sequence for 0dBm0 Signal at 1020Hz	-0.15		0.15	dB
G_{RATV}	Absolute Receive Gain Variation with Temperature and Supply Voltage	T_A = +0°C to +70°C V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%			±0.15	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method Reference Input PCM Code Corresponds to an Ideally Encoded = 10dBm0 Signal PCM Level Level = -40dBm0 to +3dBm0 PCM Level = -50dBm0 to -40dBm0 PCM Level = -55dBm0 to -50dBm0	 0.2 -0.4 -1.2		 +0.2 +0.4 +1.2	 dB dB dB
V_{RO}	Receive Ouput Drive Level	R_L = 600Ω	-2.5		2.5	V
Envelope Delay Distortion with Frequency						
D_{XA}	Transmit Delay, Absolute	f = 1600Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500Hz — 600Hz f = 600Hz — 800Hz f = 800Hz — 1000Hz f = 1000Hz — 1600Hz f = 1600Hz — 2600Hz f = 2600Hz — 2800Hz f = 2800Hz — 3000Hz		140 100 50 20 60 80 140	220 145 75 50 100 110 200	μs μs μs μs μs μs μs
D_{RA}	Receive Delay, Absolute	f = 750Hz		160	180	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500Hz — 1600Hz f = 1600Hz — 260Hz f = 2600Hz — 2800Hz f = 2800Hz — 3000Hz		40 90 120 140	60 120 140 175	μs μs μs μs

Transmission Characteristics (Continued) Unless otherwise specified: T_A = +0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GND = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Receive Section Transfer Characteristics						
G_{RR}	Receive Gain Relative to Gain at 820Hz (0dBm0)	f = 0Hz — 3000Hz f = 3000Hz — 3400Hz f = 3400Hz — 3600Hz f = 3600Hz — 4000Hz f = 4000Hz — 4600Hz	-0.15 -0.7		+0.15 +0.15 +0.15 0 -14	dB dB dB dB dB
SOS	Spurious Out-of-Band Signals at the channel output	Image Signals at VF_RO: f = 4600Hz — 7600Hz f = 7600Hz — 8400Hz			 -30 -40	 dB dB



Transmission Characteristics (Continued) Unless otherwise specified: T_A = +0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GND = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Noise						
N_{XC}	Transmit Idle Channel Noise, C Message Weighted	HC-5552, HC-5553, HC-5554 VF_XI^+ = 0V		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	HC-5557 (Note 1) VF_XI^+ = 0V (Note 2)		-74 -70	-69 -67	dBm0p dBm0p
N_{RC}	Receive Idle Channel Noise, C Message Weighted	HC-5552, HC-5553, HC-5554 PCM Code equals alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Idle Channel Noise, P Message Weighted	HC-5557 PCM Code equals Positive Zero		-82	-79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0KHz to 100KHz, Loop Around Measurment, VF_XI^+ = 0Vrms			-53	dBm0
Power Supply Rejection						
$PPSR_X$	Positive Power Supply Rejection Transmit	VF_XI^+ = 0Vrms V_{CC} = 5.0V_{DC} + 100mVrms f = 0 — 50KHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection Transmit	VF_XI^+ = 0Vrms V_{BB} = -5.0V_{DC} + 100mVrms f = 0 — 50KHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection Receive	PCM Code equals Positive Zero V_{CC} = 5.0V_{DC} + 100mVrms f = 0 — 4000Hz f = 0 — 50KHz	40 25			dBC dB
$NPSR_R$	Negative Power Supply Rejection Receive	PCM Code equals Positive Zero V_{BB} = -5.0V_{DC} + 100mVrms f = 0 — 4000Hz f = 0 — 50KHz	40 25			dBC dB
Distortion						
$STD_{X/R}$	Signal to Total Distortion Transmit or Receive Channel	Sinusoidal Test Method Level = 3.0dBm0 = 0dBm0 to -30dBM0 = -40dBm0 XMT RCV = -55dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
SFD_X	Single Frequency Distortion Transmit				-46	dB
SFD_R	Single Frequency Distortion Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = -4dBm0 to -21dBm0, two frequencies in the range 300Hz to 3400Hz			-41	dB
Crosstalk						
CT_{X-R}	Transmit to Receive Crosstalk 0dBm0 Transmit Level	f = 300Hz — 3400Hz D_R = Steady PCM Code		-90	-75	dB
CT_{R-X}	Receive to Transmit Crosstalk 0dBm0 Receive Level	f = 300Hz — 3400Hz VF_XI^+ = 0V		-90	-70	dB

NOTE: 1). Quantization Noise, measured by extrapolation from the distortion result.

2). Idle Channel Noise, due to alternating sign bit of a perfectly zeroed encoder.

Timing Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clocks						
1/TPM	Frequency of Master Clock	Depends on the Device used and the $BCLK_R$/CLKSEL pin Selection		1.536 1.544 2.048		MHz MHz MHz
TWMH	Width of Master Clock High	VIH = 2.2V	160			ns
TWML	Width of Master Clock Low	VIL = 0.6V	160			ns
TRM	Rise Time of Master Clock				50	ns
TFM	Fall Time of Master Clock				50	ns
TPB	Period of Bit Clock		488		15625	ns
TWBH	Width of Bit Clock High	VIH = 2.2V	160			ns
TWBL	Width of Bit Clock Low	VIL = 0.6V	160			ns
TRB	Rise Time of Bit Clock	TPB = 488ns			50	ns
TFB	Fall Time Bit Clock	TPB = 488ns			50	ns
Frame Sync Pulses						
TSFB	Frame Sunc High Set up before 1st Bit Clock rising		50			ns
THOLD	Frame Sunc Low Hold after Bit Clock rising		50			ns
TWFH	Width of Frame Sync High		100			ns
TSFBS	Frame Sync Low Set up before 1st Bit Clock falling	Short Frame without Signaling	100			ns
THFBS	Frame Sync High Hold after 1st Bit Clock falling	Short Frame with Signaling	100			ns
TSFBL	Frame Sync Low Set up before 3rd Bit Clock rising	Short Frame with Signaling	100			ns
THFBL	Frame Sync High Hold after 3rd Bit Clock rising	Long Frame	100			ns
TWFL	Width of Frame Sync Low	Long Frame and 64KBit/s	100			ns
TSSFB	$SF_{X/R}$ Set up before 1st Bit Clock rising	Long Frame Signaling	0			ns
THSFB	$SF_{X/R}$ Hold after 3rd Bit Clock rising	Long Frame Signaling	100			ns
Data						
TDBXE	Delay from 1st Bit Clock rising to $\overline{TSX}$ Low	Load = 150pF + 2 LSTTL loads	20		140	ns
TDBXZ	Delay from 8th Bit Clock falling to $\overline{TS_X}$ disabled		50		165	ns
TDBDE	Delay from 1st Bit Clock rising to Data output enabled	Load = 150pF + 2 LSTTL loads	20		165	ns
TDBD	Delay from Bit Clock rising to Data output valid	Load = 150pF + 2 LSTTL loads			180	ns
TDBDZ	Delay from 8th Bit Clock falling to Data output disabled		50		165	ns
TSSGB	SIG_X, Set up before 8th Bit Clock rising		50			ns
THSGB	SIG_X, Hold after 8th Bit Clock rising		100			ns
TSDB	Data input Set up before Bit Clock falling		50			ns
THDB	Data input Hold after Bit Clock falling		50			ns
TDBSG	Delay from 8th Bit Clock falling to SIG_R valid	Load = 50pF + 2 LSTTL loads	300			ns

Applications Information

Gain Adjust

Figure 4 shows the signal path interconnections between the HC-5512D and HC-5510 single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Figure 5 shows the signal path interconnections between the HC-5512D and the HC-55564 CVSD. For the circuit shown, the audio signal into the CVSD should be 1Vp-p over the 3.2kHz band to obtain a flat response. R_A, R_B and C_A form a simple lead lag filter at the output of the HC-5512D receive filter which introduces a pole and a zero at 3.3kHz to help compensate against the filters' inherent sin x/x characteristic. (See Figure 3). Note that the transmit side of the filter provides an inherent +3dB voltage gain, and the resistor RD, at VFRI causes a voltage loss from audio out to VFRI, owing to the 100kΩ output impedance of the CVSD at audio out. Generally, the higher the RD value used, the more thermal noise introduced to the circuit.

Optimum noise and distortion performance will be obtained for the HC-5512D filter when operated with system peak overload voltages of ±2.5V to ±3.2 at VF_XO and VF_RO. When interfacing to a PCM CODEC or CVSD with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the HC-5512/12A/12C/12D filter can be used with the HC-5510/11 series CODEC which has a 5.5V peak overload voltage, or with the HC-55564 CVSD which has a 4.0V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC or CVSD output are required in this case.

Board Layout

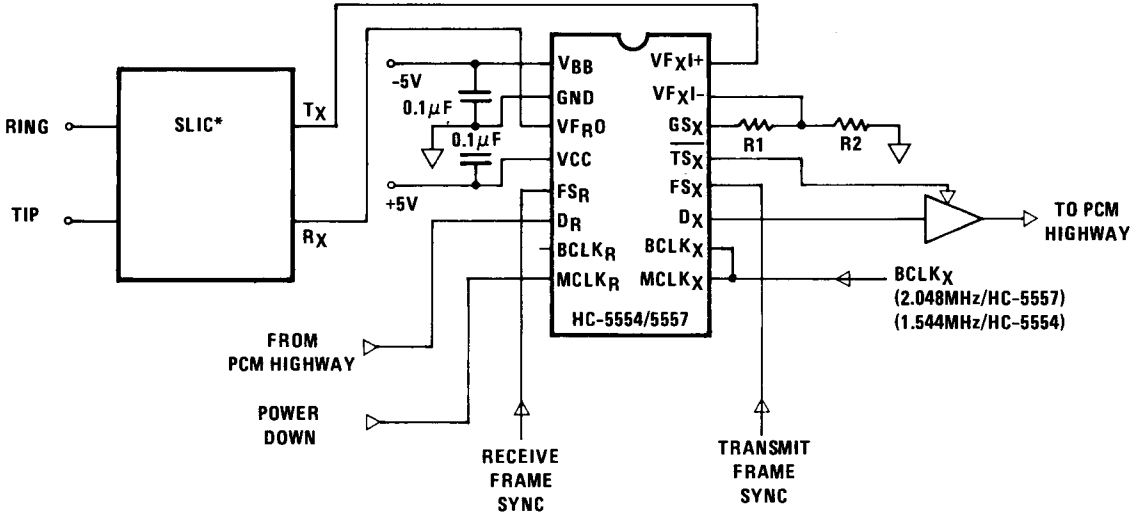
Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground o feach filter and each CVSD should be connected to digital ground at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC, and each filter and CVSD is recommended. Ground loops should be avoided between GNDA and GNDD, between the GNDA traces of adjacent filters and CODECs, and between the analog ground traces of adjacent filters and CVSDs.

Operating Instructions

Ground should be applied to the device before any other connection. Although V_{CC} and V_{BB} can be connected in any order, one should check that voltages on all inputs and on supply rails stay within absolute maximum ratings even for very short periods to avoid any latch-up. All ground connections to each device should meet at a common point as close as possible to the GND pin.

Two 0.1μF decoupling capacitors are required from the common ground point to V_{CC} and V_{BB}.

The ground point of each COFIDEC should be tied to a common card ground in star formation, rather than via a ground bus.



*HC-5502A, HC-5504, HC-5508 OR TRANSFORMER

TYPICAL SYNCHRONOUS APPLICATION