

MM58548 Multiplexed LCD Driver

General Description

The MM58548 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P and N-channel devices. It drives a 16-row by 16-column dot matrix LCD array directly under control of an external microprocessor. The MM58548 can be used with an MM58539 to drive a display that has up to 16 rows and an arbitrary number of columns. Data is input serially from the microprocessor which will service the drivers in response to an interrupt signal.

The circuit is available in either 40-pin molded dual-in-line packages or dice.

Features

- Drives up to 16 rows and 16 columns
- Expandable to larger displays with MM58539
- Flexible organization allows any display pattern
- Simple 3-line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On-chip oscillator
- Compatible with HLCD 0548

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

Block Diagram

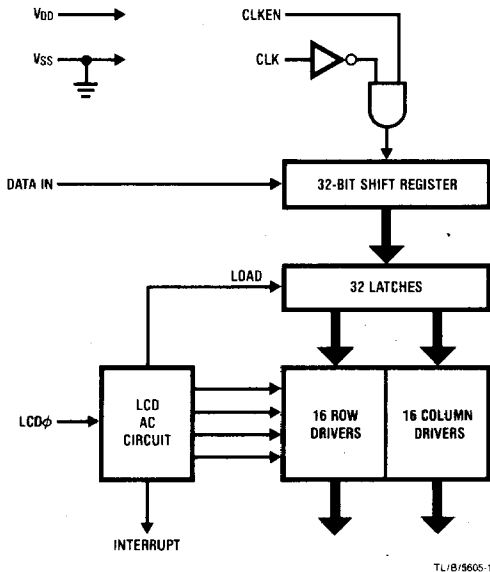


FIGURE 1

Connection Diagram

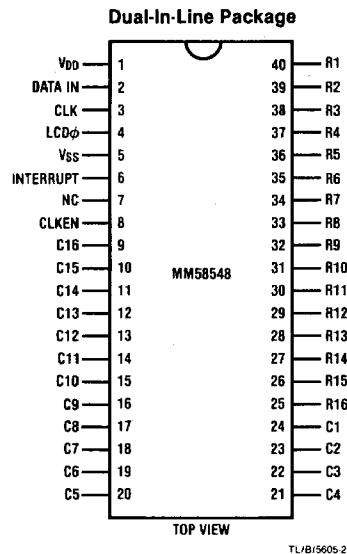


FIGURE 2

Order Number MM58548N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin
Voltage at Any Display Pin
Storage Temperature

$V_{DD} - 20V$ to $V_{DD} + 0.3V$
 $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
 $-65^{\circ}C$ to $150^{\circ}C$

Power Dissipation
Operating Temperature
Lead Temperature (Soldering, 10 seconds)

250 mW
 $-40^{\circ}C$ to $70^{\circ}C$
 $300^{\circ}C$

Electrical Characteristics $T_A = 25^{\circ}C$ and $V_{DD} = 5V$ unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage, V_{DD}		3		15	V
Supply Current, I_{DD}				400	μA
Input High Level, V_{IH}	All V_{DD}	$0.75 V_{DD}$		V_{DD}	V
Input Low Level, V_{IL}	All V_{DD}	$V_{DD} - 15$		$0.25 V_{DD}$	V
Input Leakage, I_L				5	μA
Input Capacitance, C_i				5	pF
Row Output High	All V_{DD}			V_{DD}	V
Row Output Low	All V_{DD}	V_{SS}			V
Row Unselected	All V_{DD}		$0.5 V_{DD}$		V
Column O/P High	All V_{DD}		$0.68 V_{DD}$		V
Column O/P Low	All V_{DD}		$0.32 V_{DD}$		V
Average DC Offset, Any Display Element				100	mV
Row and Column Output Impedance	$I_L = 10 \mu A$			40	$k\Omega$
Interrupt Output Impedance	$I_L = 100 \mu A$			1	$k\Omega$
Clock Frequency, f		DC		1.5	MHz
Data-In Set-Up Time, t_{DS}	Data Change to Clock Fall	300			ns
Data-In Hold Time, t_{DH}	Clock Fall to Data Change	100			ns
LCD ϕ to Interrupt Out Delay, t_D		300			ns
Clock Rise/Fall Time, t_r, t_f				200	ns
LCD ϕ High Level	All V_{DD}	$0.9 V_{DD}$		V_{DD}	V
LCD ϕ Low Level	All V_{DD}	0		$0.1 V_{DD}$	V
LCD ϕ Input Impedance		1		3	M Ω

Functional Description

A block diagram of the MM58548 LCD driver is shown in *Figure 1*. A connection diagram is shown in *Figure 2*.

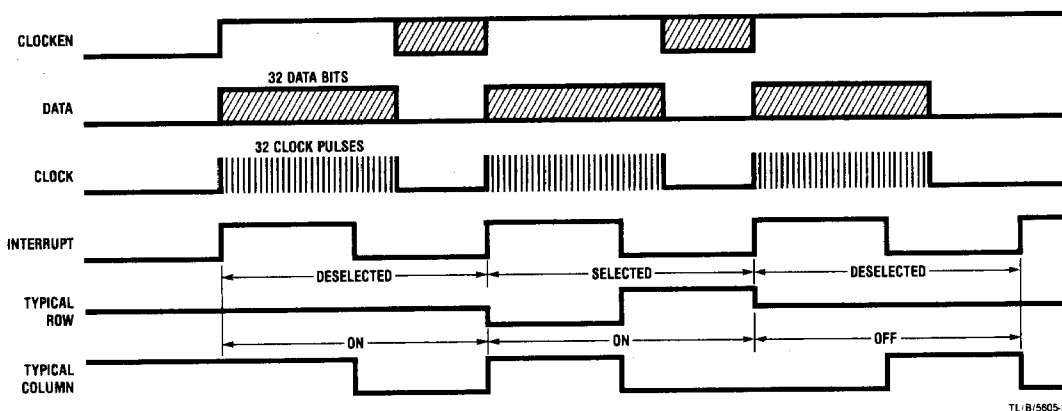
MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock. A data logic '1' on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer of data from the shift register to the latches occurs and the row and column outputs change accordingly. This interrupt signal also acts as a refresh request and new data must be loaded before the next interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 9 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown in *Figure 3*. Rows are out of phase with interrupt if selected and at midpoint voltage otherwise; levels are V_{DD} , V_{SS} and $V_{DD}/2$. Columns are in phase with interrupt if selected and out of phase if not selected; levels are $0.32 V_{DD}$ and $0.68 V_{DD}$. Backplanes, i.e., row and column outputs, should be addressed sequentially and individually. If the supply voltage has to be altered to optimize LCD contrast or for temperature compensation, it is recommended that all positive supply terminals be connected together and the negative supply varied.

Functional Description (Continued)



TLB/5805-3

FIGURE 3

LCD ϕ INPUT

This input can be used in two modes:

1) Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS} , this input operates as an RC oscillator. This frequency is divided by two to provide a 50% duty cycle and will then appear at the interrupt output as a frequency of approximately $1/RC$, where R should exceed $1M\Omega$.

The interrupt output frequency should be the minimum no-flicker frequency (approximately 30 Hz) multiplied by the number of backplanes used.

2) Driven Mode

In this mode, the interrupt output will follow the waveform input on the LCD ϕ pin.

LCD ϕ of a driven mode device should preferably be connected to the interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% \pm 1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes

the mode detect logic. This signal sets all the row outputs to the deselected state, all the column outputs to the off state and the interrupt output high. If the circuit is in the oscillating mode, the LCD ϕ pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCD ϕ pin is held high by the low impedance interrupt output of the previous device. When the first clock pulse goes to a logic '1', the level on the LCD ϕ pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating. The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the driven mode, the interrupt frequency is in phase with the input frequency on LCD ϕ .

CASCADING

Figure 4 shows an application where 2 or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The interrupt output from the 'master' oscillating circuit is connected to the LCD ϕ input of the other 'slave' circuits, with the 'slave' interrupt going to the microprocessor. It would also be possible to connect all LCD ϕ inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and data with separate clock-enable lines or by holding CLKEN high and having a common clock and separate data bus lines or vice-versa.

Functional Description (Continued)

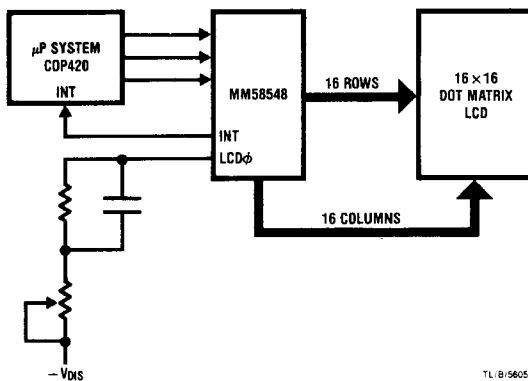


FIGURE 4