

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	- 40 to + 85 °C
Storage temperature (T_{ST}).....	- 65 to + 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	- 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	- 0.5 V to $V_{CC} + 0.5$ V
Input current on any pin during overload condition.....	- 10 mA to + 10 mA
Absolute sum of all input currents during overload condition	100 mA
Power dissipation.....	TBD

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

$V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$;

$T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ for the SAB-C501

$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ for the SAF-C501

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{\text{EA}}$, RESET)	V_{IL}	-0.5	$0.2 V_{CC} - 0.1$	V	—
Input low voltage ($\overline{\text{EA}}$)	V_{IL1}	-0.5	$0.2 V_{CC} - 0.3$	V	—
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2 V_{CC} + 0.1$	V	—
Input high voltage (except XTAL1, $\overline{\text{EA}}$, RESET)	V_{IH}	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	—
Input high voltage to XTAL1	V_{IH1}	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	
Input high voltage to $\overline{\text{EA}}$, RESET	V_{IH2}	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	—
Output low voltage (ports 1, 2, 3)	V_{OL}	—	0.45	V	$I_{OL} = 1.6\text{ mA}^{1)}$
Output low voltage (port 0, ALE, $\overline{\text{PSEN}}$)	V_{OL1}	—	0.45	V	$I_{OL} = 3.2\text{ mA}^{1)}$
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 $0.9 V_{CC}$	— —	V	$I_{OH} = -80\text{ }\mu\text{A}$, $I_{OH} = -10\text{ }\mu\text{A}$
Output high voltage (port 0 in external bus mode, ALE, $\overline{\text{PSEN}}$)	V_{OH1}	2.4 $0.9 V_{CC}$	— —	V	$I_{OH} = -800\text{ }\mu\text{A}^{2)}$, $I_{OH} = -80\text{ }\mu\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	μA	$V_{IN} = 0.45\text{ V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TI}	-65	-650	μA	$V_{IN} = 2\text{ V}$
Input leakage current (port 0, $\overline{\text{EA}}$)	I_{LI}	—	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	—	10	pF	$f_C = 1\text{ MHz}$, $T_A = 25\text{ }^{\circ}\text{C}$
Power supply current:					
Active mode, 12 MHz ⁷⁾	I_{CC}	—	21	mA	$V_{CC} = 5\text{ V}$, ⁴⁾
Idle mode, 12 MHz ⁷⁾	I_{CC}	—	4.8	mA	$V_{CC} = 5\text{ V}$, ⁵⁾
Active mode, 20 MHz ⁷⁾	I_{CC}	—	31.1	mA	$V_{CC} = 5\text{ V}$, ⁴⁾
Idle mode, 20 MHz ⁷⁾	I_{CC}	—	7.0	mA	$V_{CC} = 5\text{ V}$, ⁵⁾
Active mode, 40 MHz ⁷⁾	I_{CC}	—	56.5	mA	$V_{CC} = 5\text{ V}$, ⁴⁾
Idle mode, 40 MHz ⁷⁾	I_{CC}	—	12.5	mA	$V_{CC} = 5\text{ V}$, ⁵⁾
Power Down Mode	I_{PD}	—	50	μA	$V_{CC} = 2 \dots 5.5\text{ V}^{3)}$

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.
- 3) I_{PD} (Power Down Mode) is measured under following conditions:
 $\overline{EA} = \text{Port0} = V_{CC}$; $\text{RESET} = V_{SS}$; XTAL2 = N.C.; XTAL1 = V_{SS} ; all other pins are disconnected.
- 4) I_{CC} (active mode) is measured with:
 XTAL1 driven with t_{CLCH} , $t_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 = N.C.;
 $\overline{EA} = \text{Port0} = \text{RESET} = V_{CC}$; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).
- 5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
 XTAL1 driven with t_{CLCH} , $t_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; XTAL2 = N.C.;
 $\text{RESET} = \overline{EA} = V_{SS}$; $\text{Port0} = V_{CC}$; all other pins are disconnected;
- 7) $I_{CC\text{ MAX}}$ at other frequencies is given by:
 active mode: $I_{CC} = 1.27 \times f_{OSC} + 5.73$
 idle mode: $I_{CC} = 0.28 \times f_{OSC} + 1.45$
 where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at $V_{CC} = 5$ V.

AC Characteristics for SAB-C501-LN / C501-RN

$V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ for the SAB-C501

$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ for the SAF-C501

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values		Unit
		12 MHz Clock	Variable Clock $1/t_{\text{read}} = 3.5\text{ MHz to }12\text{ MHz}$	

AC Characteristics for SAB-C501-L / C501-1R

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/ <i>t</i> _{CLCL} = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	<i>t</i> _{RLRH}	400	—	6 <i>t</i> _{CLCL} − 100	—	ns
$\overline{\text{WR}}$ pulse width	<i>t</i> _{WLWH}	400	—	6 <i>t</i> _{CLCL} − 100	—	ns
Address hold after ALE	<i>t</i> _{LLAX2}	30	—	<i>t</i> _{CLCL} − 53	—	ns
$\overline{\text{RD}}$ to valid data in	<i>t</i> _{RLDV}	—	252	—	5 <i>t</i> _{CLCL} − 165	ns
Data hold after $\overline{\text{RD}}$	<i>t</i> _{RHDX}	0	—	0	—	ns
Data float after $\overline{\text{RD}}$	<i>t</i> _{RHDZ}	—	97	—	2 <i>t</i> _{CLCL} − 70	ns
ALE to valid data in	<i>t</i> _{LLDV}	—	517	—	8 <i>t</i> _{CLCL} − 150	ns
Address to valid data in	<i>t</i> _{AVDV}	—	585	—	9 <i>t</i> _{CLCL} − 165	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	<i>t</i> _{LLWL}	200	300	3 <i>t</i> _{CLCL} − 50	3 <i>t</i> _{CLCL} + 50	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	<i>t</i> _{AVWL}	203	—	4 <i>t</i> _{CLCL} − 130	—	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	<i>t</i> _{WHLH}	43	123	<i>t</i> _{CLCL} − 40	<i>t</i> _{CLCL} + 40	ns
Data valid to $\overline{\text{WR}}$ transition	<i>t</i> _{QVWX}	33	—	<i>t</i> _{CLCL} − 50	—	ns
Data setup before $\overline{\text{WR}}$	<i>t</i> _{QVWH}	433	—	7 <i>t</i> _{CLCL} − 150	—	ns
Data hold after $\overline{\text{WR}}$	<i>t</i> _{WHQX}	33	—	<i>t</i> _{CLCL} − 50	—	ns
Address float after $\overline{\text{RD}}$	<i>t</i> _{RLAZ}	—	0	—	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	—	20	ns
Fall time	t_{CHCL}	—	20	ns

AC Characteristics for SAB-C501-L20 / C501-1R20

$V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$

$T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ for the SAB-C501

$T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$ for the SAF-C501

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock 1/ <i>t</i> _{CLCL} = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	<i>t</i> _{LHLL}	60	—	2 <i>t</i> _{CLCL} – 40	—	ns
Address setup to ALE	<i>t</i> _{AVLL}	20	—	<i>t</i> _{CLCL} – 30	—	ns
Address hold after ALE	<i>t</i> _{LLAX}	20	—	<i>t</i> _{CLCL} – 30	—	ns
ALE low to valid instr in	<i>t</i> _{LLIV}	—	100	—	4 <i>t</i> _{CLCL} – 100	ns
ALE to $\overline{\text{PSEN}}$	<i>t</i> _{LLPL}	25	—	<i>t</i> _{CLCL} – 25	—	ns
$\overline{\text{PSEN}}$ pulse width	<i>t</i> _{PLPH}	115	—	3 <i>t</i> _{CLCL} – 35	—	ns
$\overline{\text{PSEN}}$ to valid instr in	<i>t</i> _{PLIV}	—	75	—	3 <i>t</i> _{CLCL} – 75	ns
Input instruction hold after $\overline{\text{PSEN}}$	<i>t</i> _{PXIX}	0	—	0	—	ns
Input instruction float after $\overline{\text{PSEN}}$	<i>t</i> _{PXIZ} ^{*)}	—	40	—	<i>t</i> _{CLCL} – 10	ns
Address valid after $\overline{\text{PSEN}}$	<i>t</i> _{PXAV} ^{*)}	47	—	<i>t</i> _{CLCL} – 3	—	ns
Address to valid instr in	<i>t</i> _{AVIV}	—	190	—	5 <i>t</i> _{CLCL} – 60	ns
Address float to $\overline{\text{PSEN}}$	<i>t</i> _{AZPL}	0	—	0	—	ns

*) Interfacing the SAB-C501 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C501-L20 / C501-1R20

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz Clock		Variable Clock 1/ <i>t</i> _{CLCL} = 3.5 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	<i>t</i> _{RLRH}	200	–	6 <i>t</i> _{CLCL} – 100	–	ns
$\overline{\text{WR}}$ pulse width	<i>t</i> _{WLWH}	200	–	6 <i>t</i> _{CLCL} – 100	–	ns
Address hold after ALE	<i>t</i> _{LLAX2}	20	–	<i>t</i> _{CLCL} – 30	–	ns
$\overline{\text{RD}}$ to valid data in	<i>t</i> _{RLDV}	–	155	–	5 <i>t</i> _{CLCL} – 95	ns
Data hold after $\overline{\text{RD}}$	<i>t</i> _{RHDZ}	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	<i>t</i> _{RHDZ}	–	76	–	2 <i>t</i> _{CLCL} – 24	ns
ALE to valid data in	<i>t</i> _{LLDV}	–	250	–	8 <i>t</i> _{CLCL} – 150	ns
Address to valid data in	<i>t</i> _{AVDV}	–	285	–	9 <i>t</i> _{CLCL} – 165	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	<i>t</i> _{LLWL}	100	200	3 <i>t</i> _{CLCL} – 50	3 <i>t</i> _{CLCL} + 50	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	<i>t</i> _{AVWL}	70	–	4 <i>t</i> _{CLCL} – 130	–	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	<i>t</i> _{WHLH}	20	80	<i>t</i> _{CLCL} – 30	<i>t</i> _{CLCL} + 30	ns
Data valid to $\overline{\text{WR}}$ transition	<i>t</i> _{QVWX}	5	–	<i>t</i> _{CLCL} – 45	–	ns
Data setup before $\overline{\text{WR}}$	<i>t</i> _{QVWH}	200	–	7 <i>t</i> _{CLCL} – 150	–	ns
Data hold after $\overline{\text{WR}}$	<i>t</i> _{WHQX}	10	–	<i>t</i> _{CLCL} – 40	–	ns
Address float after $\overline{\text{RD}}$	<i>t</i> _{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 20 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	50	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	—	12	ns
Fall time	t_{CHCL}	—	12	ns

AC Characteristics for SAB-C501-L40 / C501-1R40

Advance Information

$V_{CC} = 5\text{ V} \pm 10\%, -15\%$; $V_{SS} = 0\text{ V}$

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ for the SAB-C501

$T_A = -40^\circ\text{C to } 85^\circ\text{C}$ for the SAF-C501

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock 1/ t_{CLCL} = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	—	2 t_{CLCL} - 15	—	ns
Address setup to ALE	t_{AVLL}	10	—	t_{CLCL} - 15	—	ns
Address hold after ALE	t_{LLAX}	10	—	t_{CLCL} - 15	—	ns
ALE low to valid instr in	t_{LIIV}	—	55	—	4 t_{CLCL} - 45	ns
ALE to PSEN	t_{LLPL}	10	—	t_{CLCL} - 15	—	ns
PSEN pulse width	t_{PIPH}	60	—	3 t_{CLCL} - 15	—	ns
PSEN to valid instr in	t_{PIIV}	—	25	—	3 t_{CLCL} - 50	ns
Input instruction hold after PSEN	t_{PXIX}	0	—	0	—	ns
Input instruction float after PSEN	$t_{PXIZ}^{*)}$	—	15	—	t_{CLCL} - 10	ns
Address valid after PSEN	$t_{PXAIV}^{*)}$	20	—	t_{CLCL} - 5	—	ns
Address to valid instr in	$t_{A\backslash IV}$	—	65	—	5 t_{CLCL} - 60	ns
Address float to PSEN	$t_{A\backslash PL}$	-5	—	-5	—	ns

*) Interfacing the SAB-C501 to devices with float times up to 20ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for SAB-C501-L40 / C501-1R40 (cont'd)

Advance Information

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock 1/ <i>t</i> _{CLCL} = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{\text{RD}}$ pulse width	<i>t</i> _{RLRH}	120	—	6 <i>t</i> _{CLCL} − 30	—	ns
$\overline{\text{WR}}$ pulse width	<i>t</i> _{WLWH}	120	—	6 <i>t</i> _{CLCL} − 30	—	ns
Address hold after ALE	<i>t</i> _{LLAX2}	10	—	2 <i>t</i> _{CLCL} − 15	—	ns
$\overline{\text{RD}}$ to valid data in	<i>t</i> _{RLDV}	—	75	—	5 <i>t</i> _{CLCL} − 50	ns
Data hold after $\overline{\text{RD}}$	<i>t</i> _{RHDX}	0	—	0	—	ns
Data float after $\overline{\text{RD}}$	<i>t</i> _{RHDZ}	—	38	—	2 <i>t</i> _{CLCL} − 12	ns
ALE to valid data in	<i>t</i> _{LLDV}	—	150	—	8 <i>t</i> _{CLCL} − 50	ns
Address to valid data in	<i>t</i> _{AVDV}	—	150	—	9 <i>t</i> _{CLCL} − 75	ns
ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	<i>t</i> _{LLWL}	60	90	3 <i>t</i> _{CLCL} − 15	3 <i>t</i> _{CLCL} + 15	ns
Address valid to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	<i>t</i> _{AVWL}	70	—	4 <i>t</i> _{CLCL} − 30	—	ns
$\overline{\text{WR}}$ or $\overline{\text{RD}}$ high to ALE high	<i>t</i> _{WHLH}	10	40	<i>t</i> _{CLCL} − 15	<i>t</i> _{CLCL} + 15	ns
Data valid to $\overline{\text{WR}}$ transition	<i>t</i> _{QVWX}	5	—	<i>t</i> _{CLCL} − 20	—	ns
Data setup before $\overline{\text{WR}}$	<i>t</i> _{QVWH}	125	—	7 <i>t</i> _{CLCL} − 50	—	ns
Data hold after $\overline{\text{WR}}$	<i>t</i> _{WHOX}	5	—	<i>t</i> _{CLCL} − 20	—	ns
Address float after $\overline{\text{RD}}$	<i>t</i> _{RLAZ}	—	0	—	0	ns

Advance Information

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	285.7	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	—	10	ns
Fall time	t_{CHCL}	—	10	ns

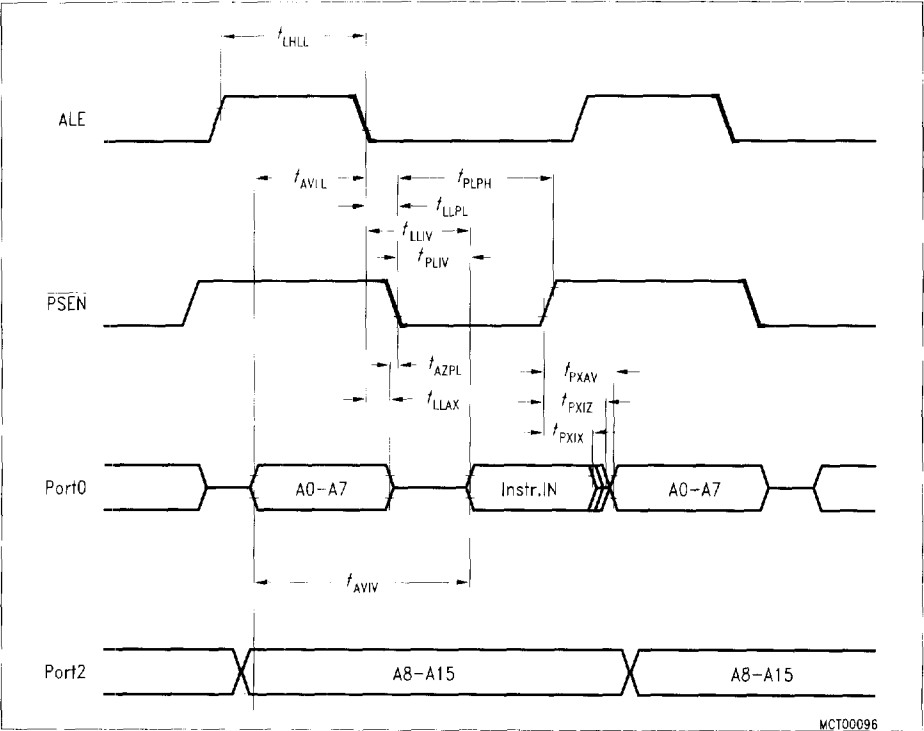


Figure 1
Program Memory Read Cycle

MCT00096

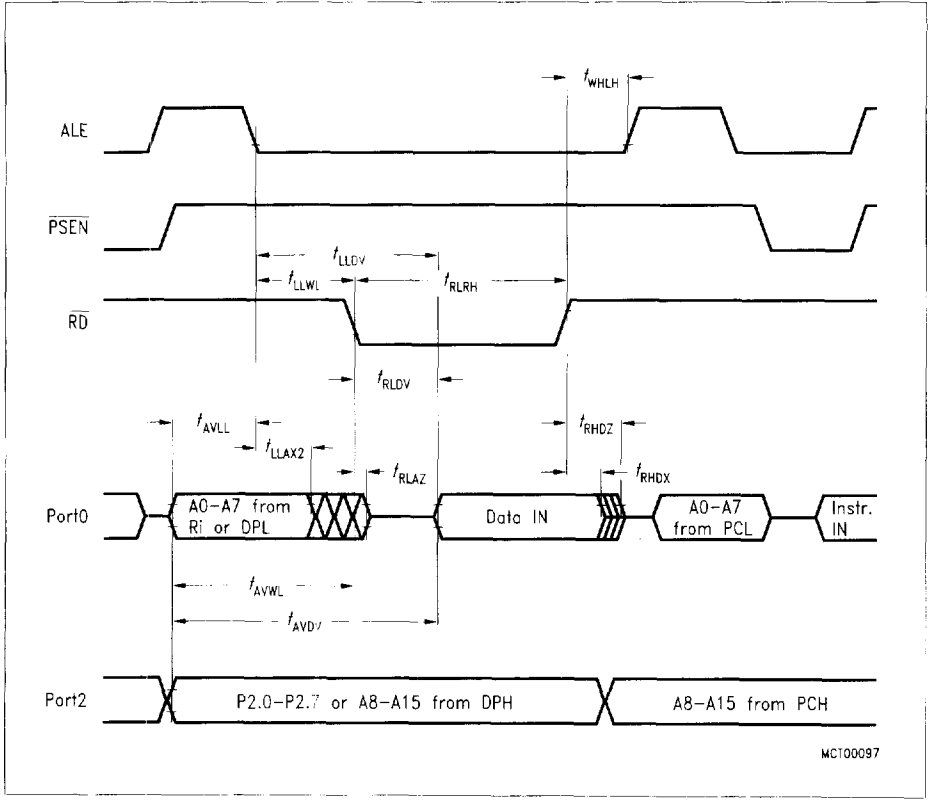


Figure 2
Data Memory Read Cycle

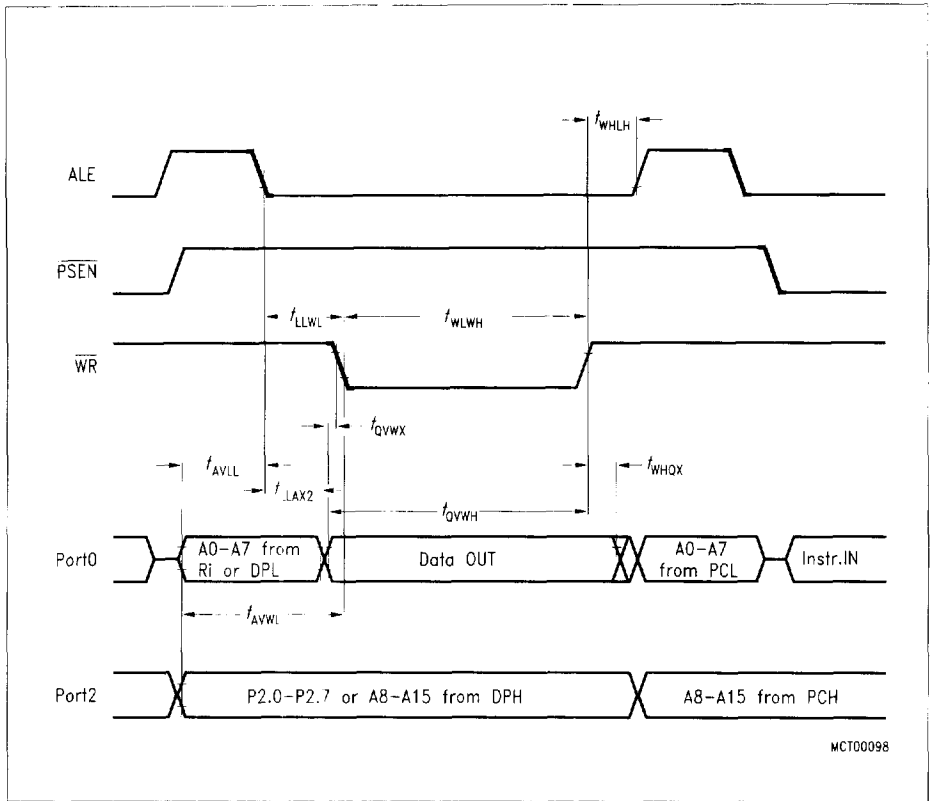


Figure 3
Data Memory Write Cycle

ROM Verification Characteristics for SAB-C501-1R

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	—	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELOV}	—	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

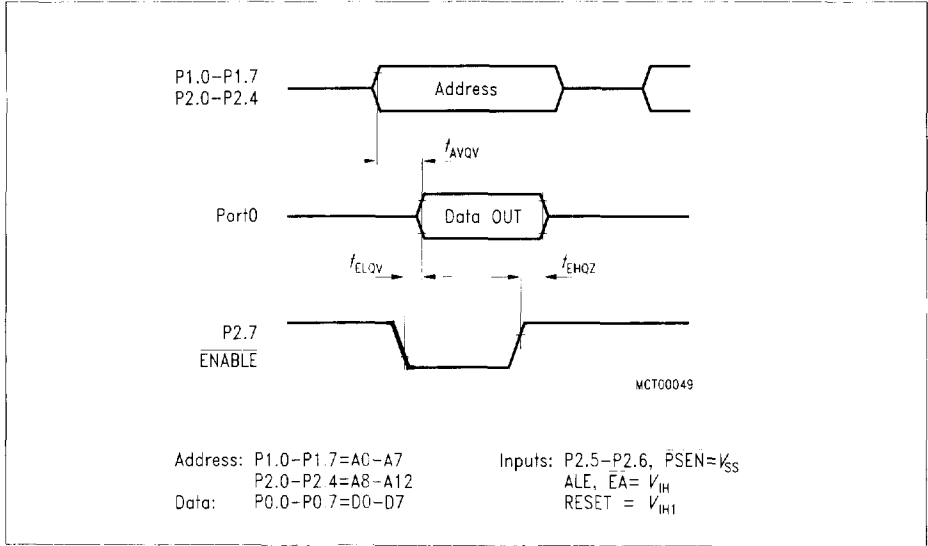


Figure 4
ROM Verification Mode 1

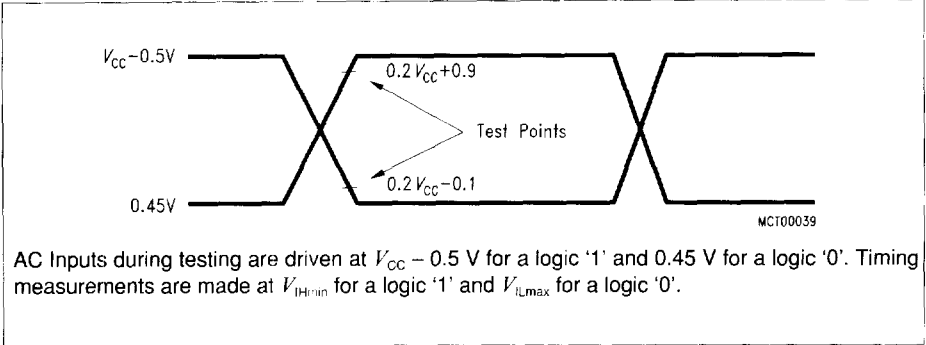


Figure 5
AC Testing: Input, Output Waveforms

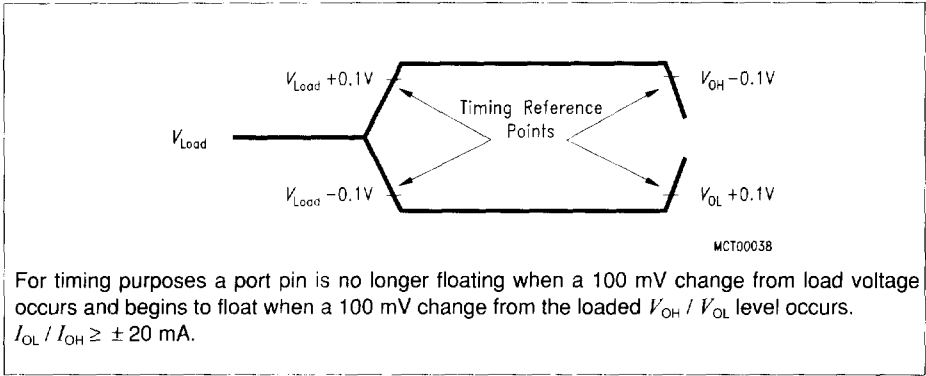


Figure 6
AC Testing: Float Waveforms

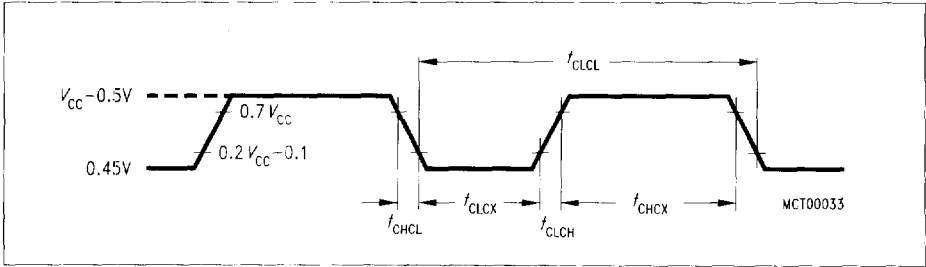


Figure 7
External Clock Cycle

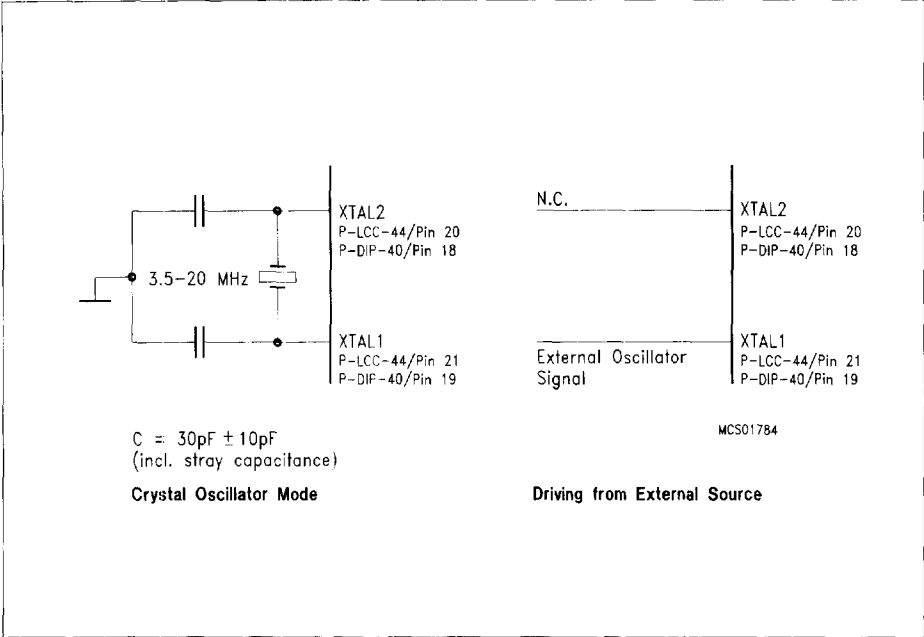


Figure 8
Recommended Oscillator Circuits