MX•COM, INC.
COMMUNICATION ICs

CMX639

DATA BULLETIN

Consumer / Commercial CVSD Digital Voice CODEC

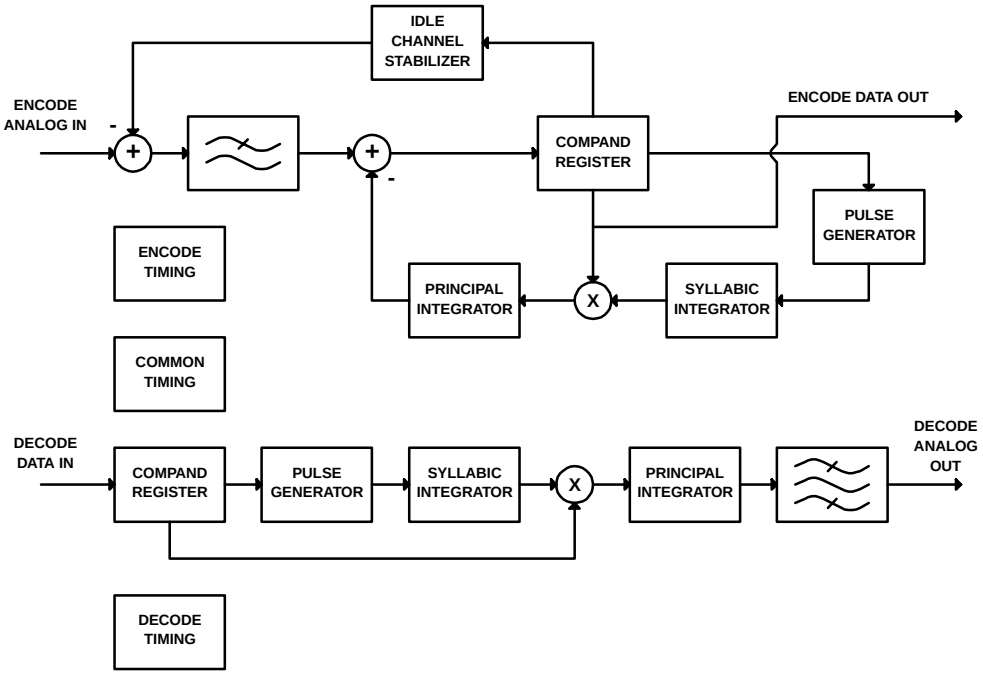
PRELIMINARY INFORMATION

Features

- **Single Chip Full Duplex CVSD CODEC**
  - **Integrated Input and Output Filters**
  - **Robust Coding for Wireless Links**
  - **Programmable Sampling Clocks**
  - **3 and 4 bit Companding Algorithms**
- **Low Power / Small Size for Portable Devices**
  - **1.9mA/2.75mA typ. @ 3V/5V**
  - **3.0V to 5.5V Operation**
  - **Powersave Mode**

Applications

- **Consumer & Business Handheld Devices**
- **Digital Voice Appliances**
  - **Spread Spectrum Wireless**
  - **Cordless Phones**
  - **Voice Recording & Storage**
  - **Delay Lines**
- **Time Domain Scramblers**
- **Multiplexers and Switches**



The CMX639 is a Continuously Variable Slope Delta Modulation (CVSD) full duplex CODEC for use in consumer and commercial digital voice communication systems. With its robust and selectable coding algorithms, low cost, very low power, and small size, the CMX639 is ideal for use in a wide variety of consumer and business digital voice applications. Its completely integrated CODEC simplifies design and eliminates the costs, complexity and risk of external filters and software algorithms.

8kbps to 128kbps data/sampling clock rates are supported both via external clock signals or internally generated, programmable clocks. Internal data/sampling clocks are derived from an on-chip reference oscillator that uses an external clock crystal. An internal data/sampling clock output signal is provided to synchronize external circuits, if desired. Multiplexer applications are also well supported by the encoder output's tri-state enable feature.

The CMX639 operates from 3.0V to 5.5V and is available in the following packages: 24-pin TSSOP (CMX639E2), 16-pin SOIC (CMX639D4) and 22-pin PDIP (CMX639P6).

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CONTENTS

Section **Page**

1 Block Diagram

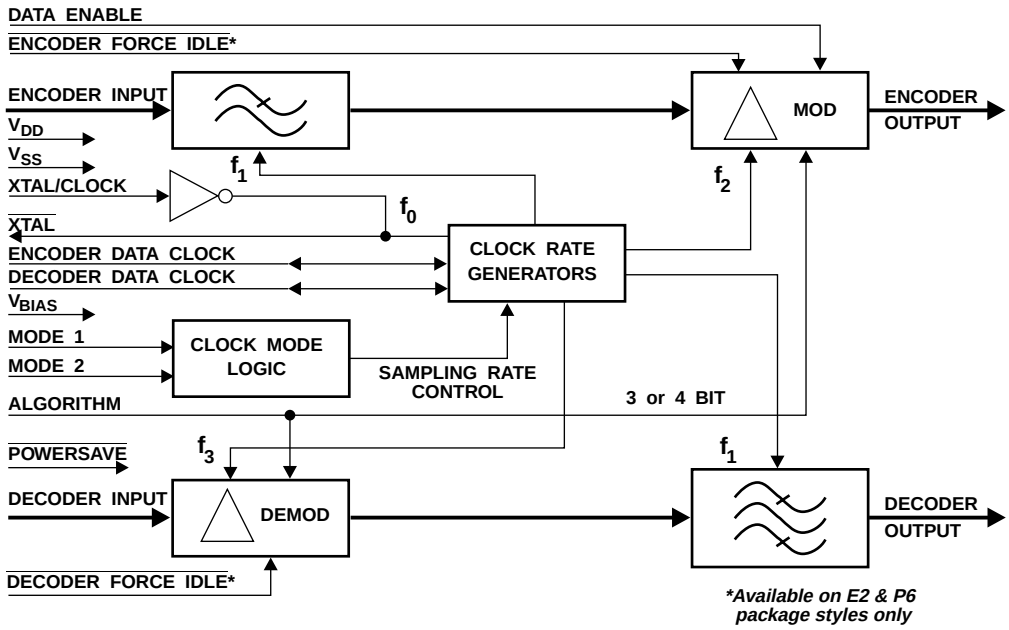


Figure 1: Block Diagram

2 Signal List

P6 22-pin PDIP	E2 24-pin TSSOP	D4 16-pin SOIC	Signal Name	Type	Description
1	1	1	Xtal/Clock	input	Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Table 3 and Figure 3.
	2		N/C		No Connection
2	3	2	$\overline{\text{Xtal}}$	output	The 1.024 MHz output of the clock oscillator inverter.
3	4		N/C		No Connection
4	5	3	Encoder Data Clock	input/ output	A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon Clock Mode 1, 2 inputs and Xtal frequency (see Table 3). Note: No internal pull-up is provided.
5	6	4	Encoder Output	output	The encoder digital output. This is a three-state output whose condition is set by the Data Enable and $\overline{\text{Powersave}}$ inputs. See Table 2.
6	7	Not present	$\overline{\text{Encoder Force Idle}}$	input	When this pin is at a logical '0' the encoder is forced to an idle state and the encoder digital output is 0101…, a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ pull-up.
7	8	5	Data Enable	input	Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 MΩ pull-up.
8	9		N/C		No Connection
9	10	6	Bias		Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C4. Internally pulled to V_{SS} when $\overline{\text{Powersave}}$ is a logical '0'.
10	11	7	Encoder Input	input	The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance driving the coupling capacitor should be less than 1kΩ. A lower driving source impedance will reduce encoder output channel noise levels. See Figure 2.
11	12	8	V_{SS}	power	Negative Supply
12	13		N/C		No Connection
13	14	9	Decoder Output	output	The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During 'Powersave' this output is open circuit.
14	15		N/C		No Connection
15	16	10	$\overline{\text{Powersave}}$	input	A logic '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1', the codec operates normally. Internal 1 MΩ pull-up.
	17		N/C		No Connection
16	18	Not present	$\overline{\text{Decoder Force Idle}}$	input	A logic '0' at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is a logical '1' the decoder operates as normal. Internal 1MΩ pull-up.
17	19	11	Decoder Input	input	The received digital signal input. Internal 1 MΩ pull-up.
18	20	12	Decoder Data Clock	input/ output	A logic I/O port. External decode clock input or internal data clock output, dependent upon Clock Mode 1 and 2 inputs. See Table 3. Note: No internal pull-up is provided.
19	21	13	Algorithm	input	A logic '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1 MΩ pull-up.
20	22	14	Clock Mode 2	input	Clock rates refer to f = 1024MHz Xtal/Clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Internal 1MΩ pull-ups. See Table 3.
21	23	15	Clock Mode 1	input	
22	24	16	V_{DD}	power	Positive Supply. A single 3.0V to 5.5V supply is required.

Table 1: Signal List

Data Enable	$\overline{\text{Powersave}}$	Encoder Output
1	1	Enable
0	don't care	High Z (open circuit)
1	0	V_{SS}

Table 2: Encoder Output

Clock Mode 1 input	Clock Mode 2 input	Data/Sampling Clock Rate (Xtal/clock = f)	Example for f = 1.024MHz
0	0	External Clocks	External Clocks
0	1	Internally generated @ f/16	Internally generated @ 64kbps
1	0	Internally generated @ f/32	Internally generated @ 32kbps
1	1	Internally generated @ f/64	Internally generated @ 16kbps

Table 3: Clock Modes and Pins

3 External Components

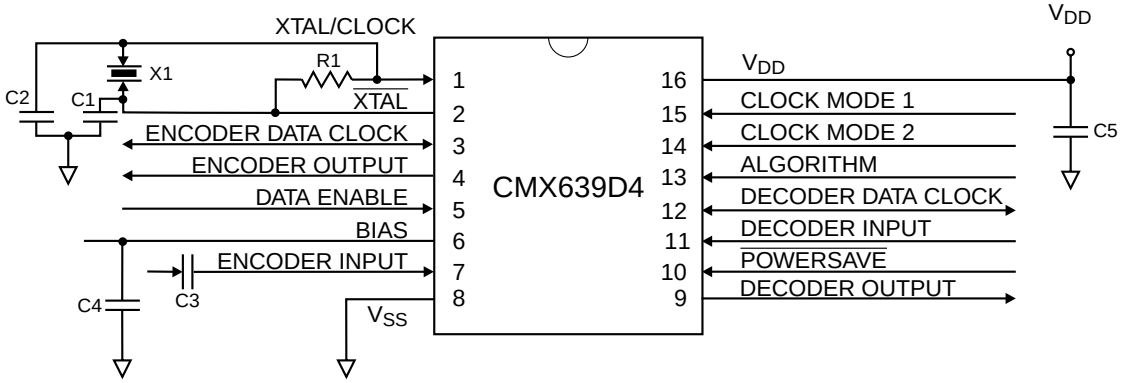


Figure 2: Recommended External Components for Typical Application

R1	Note 1	1MΩ	±10%
C1	Note 2	33pF	±20%
C2	Note 2	33pF	±20%
C3	Note 3	1.0µF	±20%

C4	Note 4	1.0µF	±20%
C5	Note 5	1.0µF	±20%
X1	Note 6, 7	1.024MHz	

Table 4: Recommended External Components for Typical Application

Notes:

1. Oscillator inverter bias resister
2. Xtal circuit load capacitor
3. The drive source impedance connected to the coupling capacitor's input node, rather than the CMX639 ENCODER INPUT pin node, should be should be less than 1kΩ. Output idle channel noise levels will improve with even lower source impedances driving the coupling capacitor's input node.
4. Bias decoupling capacitor
5. V_{DD} decoupling capacitor
6. A 1.024MHz Xtal/Clock input will yield exactly 16kbps/32kbps/64kbps internally generated data clock rates.
7. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult your crystal manufacturer.

4 Application

4.1 CODEC Integration

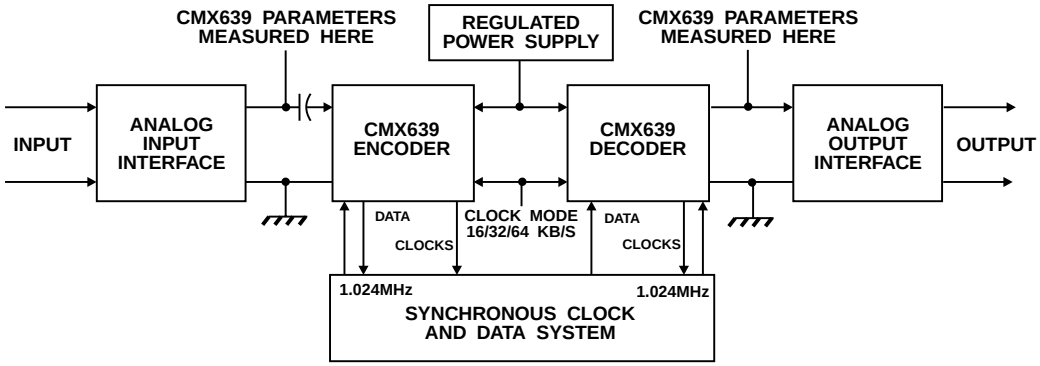


Figure 3: System Configuration using the CMX639

5 Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pin	-20	20	mA
E2 Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		300	mW
Derating above 25°C		3	mW/°C above 25°C
Storage Temperature	-40	125	°C
Operating Temperature	-40	85	°C
P6 / D4 Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Storage Temperature	-40	125	°C
Operating Temperature	-40	85	°C

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ.	Max.	Units
Supply (V_{DD} - V_{SS})	2.7		5.5	V
Operating Temperature	-40		85	°C
Xtal Frequency	0.500		2.048	MHz

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 3.0V to 5.5V at T_{AMB} = -40 to +85°C, Audio Test Frequency = 820Hz, Xtal/Clock f_0 = 1.024MHz
Sample Clock Rate = 32kbps, Audio level 0dB ref (0 dBm0) = 489mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Current (Enabled)					mA
V_{DD} = 3.0V	6		1.90		mA
V_{DD} = 5.0V	6		2.75		mA
Supply Current (Powersave)	6		600		µA
Input logic '1'		70% V_{DD}			V
Input Logic '0'				30% V_{DD}	V
Output Logic '1'		80% V_{DD}			V
Output Logic '0'				20% V_{DD}	V
Digital input Impedance					
Logic I/O pins		1			MΩ
Logic Input pins, Pull-up Resistor	1	300			kΩ
Digital output impedance				4	kΩ
Analog Input Impedance	2		100		kΩ
Analog Output Impedance				800	Ω
Three State Output Leakage			±4		µA
Insertion Loss	3		0		dB
Dynamic Values					
Encoder					
Analog signal Input levels					
V_{DD} = 3.0V	7	-37		6	dB
V_{DD} = 5.0V	7	-33		10	dB
Principal Integrator Frequency			160		Hz
Encoder Passband	4		3240		Hz
Compand Time Constant			5		ms
Decoder					
Analog Signal Output Levels	7				
V_{DD} = 3.0V	7	-37		6	dB
V_{DD} = 5.0V	7	-33		10	dB
Decoder Passband	4		3200		Hz
Encoder Decoder (Full Codec)					
Passband	4	300		3400	Hz
Stopband		6		10	KHz
Stopband Attenuation			60		dB
Passband Gain			0		dB
Passband Ripple		-3		3	dB
Output Noise (Input Short Circuit)	8		-60		dBmOp
Perfect Idle Channel Noise					
(Encode Forced)	8, 9		-63		dBmOp

	Notes	Min.	Typ.	Max.	Units
Group Delay Distortion	5				
(1000Hz-2600Hz)				450	µs
(600Hz-2800Hz)				750	µs
(500Hz-3000Hz)				1500	µs
Xtal/clock Frequency	10, 11	0.500	1.024	2.048	MHz

Notes:

1. All logic inputs except Encoder and Decoder Data clocks.
2. The source impedance driving the coupling capacitor should be less than 1kΩ. A lower driving source impedance will reduce encoder output channel noise levels.
3. For an Encoder/Decoder combination.
4. See Figure 5.
5. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input
6. Not including any current drawn from the device by external circuits.
7. Recommended values
8. dBmOp units are measured after the application of a psophometrically weighted filter that is commonly used in voice communication applications per CCITT Recommendation G.223.
9. Forced idle encode/decode control not available on D4 (16 pin SOIC) package.
10. Some applications may benefit from the use of an Xtal/clock frequency other than 1.024MHz.
    Note: CODEC time constants and filter response curves are effectively proportional to Xtal/clock frequency and so will shift with the use of Xtal/clock frequencies other than 1.024MHz. For example, the specified Encoder Decoder (Full Codec) Passband of 300Hz min. to 3400Hz max. for a 1.024MHz Xtal/clock will shift to 600Hz min. to 6800Hz max. when the device is operated from a 2.048MHz Xtal/clock. For this reason, all CMX639 CODECs involved in the same communications link should usually be operated from the same Xtal/clock frequency.

    Example 1: A design saves the cost of a 1.024MHz Xtal or clock generator by making use of an already existing clock source of a frequency other than 1.024MHz.

    Example 2: Best noise performance is achieved when the CMX639 CODEC data clock is internally generated. If a CODEC bit rate other than 16kbps, 32kbps or 64kbps is desired then an Xtal/clock different than 1.024Mhz can be used to proportionately shift the available set of internally generated clock rates, as needed.

    Example 3: To increase the CODEC high frequency response and audio bandwidth a faster Xtal/Clock speed can be used. Other designs may prefer the proportionately higher CODEC bandwidths and data rates that can be supported with faster clock speeds.
11. In general, optimum CODEC performance is achieved when both encoder and decoder Xtal/Clock signals are synchronized. While this is practical in many telecom applications it may not be in others such as wireless data links. The CMX639 decoder can generally deliver best performance when its data clock is recovered/derived from the received data stream and applied as an external data clock to the decoder per the decoder timing depicted in Figure 4. Nonetheless, some Xtal/Clock frequency and data rate combinations are better served by the use of internal clocks. Experimentation with each specific design may provide the best guidance for making this design choice.

5.1.4 Timing

Serial Bus Timings (See Figure 4)		Min.	Typ.	Max.	Units
t_{CH}	Clock 1 pulse width	1.0			µs
t_{CL}	Clock 0 pulse width	1.0			µs
t_{IR}	Clock rise time	0	100		ns
t_{IF}	Clock fall time		100		ns
t_{SU}	Data set-up time			450	ns
t_H	Data hold time	600			ns
$t_{SU} + t_H$	Data true time		1.5		µs
t_{PCO}	Clock to output delay time		750		ns
t_{DR}	Data rise time		100		ns
t_{DF}	Data fall time		100		ns
Xtal input frequency = 1.024MHz					

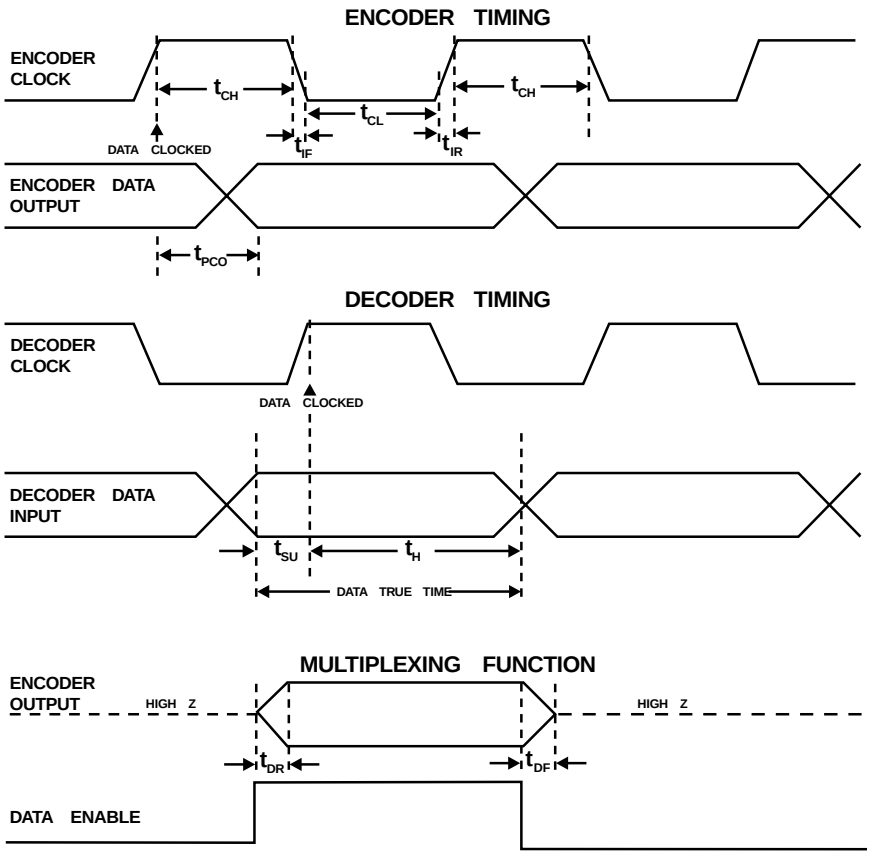


Figure 4: Serial Bus Timing

5.1.5 Typical Performance

5.1.5.1 CODEC Performance

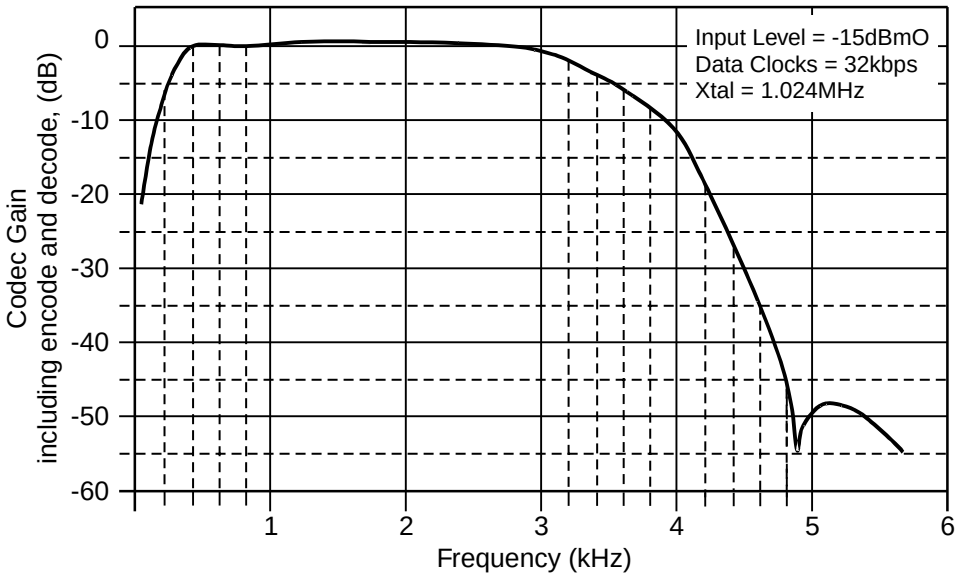


Figure 5: Typical CODEC Frequency Response (32kbps)

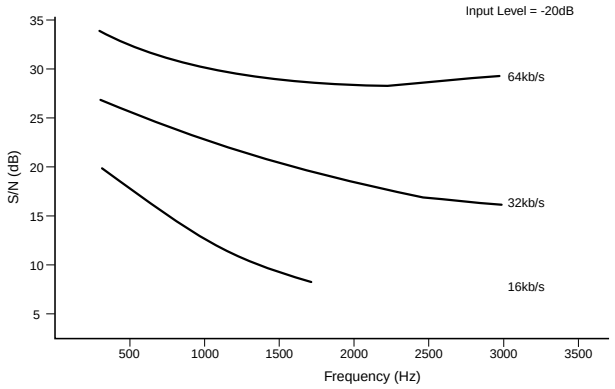


Figure 6: Typical S/N Ratio with Input Frequency

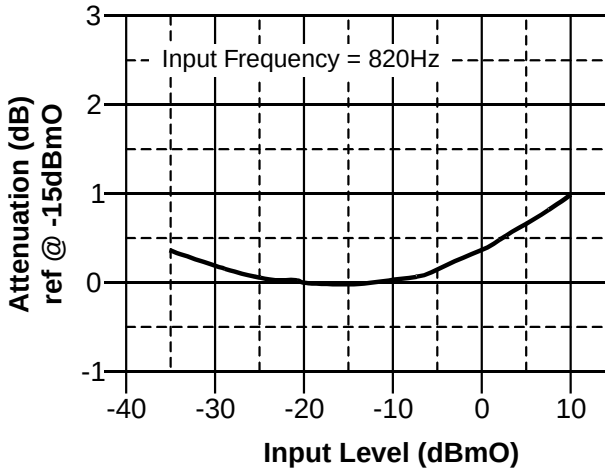


Figure 7: Typical Variation of Gain with Input Level (32kbps)

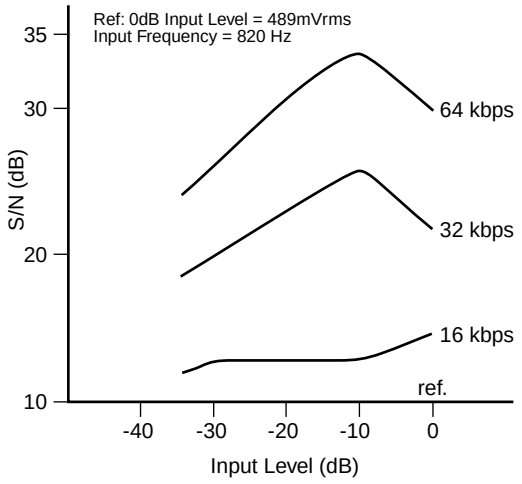
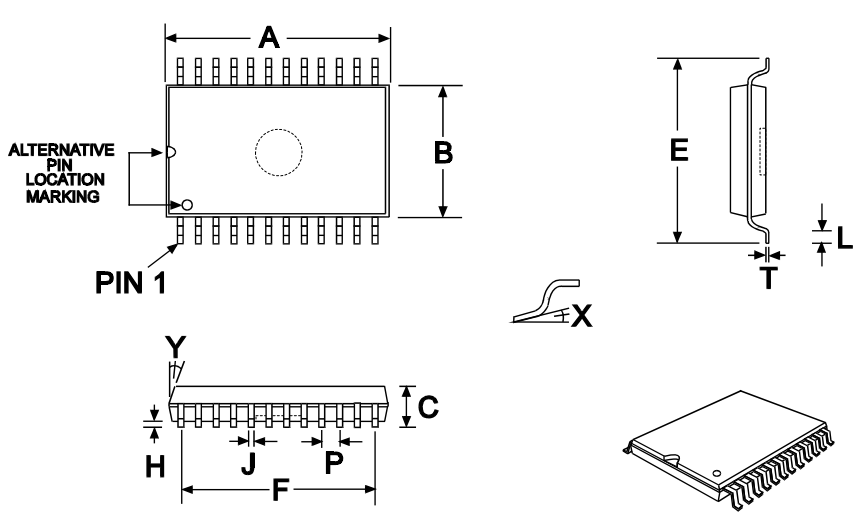


Figure 8: Typical S/N Ratio with Input Level

5.2 Packaging



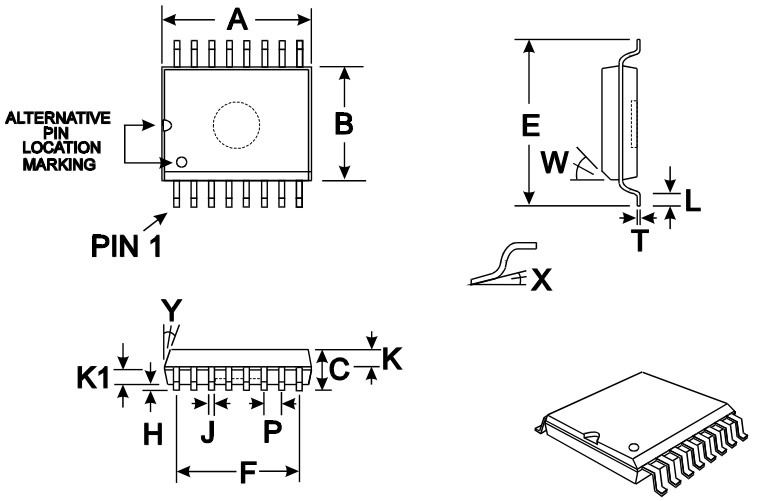
DIM.	MIN.	TYP.	MAX.
* A	0.303 (7.70)		0.311 (7.90)
* B	0.169 (4.30)		0.177 (4.50)
C	------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
F		0.286 (7.15)	
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.026 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
X	0°		7°
Y		12°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin TSSOP (E2) Mechanical Outline: *Order as part no. CMX639E2*



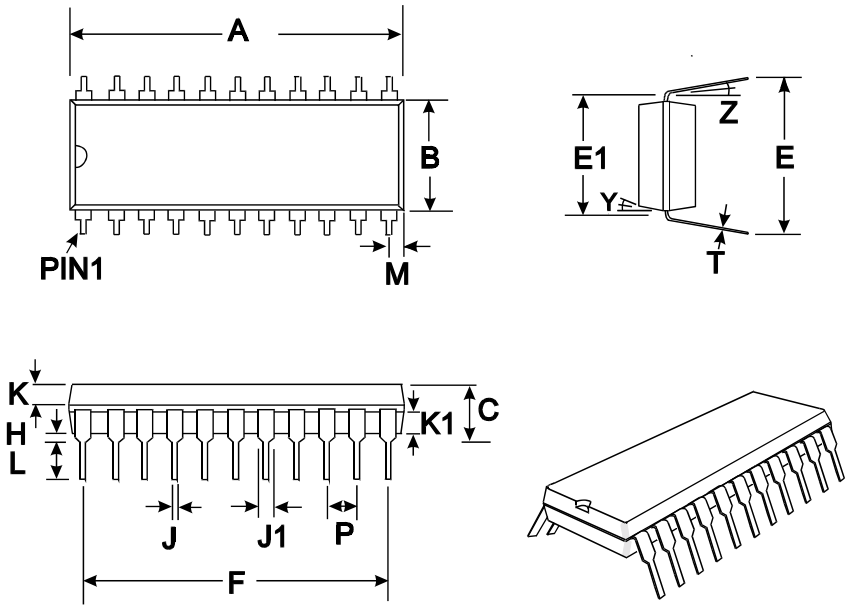
DIM.	MIN.	TYP.	MAX.
* A	0.395 (10.03)		0.413 (10.49)
* B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
F		0.350 (8.89)	
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 16-pin SOIC (DW) Mechanical Outline: *Order as part no. CMX639D4*



DIM.	MIN.	TYP.	MAX.
* A	1.080 (27.43)		1.10 (27.94)
* B	0.330 (8.38)		0.360 (9.14)
C	0.170 (4.32)		0.195 (4.95)
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.90)		0.420 (10.67)
F		1.0 (25.40)	
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.045 (1.14)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 22-pin PDIP (P) Mechanical Outline: *Order as part no. CMX639P6*

