Signetics

8X350

2K-Bit TTL Bipolar RAM (256 × 8)

Military
Bipolar Memory Products

Product Specification

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X305 based system. Internal circuitry is provided for direct use in 8X305 applications. When used with the 8X305, the RAM address and data busses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-State outputs.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Ceramic DIP 400mil-wide	8X350/BWA

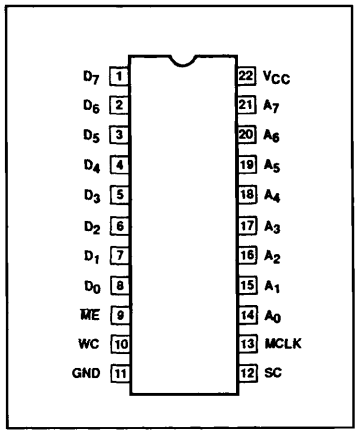
FEATURES

- On-chip address latches
- Schottky clamped
- One master enable input
- Directly interfaces with the 8X305 bipolar microprocessor with no external logic
- May be used on left or right bank
- Common I/O:
  - Inputs: PNP buffered
  - Outputs: 3-State

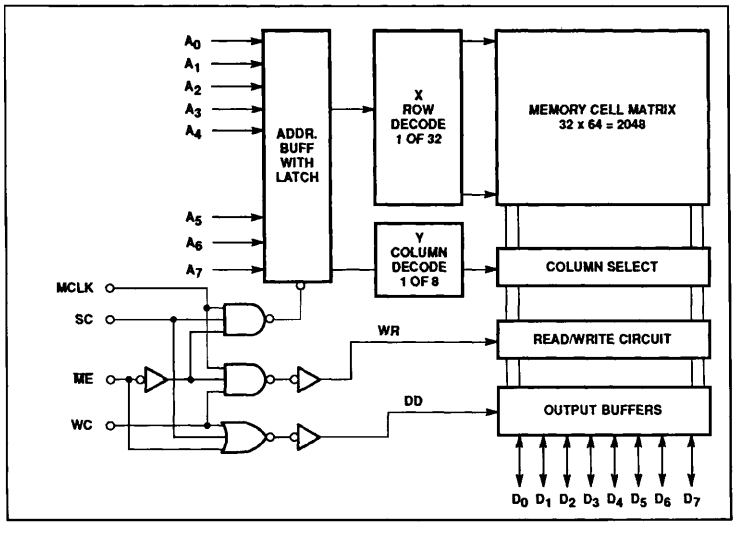
APPLICATIONS

- 8X305 working storage

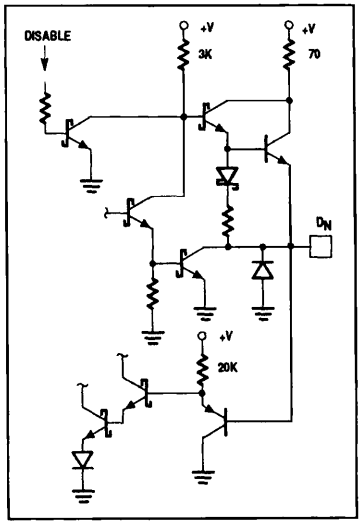
PIN CONFIGURATION



BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V[2]

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp[3]	V_{CC} = 4.75V, I_I = -18mA			-1.2	V
Output voltage						
		V_{CC} = 4.75V				
V_{OL}	Low[4]	I_{OL} = 9.6mA			0.5	V
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
Input current						
		V_{CC} = 5.25V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			50	µA
Output current						
		V_{CC} = 5.25V				
I_{OZ}	Hi-Z state	$\overline{ME}$ = High, V_O = 5.5V			60	µA
		$\overline{ME}$ = High, V_O = 0.5V			-100	µA
I_{OS}	Short circuit[3, 6, 13]	SC = WC, $\overline{ME}$ = Low				
		V_{CC} = 5.25V, V_O = 0V, High stored	-15		-85	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			200	mA
Capacitance[13]						
		$\overline{ME}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

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TRUTH TABLE

MODE	$\overline{ME}$	SC	WC	MCLK	BUSSED DATA/ ADDRESS LINES
Hold address Disable data out	1	X	X	X	Hi-Z data out
Input new address	0	1	0	1	Address Hi-Z
Hold address Disable data out	0	1	0	0	Hi-Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	Hi-Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state[12]	0	1	1	1	
Hold address[12] Disable data out	0	1	1	0	Hi-Z data out

X = Don't care

AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.75V \le V_{CC} \le 5.25V$[2]

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
t_{E1} t_{E2}	Output enable time Output enable time	Data out Data out	SC- $\overline{ME}$-			40 40	ns ns
t_{D1} t_{D2}	Output disable time Output disable time	Data out Data out	SC+ $\overline{ME}$+			40 40	ns ns
t_W	Master clock pulse width[8]			50			ns
t_{SA} t_{HA}	Setup time Hold time	MCLK- Address	Address MCLK-	40 10			ns ns
t_{SD} t_{HD}	Setup time Hold time	MCLK- Data in	Data in MCLK-	45 10			ns ns
t_{S3} t_{H3}	Setup time Hold time	MCLK- $\overline{ME}$+	$\overline{ME}$- MCLK-	50 5			ns ns
t_{S1} t_{H2}	Setup time Hold time	MCLK- $\overline{ME}$-	$\overline{ME}$- MCLK-	40 5			ns ns
t_{S2} t_{H1} t_{H4}	Setup time Hold time Hold time	$\overline{ME}$- SC- WC-	SC-, WC- MCLK- MCLK-	5 5 5			ns ns ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
3. Test each pin one at a time.
4. Measured with a logic Low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with a logic High stored.
6. Duration of the short circuit should not exceed 1 second.
7. I_{CC} is measured with the Write enable and Memory enable inputs grounded, all other inputs ≥ 4.0V and the output open.
8. Minimum required to guarantee a Write into the slowest bit.
9. Applied to the 8X305 based system with the data and address pins tied to the IV Bus.
10. SC + ME = 1 to avoid bus conflict.
11. WC + ME = 1 to avoid bus conflict.
12. The SC and WC outputs from the 8X305 are never at 1 simultaneously.
13. Guaranteed, but not tested.

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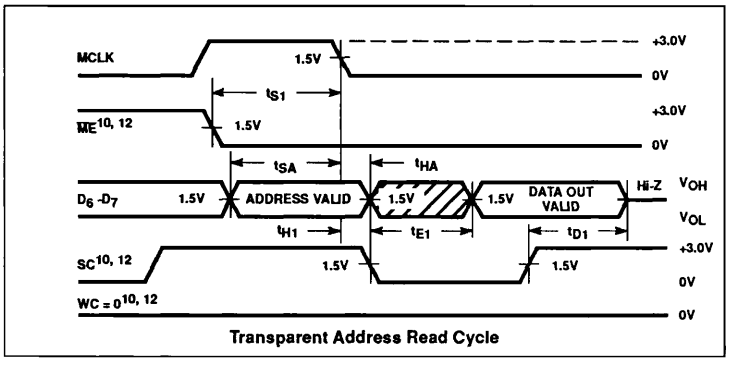
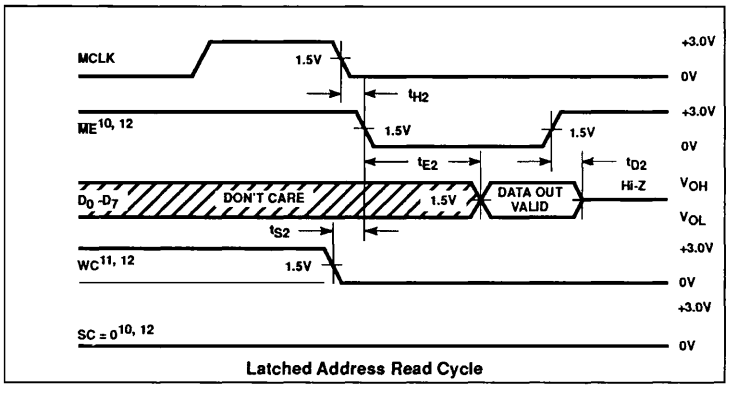
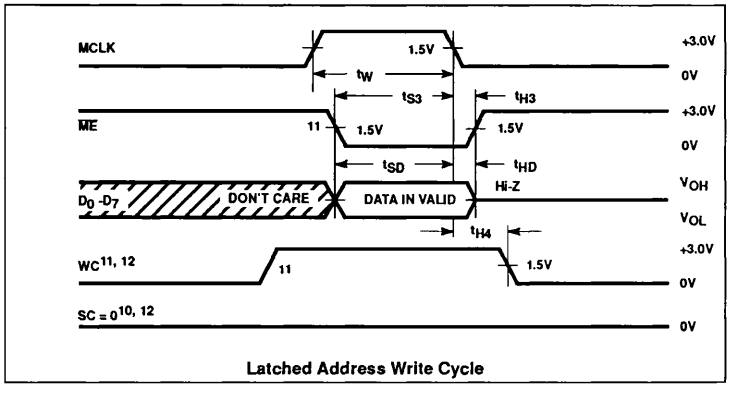
TIMING DIAGRAM



Transparent Address Read Cycle



Latched Address Read Cycle



Latched Address Write Cycle

MEMORY TIMING DEFINITIONS

t_{S1}	Required delay between beginning of Master Enable Low and falling edge of Master Clock.
t_{SA}	Required delay between beginning of valid address and falling edge of Master Clock.
t_{E1}	Delay between beginning of Select Command Low and beginning of valid data output on the IV Bus.
t_{E2}	Delay between when Master Enable becomes Low and beginning of valid data output on the IV Bus.
t_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
t_{D1}	Delay between when Select Command becomes High and end of valid data output on the IV Bus.
t_{D2}	Delay between when Master Enable becomes High and end of valid data output on the IV Bus.
t_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes Low.
t_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes Low.
t_{S2}	Required delay between when Select Command or Write Command becomes Low and when Master Enable becomes Low.
t_W	Minimum width of the Master Clock pulse.
t_{SD}	Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
t_{S3}	Required delay between when Master Enable becomes Low and falling edge of Master Clock.
t_{HD}	Required delay between beginning of valid data input on the IV Bus.
t_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes High.
t_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes Low.

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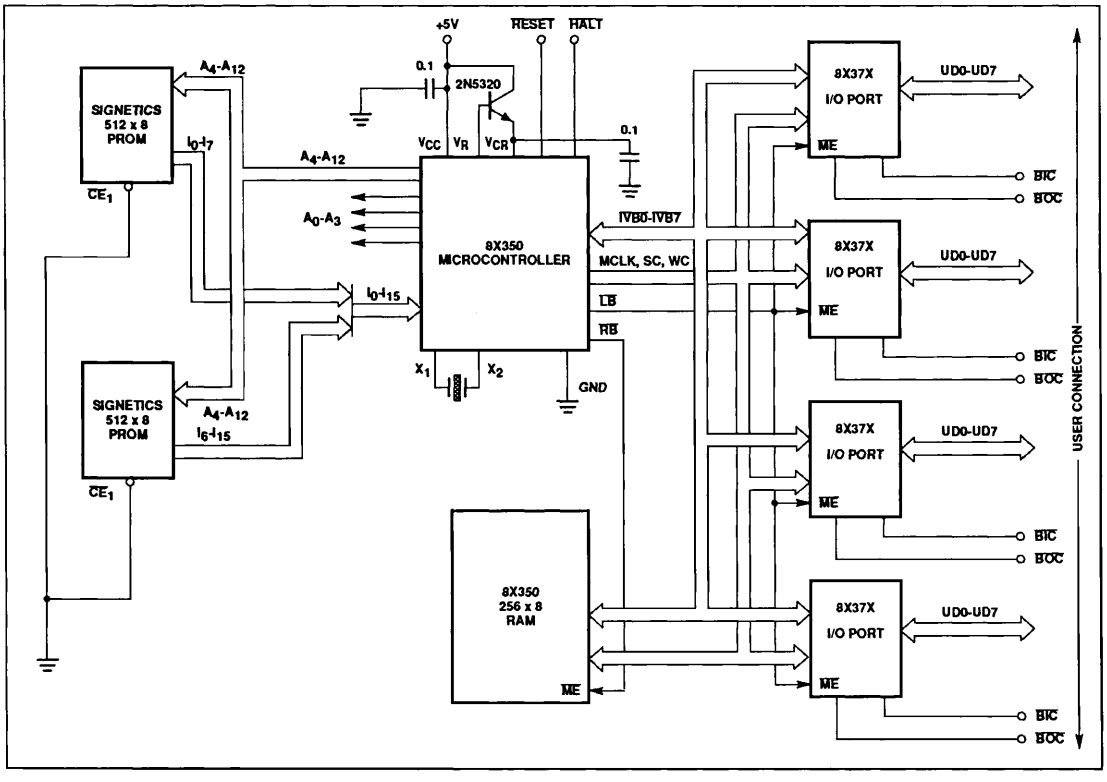
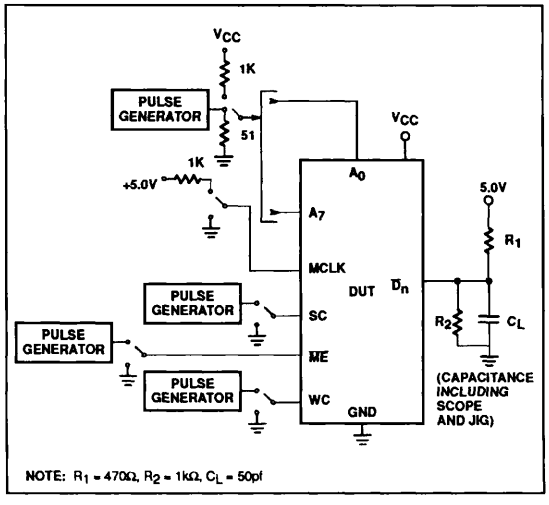
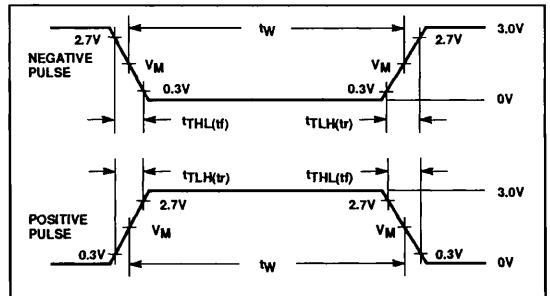
TYPICAL 8X350 APPLICATION



TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns