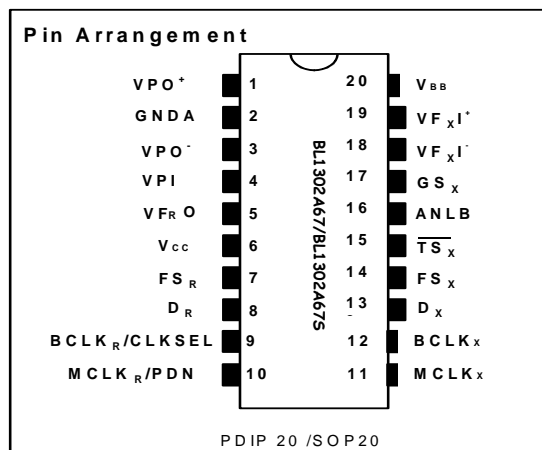


General Description

The BL1302A67/S is an A-law monolithic PCM CODEC/filter which has the A/D and D/A conversion and a serial PCM interface. The device is fabricated using the advanced double-poly nwell CMOS process. It is pin compatible with TP3067.

The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law PCM format. The decode portion consists of an expanding decoder, which reconstructs the analog signal from the companded A-law code, a low-pass filter which corrects for the $\sin x/x$ response of the decoder output and rejects signals above 3400 Hz followed by a single-ended amplifier and two power amplifiers to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to $\pm 6.6V$ across a balanced 600-ohm load. The device requires two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 KHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.



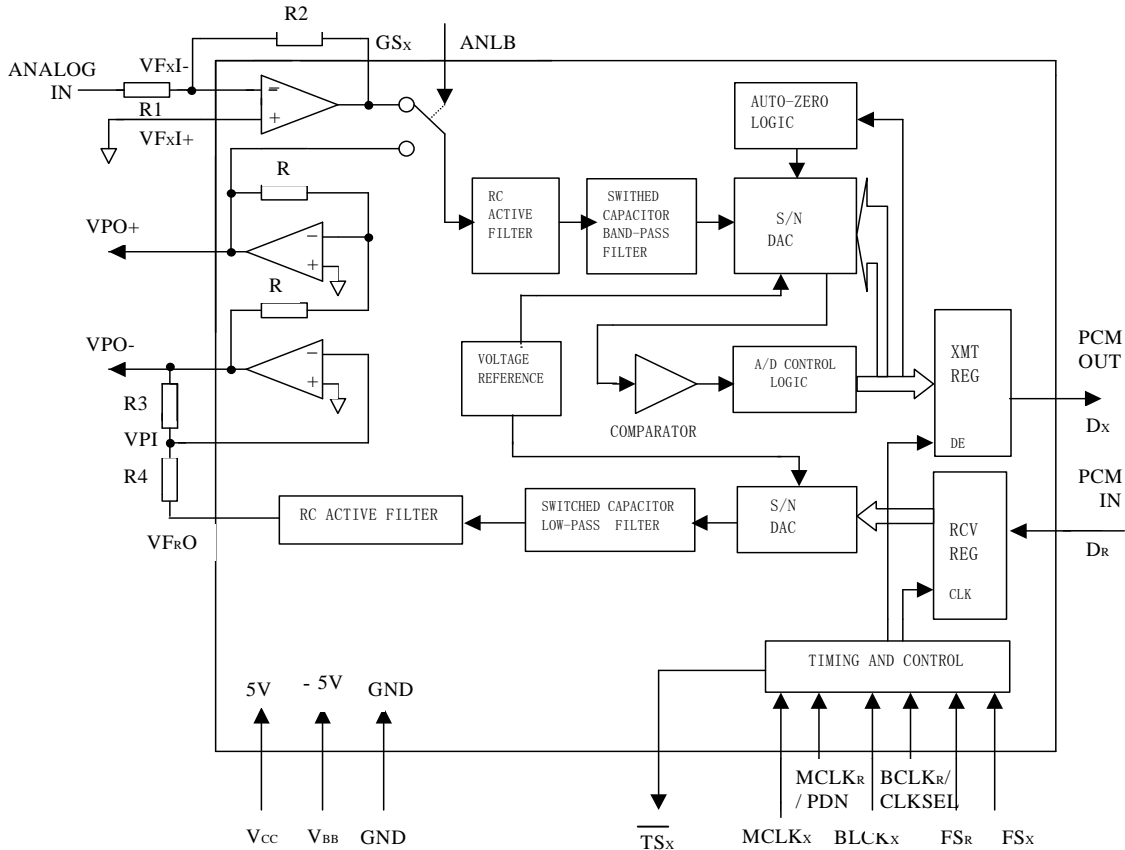
Features

- Complete CODEC and filtering system (COMBO) including:
 - Transmit high-pass and low-pass filtering
 - Receive low-pass filter with $\sin x/x$ correction
 - Active RC noise filters
 - A-law compatible COder and DECoder
 - Internal precision voltage reference
 - Serial I/O interface
 - Internal auto-zero circuitry
 - Receive push-pull power amplifiers
- 20 pin DIP or SOP
- Designed for ITU application
- $\pm 5V$ operation
- Low power: Typical 60mW

Stand-by 3mW

- Automatic power-down
- TTL or CMOS compatible digital interfaces

Block Diagram



Pin Description

Symbol	Function
VPO ⁺	The non-inverted output of the receive power amplifier.
GND _A	Analog ground. All signals are referenced to this pin.
VPO ⁻	The inverted output of the receive power amplifier.

VPI	Inverting input to the receive power amplifier.
VF _{RO}	Analog output of the receive power amplifier.
V _{CC}	Positive power supply pin. V _{CC} = +5V ± 5%
FS _R	Receive frame sync pulse which enables BCLK _R to shift PCM data into D _R . FS _R is an 8kHz pulse train.
D _R	Receive data input. PCM data is shifted into D _R following the FS _R leading edge.
BLCLK _R /CLKSEL	The bit clock which shifts data into D _R after the FS _R leading edge. May vary from 64kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and BCLK _x is used for both transmit and receive directions(see Table 1).
MCLK _R /PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. In synchronous mode, it may be needed as a power-down control. When MCLK _R is connected continuously low, MCLK _x is selected for all internal timing. When MCLK _R is connected continuously high, the device is powered down.
MCLK _x	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. In synchronous mode, it is also used as receive master clock.
BCLK _x	The bit clock which shifts out the PCM data on D _x . May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK _x .
D _x	The TRI-STATE PCM data output which is enabled by FS _x .
FS _x	Transmit frame sync pulse input which enables BCLK _x to shift out the PCM data on D _x . FS _x is an 8 KHz pulse train.
TS _x	Open drain output which pulses low during the encoder time slot.
ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO ⁺ output of the receive power amplifier.
GS _x	Analog output of the transmit input amplifier. Used to externally set gain.
VF _x I-	Inverting input of the transmit input amplifier.
VF _x I+	Non-inverting input of the transmit input amplifier.
V _{BB}	Negative power supply pin. V _{BB} = - 5V ± 5%

Functional Description

- **Power-up**

When power is first applied, the internal power-on reset circuitry initializes the device and places it into a power-down state. Most of the analog and digital circuits are deactivated, and the D_x and VF_{RO} outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the MCLK_R/PDN pin and FS_x and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the MCLK_R/PDN pin high; the alternative is to hold both FS_x and FS_R input continuously low---the device will power-down approximately 2 ms after the last FS_x or FS_R pulse. Power-up will occur on the first FS_x or FS_R pulse. The TRI-STATE PCM data output, D_x, will remain in the high impedance state until the second FS_x pulse.

- **Synchronous operation**

For synchronous operation, the same master clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to MCLK_x and the MCLK_R/PDN pin can be used as a

power-down control. A low level on MCLK_R/PDN powers up the device and a high level powers down the device. In either case, MCLK_X will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to BCLK_X and the BCLK_R/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544MHz or 2.048MHz. For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the BCLK_R/CLKSEL pin, BCLK_X will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of BCLK_R/CLKSEL . In this synchronous mode, the bit clock, BCLK_X and BCLK_R, may be from 64kHz to 2.048 MHz. The frequency of BCLK_X and BCLK_R are not necessary to be equal, but must be synchronous with MCLK_X.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled Dx output on the positive edge of BCLK_X. After 8 bit clock periods, the TRI-STATE Dx output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of BCLK_X (or BCLK_R if running). FS_X and FS_R must be synchronous with MCLK_{X/R} .

Table Selection of Master Clock Frequencies

BCLK _R /CLKSEL	Master Clock Frequency Selected
Clocked	2.048MHz
0	1.536MHz or 1.544MHz
1	2.048MHz

- **Short frame operation**

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, frame sync pulse, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in Figure 1. With FS_X high during a falling edge of BCLK_X, the next rising edge of BCLK_X enables the Dx TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the Dx output. With FS_R high during a falling edge of BCLK_R (BCLK_X, if BCLK_R is a fixed level), the next falling edge of BCLK_R latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

- **Long frame operation**

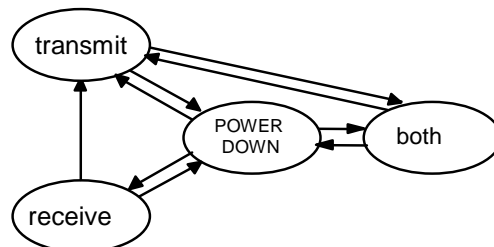
To use the long frame mode, the frame sync pulse, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in Figure 2. Based on the transmit frame sync, FS_X, the device will sense whether short or long frame sync pulse are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160ns. The Dx tri-state output buffer is enabled with the rising edge of FS_X or the rising edge of BCLK_X, whichever comes later, and the first bit clocked out is the sign bit. The following seven BCLK_X rising edges clock out the remaining seven bits. The Dx output is disabled by the falling BCLK_X edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of BCLK_R (BCLK_X if BCLK_R is a fixed level).

- **Single channel operation**

Keeping FS_R input continuously low, the device enters into transmit channel operation, the data at D_R input will be ignored. Keeping FS_X input continuously low, the device enters into receive channel operation. The most part of transmit circuitry ceases to work, D_X and TS_X output will be in high impedance. If $MCLK_R$ input is a clock, it is the internal master clock. If $MCLK_R$ input is not a clock, $MCLK_X$ is the internal master clock, and $MCLK_X$ must be synchronous with FS_R . If $BCLK_R$ input is not a clock, $BCLK_X$ is the internal bit clock. In receive channel operation, the length of FS_R determines whether it is short or long frame.

- **Switch of operation**

See picture below, it is not recommended that the switching from both channels to receive only or switching from receive channel only to transmit channel only.



- **Transmit section**

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law coding conventions. A built-in bandgap voltage reference is used to provide an input overload of nominally 2.492V peak. The FS_X frame pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165us (due to transmit filter) plus 125us (due to encoding delay), which totals 290us. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

- **Receive section**

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law and the 5th order low pass filter corrects for the $\sin x/x$ attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600ohm load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R , the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins. The total decoder delay approximately 280 us.

- **Receive power amplifiers**

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the $\pm 2.5V$ peak output signal from the receive filter up to $\pm 3.3V$ peak into an unbalanced 300 Ω load, or $\pm 4.0V$ into an unbalanced 15 k Ω

load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Electrical parameters and timing

Absolute Maximum Ratings

Rating	Value	Unit
V _{CC} to GNDA	7	V
V _{BB} to GNDA	-7	V
Voltage at any Analog Input or Output	V _{CC} +0.3 to V _{BB} -0.3	V
Voltage at any Digital Input or Output	V _{CC} +0.3 to GNDA-0.3	°C
Operating Temperature Range	-25 to +125	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10sec.)	300	°C
ESD (Human Body Model)	2000	V
Latch-Up Immunity at any Pins	100	mA

Electrical Characteristics: V_{CC} = +5.0V±5%, V_{BB} = -5.0V±5%, T_A = 0°C to +70°C. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = -5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital INTERFACE						
V _{IL}	Input Low Voltage				0.6	V
V _{IH}	Input High Voltage		2.2			V
V _{OL}	Output Low Voltage	Dx, I _L =3.2mA			0.4	V
		TSx, I _L =3.2mA, Open Drain			0.4	V
V _{OH}	Output High Voltage	Dx, I _H = - 3.2mA	2.4			V
I _{IL}	Input Low Current	GNDA≤V _{IN} ≤V _{IL} , All digital inputs	-10		10	μA
I _{IH}	Input High Current	V _{IH} ≤V _{IN} ≤V _{CC}	-10		10	μA
IOZ	Output Current in High Impedance State (TRI-STATE)	Dx, GNDA≤V _O ≤V _{CC}	-10		10	μA

Analog Interface with transmit input amplifier

I _I XA	Input Leakage Current	-2.5V≤V≤+2.5V, VFxI+ or VFxI-	-200		200	nA
R _I XA	Input Resistance	-2.5V≤V≤+2.5V, VFxI+ or VFxI-	10			MΩ
R _O XA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R _L XA	Load Resistance	GSx	10			kΩ
C _L XA	Load Capacitance	GSx			50	pF
V _O XA	Output Dynamic Range	GSx, R _L ≥10kΩ	-2.8		2.8	V
A _V XA	Voltage Gain	VFxI+ to GSx	5000			V/V
F _U XA	Unity Gain Bandwidth		1	2		MHz
V _{OS} XA	Offset Voltage		-20		20	mV
V _{CM} XA	Common-Mode Voltage	CMRRXA>60dB	-2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	60			dB

PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
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ANALOG INTERFACE WITH RECEIVE FILTER

$R_{O}RF$	Output Resistance	Pin $V_{F_R O}$		1	3	Ω
$R_{L}RF$	Load Resistance	$V_{F_R O} = \pm 2.5V$	10			k Ω
$C_{L}RF$	Load Capacitance				25	pF
VOS_{RO}	Output DC Offset Voltage		-200		200	mV

ANALOG INTERFACE WITH POWER AMPLIFIERS

IPI	Input Leakage Current	$-1.0V \leq V_{PI} \leq 1.0V$	-100		100	nA
TIPI	Input Resistance	$-1.0V \leq V_{PI} \leq 1.0V$	10			M Ω
VIOS	Input Offset Voltage		-25		25	mV
ROP	Output Resistance	Inverting Unity-Gain at V_{PO}^+ or V_{PO}^-		1		Ω
F_C	Unity-Gain Bandwidth	Open Loop (V_{PO}^-)		400		kHz
C_{LP}	Load Capacitance				100	pF
GA_{P^+}	Gain from V_{PO}^- to V_{PO}^+	$R_L = 600\Omega$ V_{PO}^+ to V_{PO}^- Level at $V_{PO}^- = 1.77 V_{rms}$		-1		V/V
PSRR _p	Power Supply Rejection of V_{CC} or V_{BB}	V_{PO}^- connected to VPI 0 kHz —4 kHz 4 kHz —50 kHz	60 36			dB dB
R_{LP}	Load Resistance	Connect from V_{PO}^+ to V_{PO}^-	600			Ω

POWER DISSIPATION

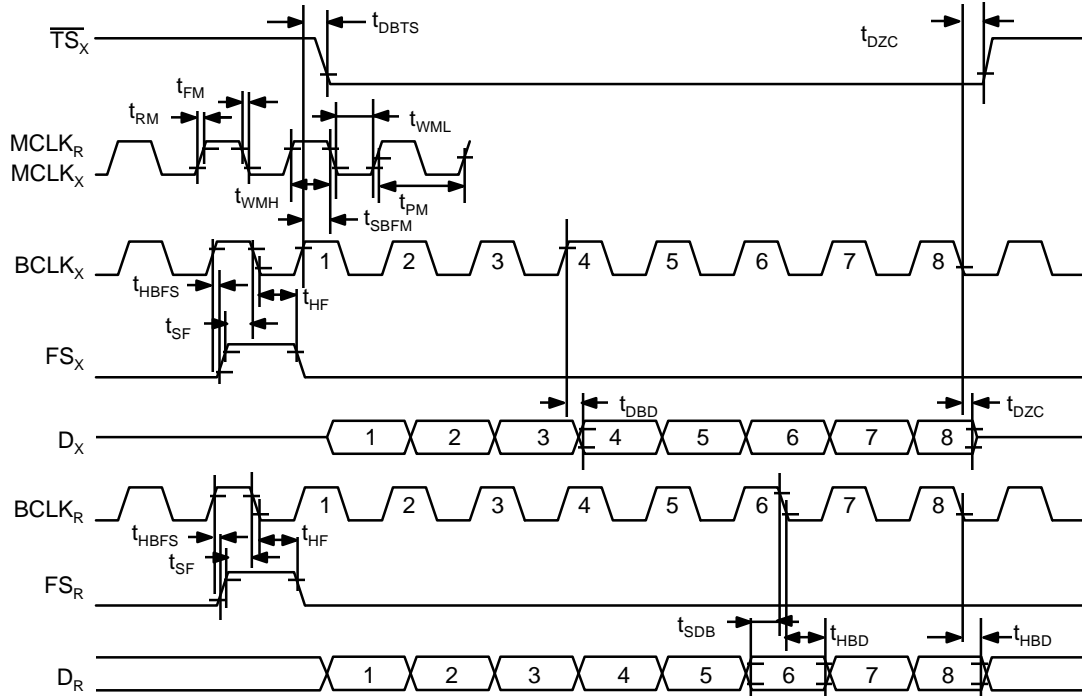
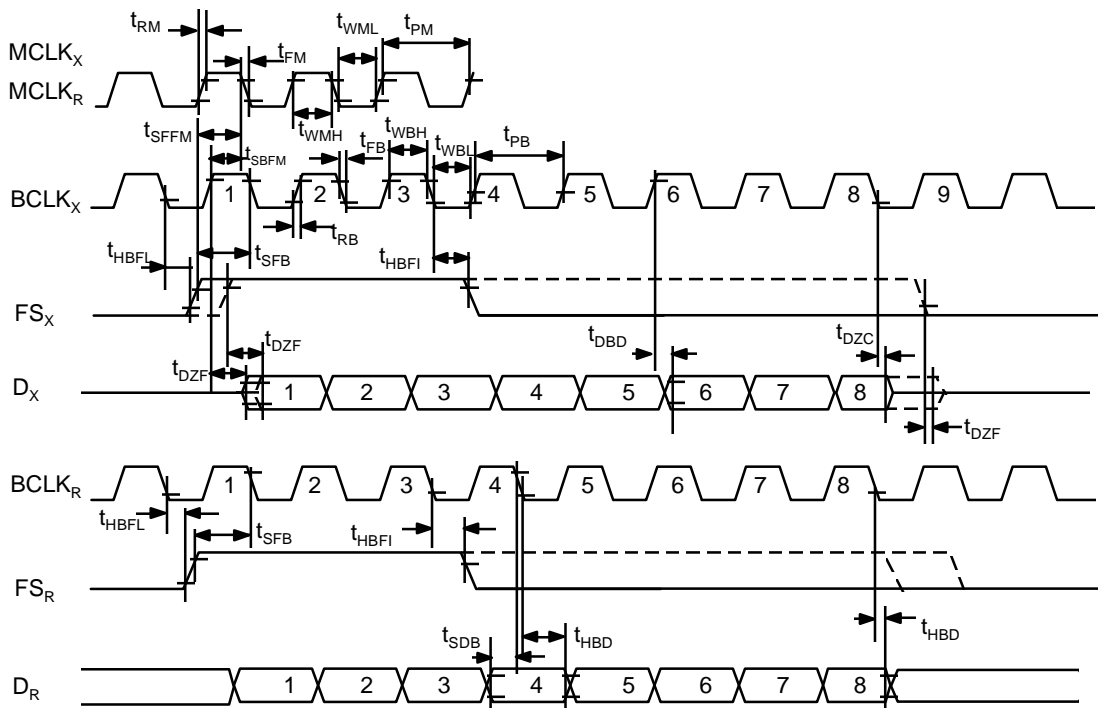
I_{CC0}	Power-Down Current	No Load (Note)		0.14	0.3	mA
I_{BB0}	Power-Down Current	No Load (Note)		0.20	1.5	mA
I_{CC1}	Power-Up Active Current	No Load		6.0	10	mA
I_{BB1}	Power-Up Active Current	No Load		6.0	10	mA

Note: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Timing Specifications: $V_{CC} = +5.0 \pm 5\%$, $V_{BB} = -5.0 \pm 5\%$, $T_a = 0^\circ C \sim +70^\circ C$. All signals referenced to GNDA. Typical specified at $V_{OH} = +5.0V$, $V_{BB} = -5.0V$, $T_H = 25^\circ C$. All timing parameters are assured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	Depends on $BCLK_R/CLKSEL$ Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock		485	488	15725	ns
t_{RB}	Rise Time of Bit Clock	$BCLK_X$ and $BCLK_R$			50	ns
t_{FB}	Fall Time of Bit Clock	$BCLK_X$ and $BCLK_R$			50	ns
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns

t _{SBFM}	Set-Up Time from BCLKx High to MCLKx Falling Edge	First Bit Clock after the Leading Edge of FSx	100			ns
t _{SFFM}	Set-up Time from FSx High to MCLKx Falling Edge	Long Frame Only	100			ns
t _{WBH}	Width of Bit Clock High	VIH=2.2V	160			ns
t _{WBL}	Width of Bit Clock Low	VIL=0.6V	160			ns
t _{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t _{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t _{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t _{DBD}	Delay Time from BCLKx High to Data Valid	Load=150 pF plus 2 LSTTL	0		140	ns
t _{DBTS}	Delay Time to TSx Low	Load=150 pF plus 2 LSTTL Loads			140	ns
t _{DZC}	Delay Time from BCLKx Low to Data Output Disabled	CL=0 pF to 150 pF	50		165	ns
t _{DZF}	Delay Time to Valid Data from FSx or BCLKx, Whichever Comes Later	CL=0 pF to 150 pF	20		165	ns
t _{SDB}	Set-Up time from D _R Valid to BCLK _{R/X} Low		50			ns
t _{HBD}	Hold Time from BCLK _{R/X} Low to D _R Invalid		50			ns
t _{SF}	Set-Up Time from FS _{X/R} to BCLK _{X/R} Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	50			ns
t _{HF}	Hold Time from BCLK _{X/R} Low to FS _{X/R} Low	Short Frame Sync Pulse (1 bit Clock Period Long)	100			ns
t _{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FSx or FS _R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t _{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64K Bit/s Operating Mode	160			ns

Timing diagrams
Figure 1. Short Frame Sync Timing

Figure 2. Long Frame Sync Timing


Transmission Characteristics: $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, $G_{NDA} = 0V$, $T_A = 0^\circ C$ to $+70^\circ C$, $f = 1.02kHz$, $V_{in} = 0dBm_0$, transmit input amplifier connected for unity gain inverting. Typical values are specified at $V_{CC} = +5V$, $V_{BB} = -5.0V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Amplitude response						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm ₀ Level is 4 dBm(600Ω) 0 dBm ₀		1.2276		V _{rms}
t _{MAX}	Virtual Decision Valve Defined Per CCITT Rec. G711	Max Overload Level (3.14 dBm ₀)		2.492		V _{PK}
G _{XA}	Transmit Gain, Absolute	T _A =25 °C, V _{CC} =5V, V _{BB} = -5V Input at G _{SX} =0 dBm ₀ at 1020 Hz	-0.25		0.25	dB
G _{XR}	Transmit Gain, Relative to G _{XA}	f=16Hz f=50Hz f=60Hz f=200Hz f=300Hz-3000Hz f=3300Hz f=3400Hz f=4000Hz f=4600Hz and Up, Measure Response from 0 Hz to 4000 Hz	-1.8 -0.15 -0.35 -0.7		-40 -30 -26 -0.1 0.15 0.05 0 -14 -32	dB
G _{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G _{XA}	-0.1		0.1	dB
G _{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G _{XA}	-0.05		0.05	dB
G _{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level=-10dBm ₀ VFxI+/-40dBm ₀ to +3dBm ₀ VFxI+/-50dBm ₀ to -40dBm ₀ VFxI+/-55dBm ₀ to -50dBm ₀	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB
G _{RA}	Receive Gain, Absolute	T _A =25 °C, V _{CC} =5V, V _{BB} =-5V Input=Digital Code Sequence for 0 dBm ₀ Signal at 1020 Hz	-0.25		0.25	dB
G _{RR}	Receive Gain, Relative to G _{RA}	f=0Hz to 3000 Hz f=3300Hz f=3400Hz f=4000Hz	-0.15 -0.35 -0.7		0.15 0.05 0 -14	dB
G _{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G _{RA}	-0.1		0.1	dB
G _{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G _{RA}	-0.05		0.05	dB

G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level =-40 dBm0 to +3 dBm0 =-50 dBm0 to -40 dBm0 =-55 dBm0 to -50 dBm0	-0.2 -0.4 -1.2	0.2 0.4 1.2	dB dB dB	
V_{RO}	Receive Output Drive Level	$R_L=10\text{ k}\Omega$	-2.5	2.5	V	
<h2>Envelope delay distortion with frequency</h2>						
D_{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	us
D_{XR}	Transmit Delay, Relative to D_{XA}	f=500 Hz - 600 Hz f=600 Hz - 800 Hz f=800 Hz - 1000 Hz f=1000 Hz - 1600 Hz f=1600 Hz - 2600 Hz f=2600 Hz - 2800 Hz f=2800 Hz - 3000 Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	us us us us us us us
D_{RA}	Receive Delay, Absolute	f=1600 Hz		270	290	us
D_{RR}	Receive Delay, Relative to D_{RA}	f=500 Hz - 1000 Hz f=1000 Hz - 1600 Hz f=1600 Hz - 2600 Hz f=2600 Hz - 2800 Hz f=2800 Hz - 3000 Hz	-40 -30	-25 -20 70 100 145	90 125 175	us us us us us
<h2>Noise</h2>						
N_{XP}	Transmit Noise, P Message Weighted			-74	-67	dBm0p
N_{RP}	Receive Noise, P Message Weighted	PCM Code Equals Positive Zero		-82	-79	dBm0p
N_{RS}	Noise, Single Frequency	f=0kHz to 100 kHz, Loop Around Measurement, $V_{Fxi}=\pm 0\text{ Vrms}$			-53	dBm0
PPSRx	Positive Power Supply	$V_{Fxi}=\pm 50\text{ dBm0}$				

	Rejection, Transmit	V _{CC} =5.0 V _{DC} +100 mVrms f=0 kHz - 50 kHz (Note 2)	40			dBC
NPSR _X	Negative Power Supply Rejection, Transmit	V _{Fx1±} -50 dBm0 V _{CC} =-5.0 V _{DC} +100 mVrms f=0 kHz - 50 kHz (Note 2)	40			dBC
PPSR _R	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero, V _{CC} =5.0V _{DC} +100mVrms Measure V _{FRO}	40			dBC
		f=0 Hz - 4000 Hz	40			dB
		f=4 kHz - 25 kHz f=25 kHz - 50 kHz	36			dB
NPSR _R	Negative Power Supply Rejection, Receive	PCM code Equals Positive Zero, V _{BB} =-5.0V _{DC} +100mVrms Measure V _{FRO}	38			dBC
		f=0 Hz - 4000 Hz f=4 kHz - 50 kHz	25			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D _R . 4600 Hz - 7600 Hz 7600 Hz - 8400 Hz 8400 Hz - 100,000 Hz			-30 -40 -30	dB dB dB
<h1>Distortion</h1>						
STD _X STD _R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3) Level=3.0 dBm0 =0 dBm0 to -30 dBm0 =-40 dBm0 XMT RCV =-55 dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
SFD _X	Single Frequency Distortion, Transmit				-46	dB
SFD _R	Single frequency Distortion, Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, V _{Fx±} =-4dBm0 to -21 dBm0, Two Frequencies in the Range 300 Hz-3400Hz			-41	dB

Crosstalk

CT _{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f=300Hz-3400Hz D _R =Quiet PCM Code (Note 2)		-90	-75	dB
CT _{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f=300Hz-3400Hz, VF _{XI} =Multitone (Note1)		-90	-70	dB

Power Amplifiers

V _O PA	Maximum 0 dBm0 Level (Better than ± 0.1dB Linearity over the Range -10 dBm0 to + 3 dBm0)	Balanced Load, R _L connected Between VPO ⁺ and VPO ⁻ R _L = 600 Ω R _L = 1200 Ω		3.3 3.5		V _{rms} V _{rms}
S/D _p	Signal/Distortion	R _L = 600 Ω	50			dB

Note 1: Measured by extrapolation from the distortion test result at -50 dBm0.

Note 2: PPSRx, NPSRx, and CTR-X are measured with a -50 dBm0 activation signal applied to VF_{XI}+.

Note 3: Device is measured using psophometric weighted filter.

Encoding Format at Dx Output

V _{in} (at GS _x) = +Full-Scale	1 0 1 0 1 0 1 0
V _{in} (at GS _x) = 0V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V _{in} (at GS _x) = -Full-Scale	0 0 1 0 1 0 1 0

Applications Information

Power supplies

While the pins of the device are well protected against electrical misuse, it is recommended that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a “hot” socket with power and clocks already present, an extra long ground pin in the connector should be used.

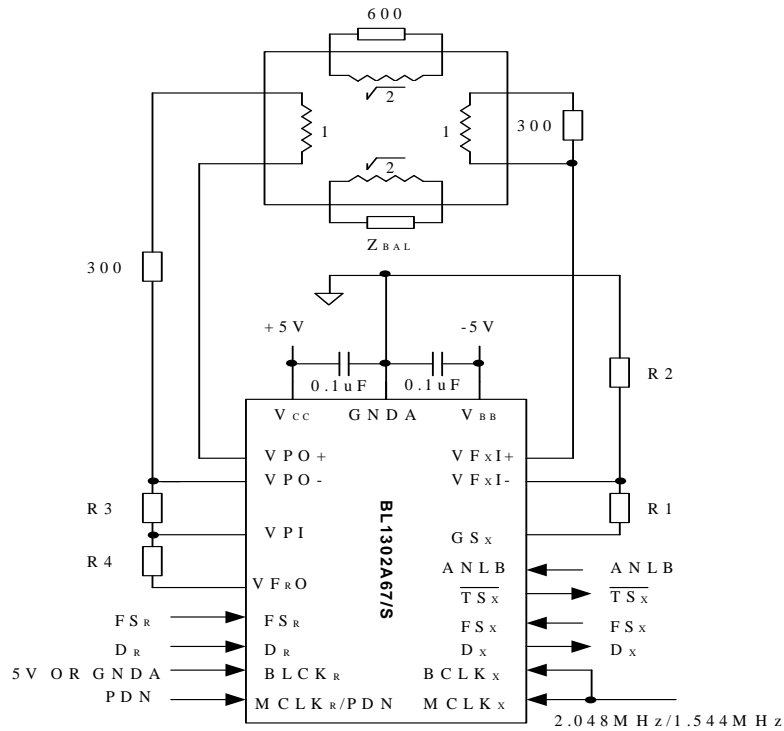
All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance.

0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} , as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with $10\mu\text{F}$ capacitors.

Typical synchronous application

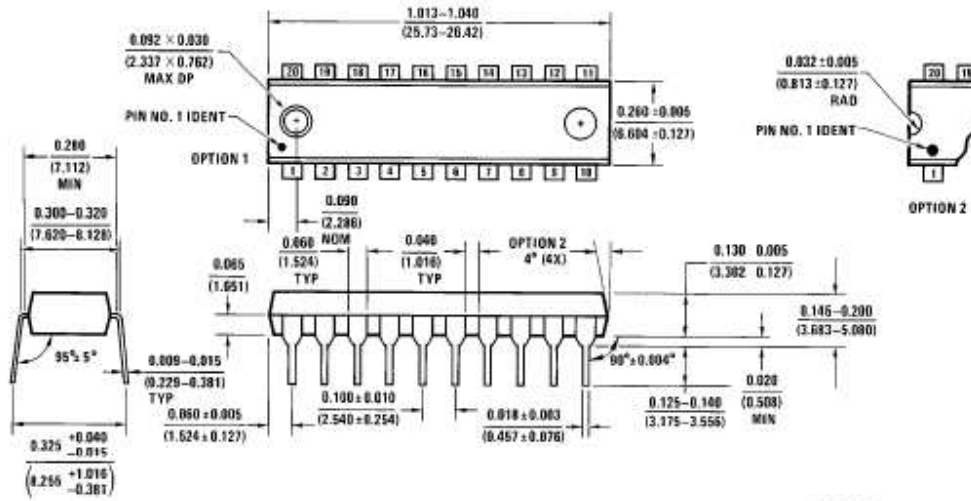


Note 1: Transmit gain = $20 \times \log\left(\frac{R1+R2}{R2}\right)$, $R1 + R2 \geq 10k\Omega$

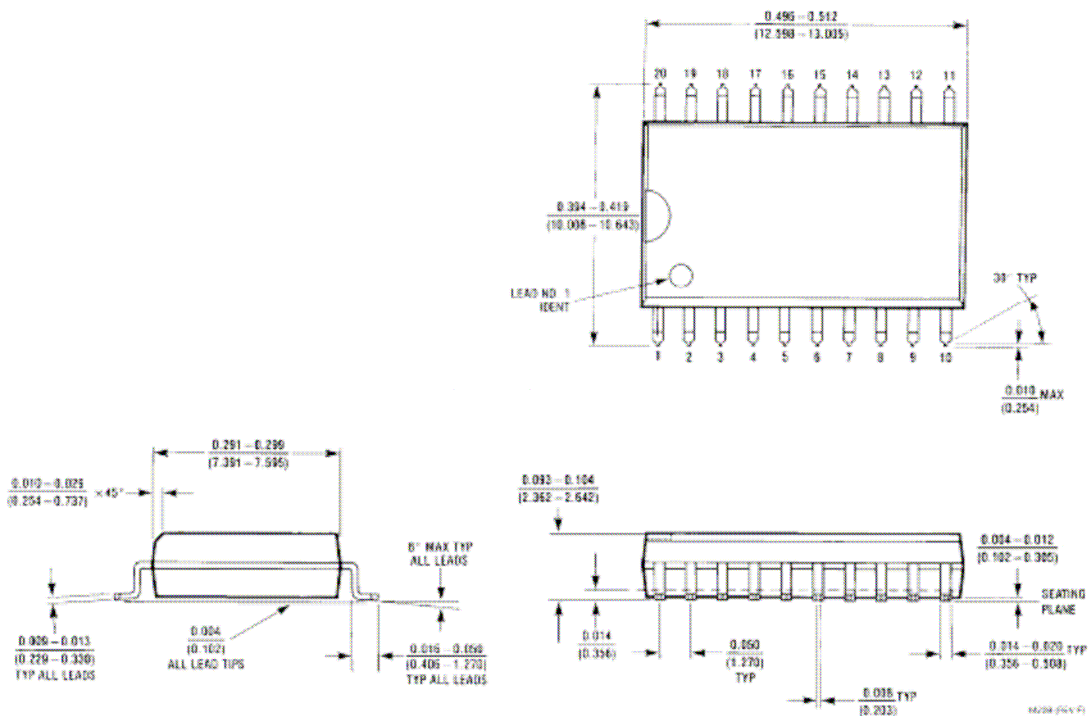
Note 2: Receive gain = $20 \times \log\left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10k\Omega$

Print Information

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)



Molded Small Outline Package (WM)