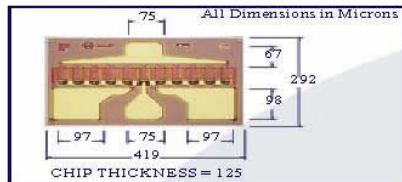


MwT-9

18 GHz High Power GaAs FET



DOWNLOAD ADDITIONAL DATA WWW.MWTINC.COM



FEATURES

- +26 dBm OUTPUT POWER AT 12 GHz
- 8.5 dB SMALL SIGNAL GAIN AT 12 GHz
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 750 MICRON GATE WIDTH
- CHOICE OF CHIP AND THREE PACKAGE TYPES

DESCRIPTION

The MwT-9 is a GaAs MESFET device whose nominal quarter-micron gate length and 750 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 18 GHz frequency range with power output ranging from +24 to +26 dBm. It can be easily matched as the driver stage in high power communications amplifiers or in broad-band military amplifiers and operated at reduced bias in battery powered wireless communications devices. The chip is produced using MwT's reliable metal system and devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

DC SPECIFICATIONS AT Ta = 25°C

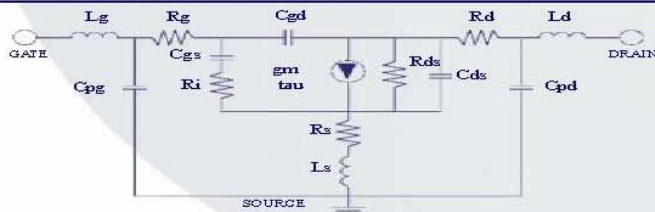
SYMBOL	PARAM. & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current Vds= 4.0 V VGS= 0.0 V	mA	78		282
Gm	Transconductance Vds= 2.0 V VGS= 0.0 V	mS	95	120	
Vp	Pinch-off Voltage Vds= 3.0 V IDS= 5.0 mA	V		-2.0	-5.0
BVGS0	Gate-to-Source Breakdown Volt. Igs= -1.0 mA	V	-6.0	-12.0	
BVGDO	Gate-to-Drain Breakdown Volt. Igd= -1.0 mA	V	-8.0	-12.0	
Rth	Thermal Resistance MwT-9 Chip, 971 MwT-970, 973	°C/W		70	175*

*Overall Rth depends on case mounting.

RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1 dB Compression VDS= 6.0 V IDS= 180mA	12 GHz	dBm	25.0	26.0
PAE	Power Added Efficiency VDS= 6.0 V IDS= 180mA	12 GHz	%	30	35
SSG	Small Signal Gain VDS= 6.0 V IDS= 180mA	12 GHz	dB	8	8.5
IDSS	Recommended IDSS Range for Optimum P1dB		mA		198-270

DEVICE EQUIVALENT CIRCUIT MODEL



PARAMETER

VALUE

Source Resistance	R _s	0.2	Ω
Source Inductance	L _s	0.055	nH
Drain-Source Resistance	R _{ds}	300.0	Ω
Drain-Source Capacitance	C _{ds}	0.05	pF
Drain Resistance	R _d	1.02	Ω
Drain Pad Capacitance	C _{pd}	0.05	pF
Drain Inductance	L _d	0.23	nH
Gate Bond Wire Inductance	L _g	0.15	nH
Gate Pad Capacitance	C _{pg}	0.07	pF
Gate Resistance	R _g	0.50	Ω
Gate-Source Capacitance	C _{gs}	0.85	pF
Channel Resistance	R _i	1.0	Ω
Gate-Drain Capacitance	C _{gd}	0.08	pF
Transconductance	gm	95.0	mS
Transit Time	tau	2.6	psec

ORDERING INFORMATION

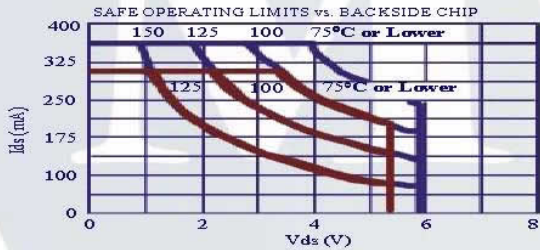
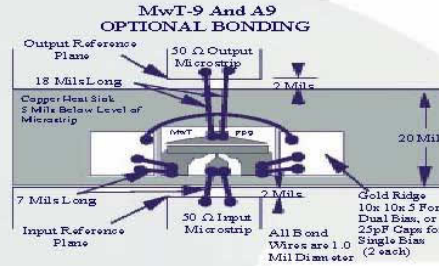
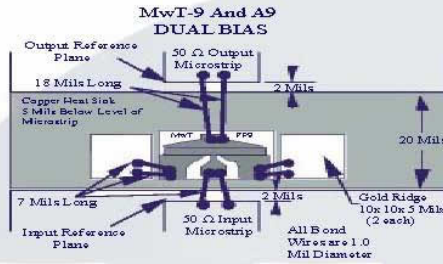
Chip	MwT-9
Package 70	MwT-970
Package 71	MwT-971
Package 73	MwT-973

NOTE:

For Package information, please see supplementary application note from our website at www.mwtinc.com. When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

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Legend: Absolute Maximum (blue line), Continuous Maximum (red line)

MAXIMUM RATINGS AT Ta = 25°C

SYMBOL	PARAMETER	UNITS	CONT MAX*	ABSOLUTE MAX*
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	R.F. Input Power	mW	300	450

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean time-to-failure below the design goals.
 2. Exceeding any one of these limits may cause permanent damage.

TYPICAL NOISE PARAMETERS

MwT-9LN Chip; VDS= 3.0V IDS= 35mA

FREQUENCY GHz	NF MIN dB	GAMMA OPT		Rn/50
		MAG	ANGLE	
2.00	0.326	0.838	19.11	0.48
4.00	0.6	0.726	38.47	0.41
6.00	0.858	0.623	58.31	0.38
10.00	1.33	0.51	98.59	0.33
12.00	1.55	0.493	117.7	0.313
16.00	1.96	0.508	130.4	0.286

Bin Selection Guide

Bin No.	A	B	C	D	E
Idss Range	78-114mA	114-150mA	150-198mA	198-234mA	234-294mA

BIN ACCURACY STATEMENT

When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.