

- 35-ns and 50-ns Single-Cycle Instruction Execution Time for 5 V Operation
- 50-ns Single-Cycle Instruction Execution Time for 3.3 V Operation
- Source-Code Compatible With All 'C1x and 'C2x Devices
- RAM-Based Operation
 - 9K-Words $\times$ 16-Bit Single-Access On-Chip Program/Data RAM
 - 1056-Word $\times$ 16-Bit Dual-Access On-Chip Data RAM
- 2K-Word $\times$ 16-Bit On-Chip Boot ROM
- 224K-Word $\times$ 16-Bit Maximum Addressable External Memory Space (64K-Word Program, 64K-Word Data, 64K-Word I/O, and 32K-Word Global)
- 32-Bit Arithmetic Logic Unit (ALU)
 - 32-Bit Accumulator (ACC)
 - 32-Bit Accumulator Buffer (ACCB)
- 16-Bit Parallel Logic Unit (PLU)
- 16 $\times$ 16-Bit Multiplier, 32-Bit Product
- Eleven Context Switch Registers
- Two Buffers for Circular Addressing
- Full-Duplex Synchronous Serial Port
- Time-Division Multiplexed Serial Port (TDM)
- Timer With Control and Counter Registers
- 16 Software Programmable Wait-State Generators
- Divide-By-1 Clock Option
- IEEE Standard 1149.1[†] Test Access Port
- Operations are Fully Static
- Fabricated Using the Texas Instruments Enhanced Performance Implanted CMOS (EPIC[™]) 0.72- μ m Technology

description

The TMP320C50KGD digital signal processor (DSP) is a high performance, 16-bit, fixed-point processor manufactured in 0.72- μ m double-level metal CMOS technology. The TMP320LC50KGD has the same functionality as the 'C50KGD except for operation at 3.3 V instead of 5 V.

Texas Instruments Military Products currently employs three primary processes for the development of a known good die (KGD), one of which is applied to the TMP320C50 and TMP320LC50 devices. This process, known as hot-chuck-probe, uses a standard probed product that is tested again, this time at full data sheet specifications, in wafer form at speed and elevated temperature (85°C). Each individual die then is sawed, inspected, and packed for shipment. This flow produces a bare die that has been temperature-tested at speed and is known to be good, without having to use a temporary package.

A number of enhancements to the basic 'C2x architecture give the 'C5x a minimum 2x performance over the previous generation. A four-deep instruction pipeline, incorporating delayed branching, delayed call to subroutine, and delayed return from subroutine, allows the 'C5x to perform instructions in fewer cycles. The addition of a PLU gives the 'C5x a method of manipulating bits in data memory without using the accumulator and ALU. The 'C5x has additional shifting and scaling capability for proper alignment of multiplicands or storage of values to data memory.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port and Boundary-Scan Architecture
EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description (continued)

With the addition of the IDLE2 instruction, the 'C5x achieves low-power consumption. IDLE2 removes the functional clock from the internal hardware of the 'C5x that puts it into a total-sleep mode using only 5 μ A. A low-logic level on an external interrupt with chip duration of at least five clock cycles ends the IDLE2 mode.

TMP Product Flow; 40 and 57 MHz

Multiprobe	dc test @ 25°C
Visual	40x
Test conditions	Per commercial data sheet
DC test	Hot chuck probe @ 85°C
AC test	Hot chuck probe @ 85°C @ Speed
Warranty	Datasheet upon shipment, 1 year

For electrical and timing specifications, see the *TMS320C5x, TMS320LC5x Digital Signal Processors* data sheet, literature number SPRS030.

Specific Die-Related Information

Die Size (approximate)	391 mils x 421 mils
Die Thickness	15.5 mils $\pm$ 1 mil
Backside Surface Finish	SiO ₂
Die Backside Potential	Floating
Max Allowable Die Junction Operating Temperature	175°C
Glassivation Material and Thickness	3KAOX/9KACN
Recommended Packing	GEL PAK
Die Attach Information	SILVER GLASS
Suggested Bond Wire Size	1.25 AL
Suggested Bonding Method	WEDGE
ESD Sensitivity	Class II
Max Allowable Process Temperature for Die Attach	450°C



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TMP320C50/LC50 Pad Information

	PAD	XCENTER	YCENTER	PAD NAME		PAD	XCENTER	YCENTER	PAD NAME
TOP	1	5347.4	9670.8	$\overline{\text{IAQ}}$	BOTTOM	41	106.3	1783.3	CLKR
	2	5161.8	9670.8	$\overline{\text{TRST}}$		42	106.3	1353.6	V _{DD5}
	3	4908.6	9670.8	V _{SS1}		43	106.3	1218.6	V _{DD6}
	4	4773.6	9670.8	V _{SS2}		44	1513.4	106.3	V _{SS7}
	5	4573.4	9670.8	MP/MC		45	1648.4	106.3	V _{SS8}
	6	4139.3	9670.8	D15		46	2128.3	106.3	A0
	7	3851.3	9670.8	D14		47	2403.3	106.3	A1
	8	3515.3	9670.8	D13		48	2637.3	106.3	A2
	9	3272.3	9670.8	D12		49	2912.2	106.3	A3
	10	3024.8	9670.8	D11		50	3132.7	106.3	A4
	11	2777.3	9670.8	D10		51	3407.7	106.3	A5
	12	2421.0	9670.8	D9		52	3628.2	106.3	A6
	13	2121.1	9670.8	D8		53	3903.1	106.3	A7
	14	1702.6	9670.8	V _{DD1}		54	4123.6	106.3	A8
LEFT	15	1567.6	9670.8	V _{DD2}	RIGHT	55	4398.6	106.3	A9
	16	106.3	8552.8	V _{SS3}		56	4569.6	106.3	V _{DD7}
	17	106.3	8417.8	V _{SS4}		57	4704.6	106.3	V _{DD8}
	18	106.3	7859.8	D7		58	4896.7	106.3	TDI
	19	106.3	7616.8	D6		59	5319.8	106.3	V _{SS9}
	20	106.3	7321.3	D5		60	5454.8	106.3	V _{SS10}
	21	106.3	7096.3	D4		61	5646.0	106.3	CLKMOD1
	22	106.3	6871.3	D3		62	5886.6	106.3	A10
	23	106.3	6646.3	D2		63	6161.6	106.3	A11
	24	106.3	6323.9	D1		64	6527.3	106.3	A12
	25	106.3	6098.9	D0		65	6802.3	106.3	A13
	26	106.3	5818.7	TMS		66	7036.3	106.3	A14
	27	106.3	5498.0	V _{DD3}		67	7311.2	106.3	A15
	28	106.3	5363.0	V _{DD4}		68	8202.2	106.3	V _{DD9}
	29	106.3	4942.2	TCK		69	8337.2	106.3	V _{DD10}
	30	106.3	4764.3	NC		70	8649.0	106.3	$\overline{\text{RD}}$
	31	106.3	4601.2	V _{SS5}		71	9195.5	106.3	$\overline{\text{WE}}$
	32	106.3	4466.2	V _{SS6}		72	10274.3	1253.8	V _{SS11}
	33	106.3	4041.0	$\overline{\text{INT1}}$		73	10274.3	1388.8	V _{SS12}
	34	106.3	3789.2	$\overline{\text{INT2}}$		74	10274.3	1902.2	$\overline{\text{DS}}$
	35	106.3	3537.4	$\overline{\text{INT3}}$		75	10274.3	2236.6	$\overline{\text{IS}}$
	36	106.3	3201.4	$\overline{\text{INT4}}$		76	10274.3	2524.8	$\overline{\text{PS}}$
	37	106.3	2949.6	$\overline{\text{NMI}}$		77	10274.3	2882.6	$\overline{\text{RW}}$
	38	106.3	2697.8	$\overline{\text{DR}}$		78	10274.3	3168.8	$\overline{\text{STRB}}$
	39	106.3	2445.9	$\overline{\text{TDR}}$		79	10274.3	3365.0	$\overline{\text{BR}}$
	40	106.3	2035.1	FSR		80	10274.3	3625.7	NC



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TMP320C50/LC50 Pad Information (Continued)

PAD	XCENTER	YCENTER	PAD NAME
81	10274.3	3795.5	CLKIN2
82	10274.3	3950.6	X2/CLKIN
83	10274.3	4126.6	X1
84	10274.3	4296.2	NC
85	10274.3	4459.4	VDD11
86	10274.3	4594.4	VDD12
87	10274.3	4766.7	TDO
88	10274.3	5085.1	VSS13
89	10274.3	5220.1	VSS14
90	10274.3	5375.3	CLKMD2
91	10274.3	5579.4	FSX
92	10274.3	5866.1	TFSX/TFRM
93	10274.3	6086.8	DX
94	10274.3	6379.1	TDX
95	10274.3	6599.8	HOLDA
96	10274.3	6820.5	XF
97	10274.3	7180.3	CLKOUT1
98	10274.3	7558.5	IACK
99	10274.3	8089.5	VDD13
100	10274.3	8224.5	VDD14
101	10274.3	8724.3	NC
102	10274.3	8859.3	NC
103	9201.4	9670.8	EMU0
104	8796.6	9670.8	EMU1/OFF
105	8540.1	9670.8	VSS15
106	8405.1	9670.8	VSS16
107	7927.9	9670.8	TOUT
108	7690.0	9670.8	TCLKX
109	7456.5	9670.8	CLKX
110	7133.8	9670.8	TFSR/TADD
111	6956.1	9670.8	TCLKR
112	6771.8	9670.8	RS
113	6587.5	9670.8	READY
114	6403.1	9670.8	HOLD
115	6016.9	9670.8	BIO
116	5780.7	9670.8	VDD15
117	5645.7	9670.8	VDD16

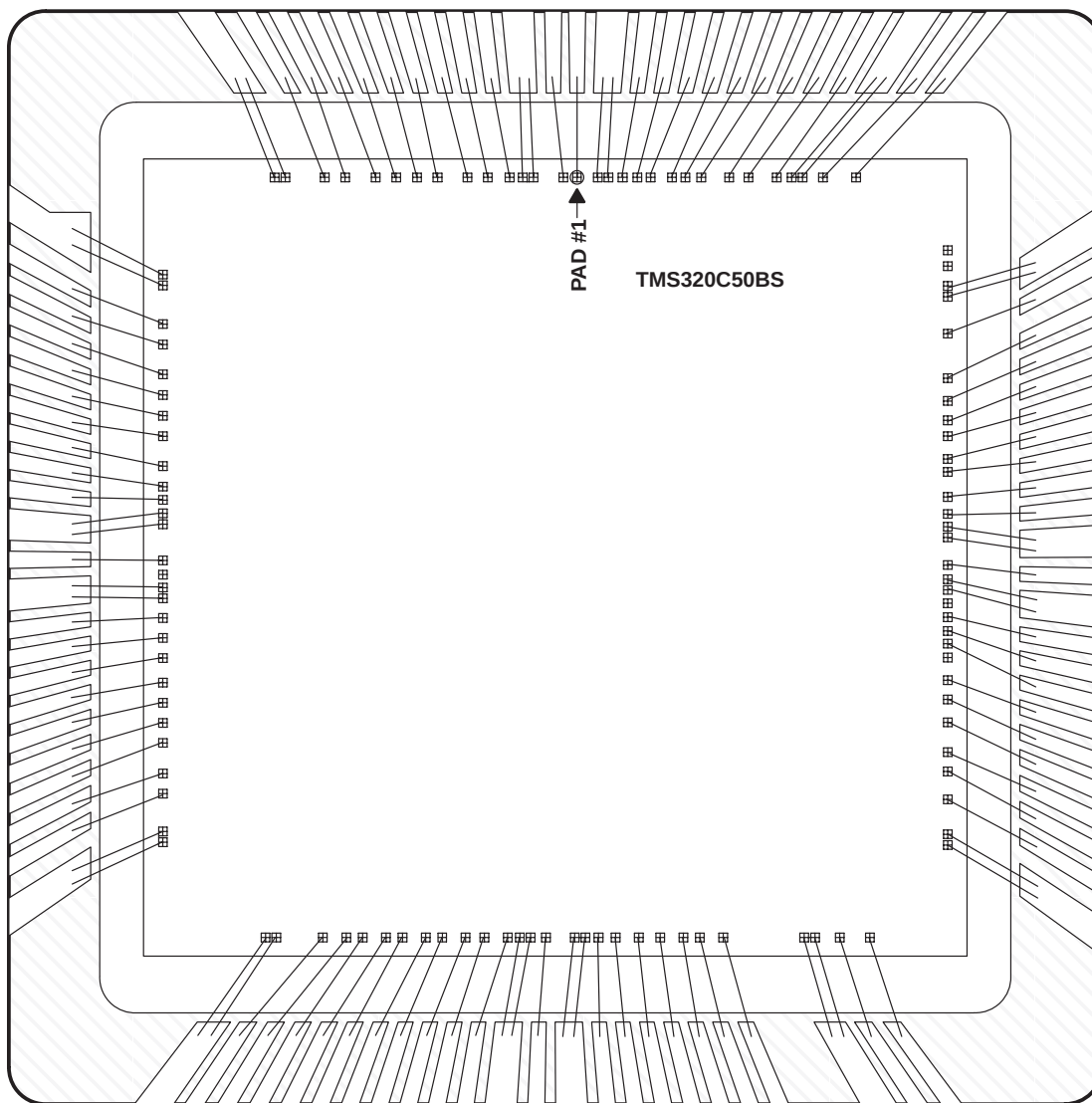
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