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4GB SDRAM - DDR3
MYX4DD3K512M72PBG2

***PRELIMINARY information. Subject to change without notice.**

4GByte DDR3 iPEM, Unbuffered w/ ECC - 512M x 72, 375 PBGA

Features

- V_{CC} = 1. 35V (-0.067V, + 1.00V)
- Differential biredirectional data strobe
- Differential clock inputs
- 8*n*-bit prefetch architecture
- 8 internal banks for concurrent operation (per DDR3 SDRAM Die)
- Auto refresh and self refresh modes
- Nominal and dynamic On-Die Termination (ODT)
- JEDEC On-Substrate FLY-BY Termination
- Programmable CAS latency: 6, 7, 8, 9, 10, 11
- Posted CAS additive latency: 0, 1, 2
- Differential Clock inputs (CK, CK\)
- Selectable BC4 or BL8 on the fly
- Write leveling
- Fixed Burst Length (BL) of 8 and Burst Chop (BC) of 4
- Programmable write latency = 5, 6, 7, 8 based on T_{CK}
- Military, Extended, and Industrial and Temp Options
- Organized as 512M x 72
- Weight: MYX4DD3K512M72PBG2 - 4 grams max.
- DDR3 Data rate = 800, 1066, 1333 and 1600 Mbps
- Self Refresh (Industrial Only)
- Partial Array Self Refresh (Industrial Only)
- Package:
  - 375 Plastic Ball Grid Array (PBGA). 19 x 21.5mm
  - 1.0mm pitch

Benefits

- 40% space savings vs. FBGA
- Reduced part count and memory-down routing
- 22% I/O reduction vs. FBGA approach
- Reduced trace lengths for lower parasitic capacitance
- Suitable for hi-reliability applications
- Address control and differential clock terminations included
- Designed as a complete memory subsystem with JEDEC Fly-By-Termination and shortest equal length, impedance matched signal routings. This providing a robust, signal integrity enhanced memory array solution

Addressing

Parameters	512K x 72
Row Addressing	A0-A15
Column Addressing	A0-A9
Bank Addressing	BA0-BA2
Page Size	2KB

Speed Options

Access Speed	800	1066	1333	1600
JEDCEC Speed Grade	DDR3-800E	DDR3-1066G	DDR3-1333H	DDR3-1600K
CL-nRCD-nRP	6 - 6 - 6	8 - 8 - 8	9 - 9 - 9	11 - 11 - 11
tRCD, tRP (MIN)	15.0 ns	15.0 ns	13.5 ns	13.75 ns

Figure 1: DDR3 iPEM Array vs. x8 Discrete BGA comparison

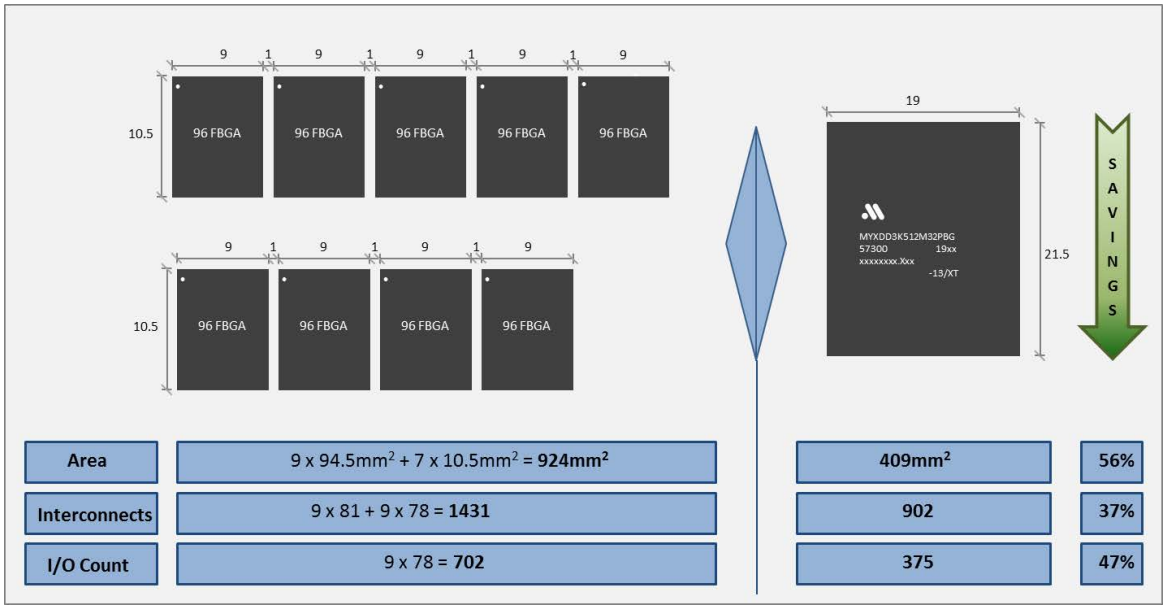
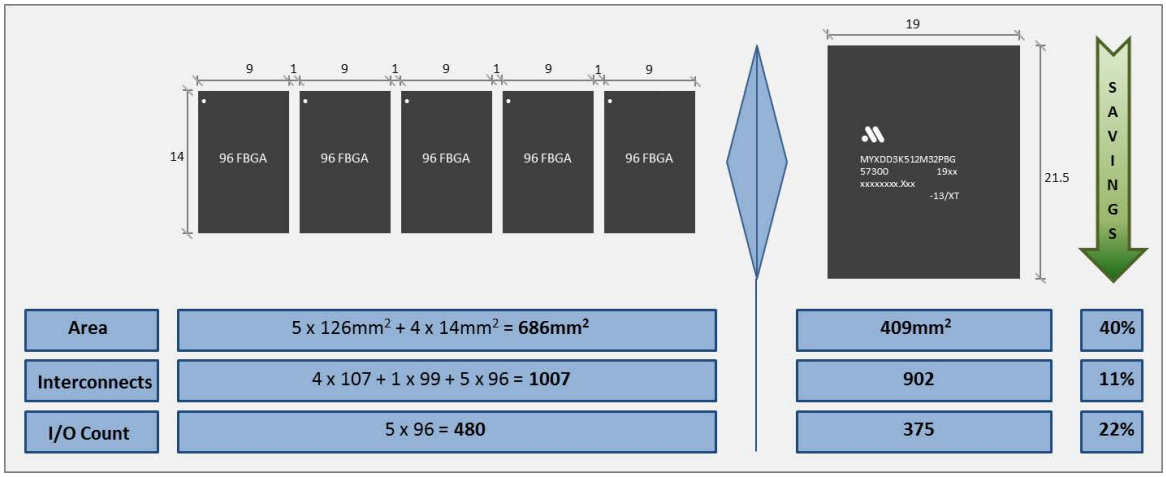


Figure 2: DDR3 iPEM Array vs. x16 Discrete BGA comparison



Functional Description

The MYX4DD3K512M72 is a CMOS DRAM memory containing five (5) 8GBit die. Each of the five die are configured as 8-bank DRAM. The device uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 8*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the device effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bitwide, one-half-clock-cycle data transfers at the I/O balls.

A differential data strobe (DQS, DQS\) is transmitted externally, along with data, for use in data capture at the receiver. DQS is center-aligned with data for writes. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The MYX4DD3K512M72 iPEM operates from a differential clock (CK and CK\); the crossing of CK going HIGH and CK\ going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

Read and write accesses to the DDR3 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is indicated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM enables concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self-refresh mode is provided, along with a power-saving, power-down mode.

General Notes

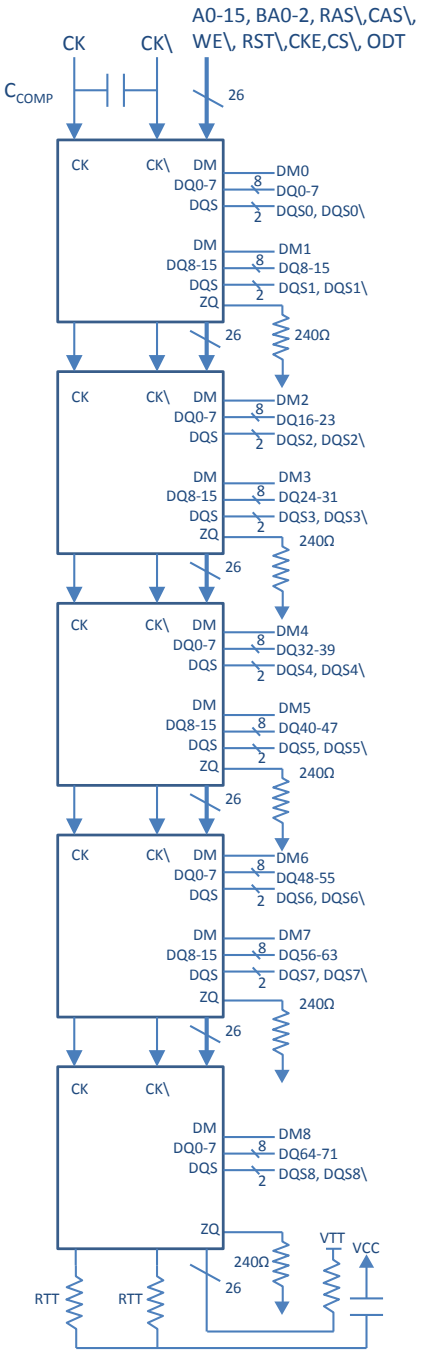
The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.

Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, each chip is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]), DM refers to UDM and DQS refers to UDQS.

Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Figure 3: Functional Block Diagram

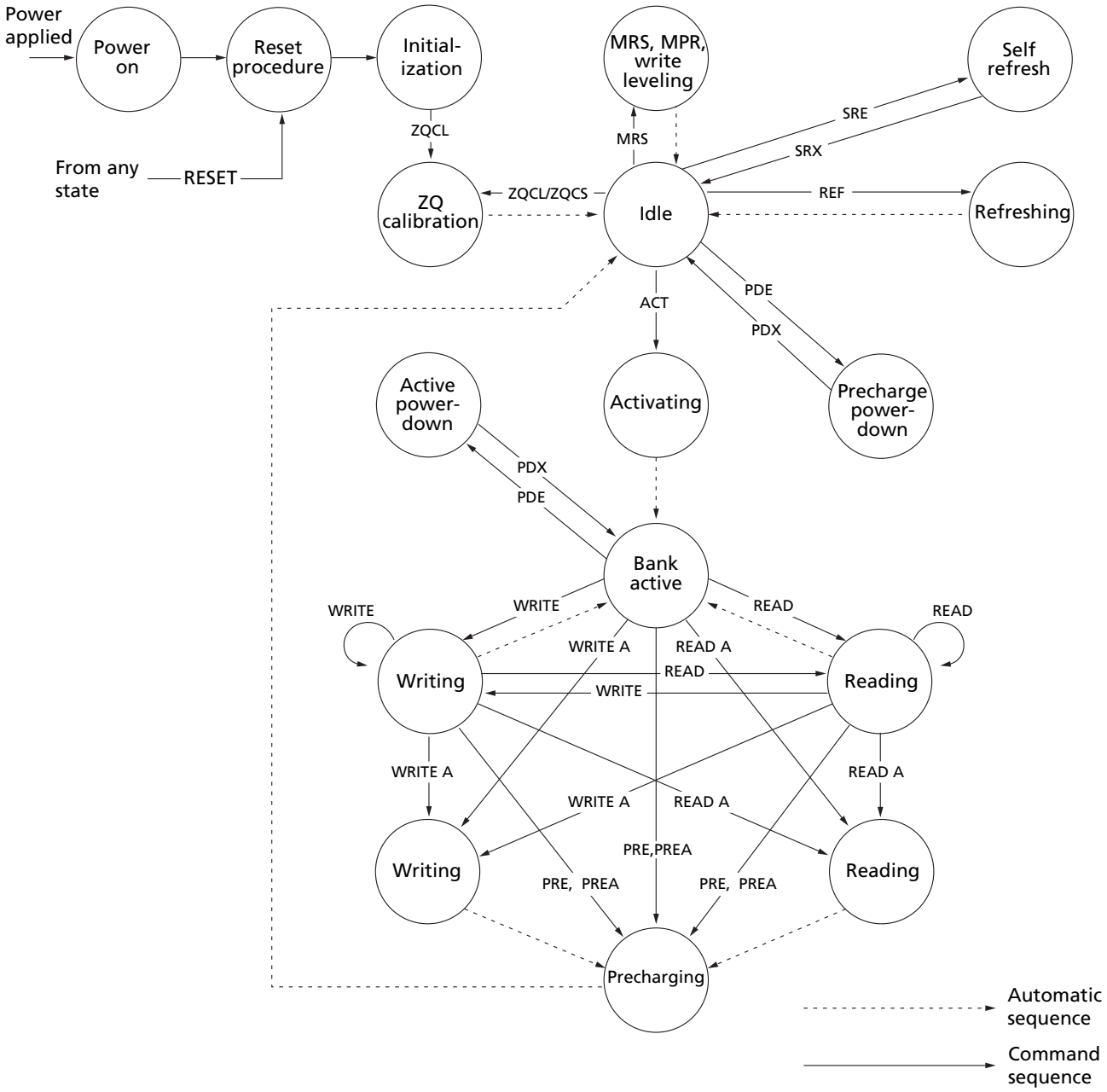


Note: Figure 2 indicates actual fly-by order.

Figure 4: 375-Ball PBGA (Top View, Ball Down)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A		GND	VCC	DM7	DQS7\	DQS7	DQ65	DQ69	DQ33	DQ39	DM4	DQ34	DQ36	DQ45	DQS6	DQS6\	DQS5\	DQS5	VCC	GND	GND	A
B	GND	VCC	DQ68	GND	DQ60	DQ71	GND	DQ56	DQ35	GND	VCC	GND	DQ50	DQ54	GND	DM5	DQ41	GND	DQ51	VCC	GND	B
C	VCC	DQ59	DQ70	DQ64	DQ62	DQ58	DQ67	DM8	DQ37	DQ32	DQ38	DQS4	DQS4\	DQ48	DQ52	DQ43	DQ47	DQ55	DQ40	DQ46	VCC	C
D	DQ63	GND	DQS8\	GND	DQ57	VCC	VCC	VCC	GND	VCC	GND	VCC	GND	VCC	VCC	VCC	DQ42	GND	DM6	GND	DQ53	D
E	DQ61	DQ66	DQS8	DQ13	DQ15	GND	VCC	NC	NC	NC	NC	NC	NC	NC	VCC	GND	DQ31	DQ28	DQ30	DQ49	DQ44	E
F	DQ11	DQ9	DQ12	DQS1\	DQS1	GND	VCC	NC	NC	NC	NC	NC	NC	NC	VCC	GND	DQ29	DQ24	DQS3	DQS3\	DQ26	F
G	DM1	GND	DQ14	GND	DQ10	VCC	VCC	NC	NC	NC	NC	NC	NC	NC	VCC	VCC	DQ27	GND	DQ25	GND	DM2	G
H	DQ0	DQ2	DQS0	DQ8	DM0	VCC	VCC	NC	NC	NC	NC	NC	NC	NC	VCC	VCC	DQS2	DQ16	DM3	DQ17	DQ19	H
J	DQ6	DQ4	DQS0\	DQ1	DQ3	GND	GND	NC	NC	NC	NC	NC	NC	NC	GND	GND	DQS2\	DQ22	DQ18	DQ23	DQ21	J
K		GND	DQ7	GND	DQ5	GND	GND	NC	NC	NC	NC	NC	NC	NC	GND	GND	NC	GND	DQ20	VCC		K
L	VCC	VCC	V_{REFDQ}	ODT	VCC	VCC	VCC	NC	NC	NC	NC	NC	NC	NC	VCC	VCC	GND	NC	NC	VCC	VCC	L
M	CK	GND	CAS\	WE\	VCC	VCC	VCC	NC	NC	NC	NC	NC	NC	NC	VCC	VCC	GND	VCC	GND	GND	GND	M
N	CK\	GND	A10	BA2	GND	GND	GND	NC	NC	NC	NC	NC	NC	NC	GND	GND	VCC	VCC	VCC	GND	GND	N
P	VCC	VCC	BA1	A0	GND	GND	GND	NC	NC	NC	NC	NC	NC	NC	GND	GND	VCC	VCC	VCC	GND	GND	P
R	A4	A2	A6	VTT	VCC	VCC	VCC	VCC	GND	GND	VCC	GND	GND	VCC	VCC	VCC	GND	GND	GND	VCC	VCC	R
T	VCC	VTT	VTT	A9	VCC	VCC	VCC	NC	A5	A12	CS\	RAS\	GND	VCC	VCC	VCC	GND	GND	GND	GND	VCC	T
U	GND	VCC	VTT	A8	GND	GND	GND	A14	A11	A3	A15	CKE	VCC	GND	GND	GND	VCC	VCC	VCC	VCC	GND	U
V	GND	GND	VCC	A13	GND	GND	GND	RST\	A7	A1	BA0	V_{REFCA}	VCC	GND	GND	GND	VCC	VCC	VCC	GND	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Figure 5: Simplified Functional State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short		

Table 1: Signal Descriptions

Symbol	Type	Description
A[15:13], A12/ BC#, A11, A10/ AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Table 7 (page 27).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK\	Input	**Clock:** CK and CK\ are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK\. Output data strobe (DQS, DQS\) is referenced to the crossings of CK and CK\.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK\, CKE, RESET\, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET\) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS\	Input	**Chip select:** CS\ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS\ is registered HIGH. CS\ provides for external rank selection on systems with multiple ranks. CS\ is considered part of the command code. CS\ is referenced to V_{REFCA}.
DM0-8	Input	**Input data mask:** DM0-8 is the, input write data mask per byte. Input data is masked when DMx is sampled HIGH along with the input data during a write access. Although the DMx pin is an input only pin, its loading is designed to match that of the DQxx and DQSx balls. DMx is referenced to VREFDQ
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS\, UDQS, UDQS\, LDM, and UDM.
RAS\, CAS\, WE\	Input	**Command inputs:** RAS\, CAS\, and WE\ (along with CS\) define the command being entered and are referenced to V_{REFCA}.
RST\	Input	**Reset:** RST\ is an active LOW CMOS input referenced to V_{SS}. The RST\ input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{CC} and DC LOW ≤ 0.2 × V_{CCQ}. RESET\ assertion and de-assertion are asynchronous.
DQ[71:0]	I/O	**Data input/output:** Bidirectional data bus DQ's are referenced to V_{REFDQ}.
DQS0-8, DQS\0-8	I/O	**Byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
V_{CC}	I/O	**Power supply:** 1.35V + 0.1V, -0.067V
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	**Ground**
NC	-	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
V_{TT}	Supply	**Termination supply**

Commands - Truth Tables

Table 2: Truth Table - Command

Notes 1-6 apply to the entire table.

Function	Abbrev.	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A11, A13 A14 A15	A12/BC#	A10/AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9,12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address(RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L		H	H	H	V	V	V	V	V	6,12
				L	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	H	H	H	H	V	V	V	V	V	6,12
				L	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	H	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Table 2: Truth Table - Command (continued)

Notes:
1. All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

Table 3: Truth Table - CKE

Notes 1 - 7 apply to the entire table.

Current State[2]	CKE		Command (N)[3] RAS#, CAS#, WE#, CS#	Action (N)[3]	Notes
	Previous Cycle[1] (N- 1)	Current Cycle[1](N)			
Power-Down	L	L	X	Maintain Power-Down	14,15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Bank Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9.13.18

Notes:
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh cannot be entered during Read or Write operations.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

Commands

DESELECT

The DESELECT (DES) command (CS\ HIGH) prevents new commands from being executed by the DRAM. Operations already in progress are not affected.

NO OPERATION

The NO OPERATION (NOP) command (CS\ LOW) prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

ZQ CALIBRATION LONG

The ZQ CALIBRATION LONG (ZQCL) command is used to perform the initial calibration during a power-up initialization and reset sequence (see Figure 11 & 21). This command may be issued at any time by the controller, depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the DRAM I/O, which are reflected as updated RON and ODT values.

The DRAM is allowed a timing window defined by either tZQinit or tZQoper to perform a full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter tZQinit must be satisfied. When initialization is complete, subsequent ZQCL commands require the timing parameter tZQoper to be satisfied.

ZQ CALIBRATION SHORT

The ZQ CALIBRATION SHORT (ZQCS) command is used to perform periodic calibrations to account for small voltage and temperature variations. A shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter tZQCS. A ZQCS command can effectively correct a minimum of 0.5% RON and RTT impedance error within 64 clock cycles.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA[2:0] inputs selects the bank, and the address provided on inputs A[n:0] selects the row. This row remains open (or active) for accesses until a PRECHARGE command is issued to that bank.

A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The address provided on inputs A[2:0] selects the starting column address, depending on the burst length and burst type selected. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. The value on input A12 (if enabled in the mode register) when the READ command is issued determines whether BC4 (chop) or BL8 is used. After a READ command is issued, the READ burst may not be interrupted.

Table 4: READ Command Summary

Functions		Symbol	CKE		CS\	RAS\	CAS\	WE\	BA [3:0]	A*n*	A12	A10	A[11, 9:0]
			Prev. Cycle	Next Cycle									
READ	BL8MRS, BC4MRS	RD	H		L	H	L	H	BA	RFU	V	L	CA
	BC4OTF	RDS4									L	L	
	BL8OTF	RDS8									H	L	
READ with auto precharge	BL8MRS, BC4MRS	RDAP									V	H	
	BC4OTF	RDAPS4									L	H	
	BL8OTF	RDAPS8									H	H	

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA[2:0] inputs selects the bank. The value on input A10 determines whether auto precharge is used. The value on input A12 (if enabled in the MR) when the WRITE command is issued determines whether BC4 (chop) or BL8 is used. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored and a WRITE will not be executed to that byte/column location.

Table 5: WRITE Command Summary

Functions		Symbol	CKE		CS\	RAS\	CAS\	WE\	BA [3:0]	A*n*	A12	A10	A[11, 9:0]
			Prev. Cycle	Next Cycle									
WRITE	BL8MRS, BC4MRS	WR	H		L	H	L	L	BA	RFU	V	L	CA
	BC4OTF	WRS4									L	L	
	BL8OTF	WRS8									H	L	
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP									V	H	
	BC4OTF	WRAPS4									L	H	
	BL8OTF	WRAPS8									H	H	

PRECHARGE

The PRECHARGE command is used to de-activate the open row in a particular bank or in all banks. The bank(s) are available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge. A READ or WRITE command to a different bank is allowed during a concurrent auto precharge as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are precharged. In the case where only one bank is precharged, inputs BA[2:0] select the bank; otherwise, BA[2:0] are treated as "Don't Care."

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period is determined by the last PRECHARGE command issued to the bank.

REFRESH

The REFRESH command is used during normal operation of the DRAM and is analogous to CAS\-before-RAS\ (CBR) refresh or auto refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during a REFRESH command. The DRAM requires REFRESH cycles at an average interval of 7.8µs (maximum when T_C ≤ 85°C or 3.9µs maximum when T_C ≤ 95°C or 1.95µs maximum when T°C</=125°C.). The REFRESH period begins when the REFRESH command is registered and ends ^{t}RFC (MIN) later.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to any given DRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is nine times the maximum average interval refresh rate. Self refresh may be entered with up to eight REFRESH commands being posted. After exiting self refresh (when entered with posted REFRESH commands), additional posting of REFRESH commands is allowed to the extent that the maximum number of cumulative posted REFRESH commands (both pre and post-self refresh) does not exceed eight REFRESH commands.

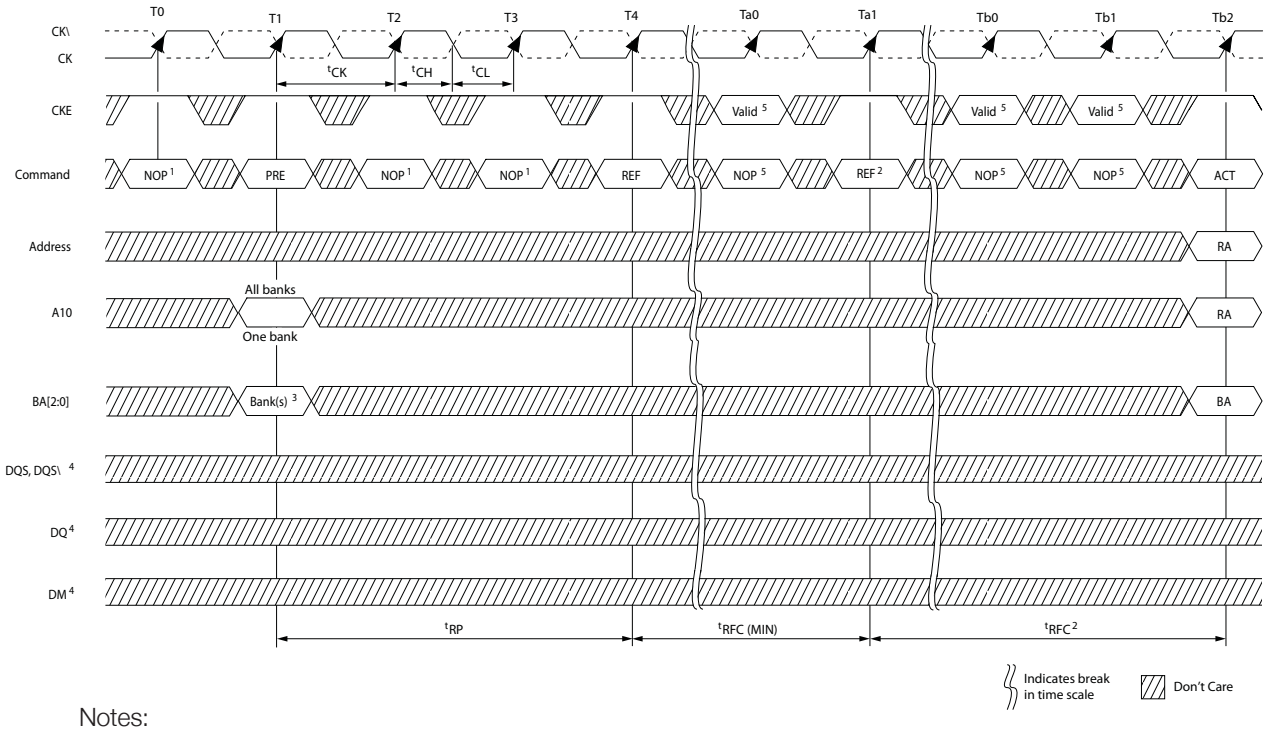
The posting limit of eight REFRESH commands is a JEDEC specification; however, as long as all the required number of REFRESH commands are issued within the refresh period (64ms), exceeding the eight posted REFRESH commands is allowed.

SELF REFRESH

The SELF REFRESH command is used to retain data in the DRAM, even if the rest of the system is powered down. When in self refresh mode, the DRAM retains data without external clocking. Self refresh mode is also a convenient method used to enable/disable the DLL as well as to change the clock frequency within the allowed synchronous operating range (see Input Clock Frequency Change). All power supply inputs (including V_{REFCA} and V_{REFDQ}) must be maintained at valid levels upon entry/exit and during self refresh mode operation. All power supply inputs (including V_{REFCA} and V_{REFDQ}) must be maintained at valid levels upon entry/exit and during self refresh mode operation. V_{REFDQ} may float or not drive $V_{CCQ/2}$ while in self refresh mode under the following conditions:

- $V_{SS} < V_{REFDQ} < V_{CC}$ is maintained
- V_{REFDQ} is valid and stable prior to CKE going back HIGH
- The first WRITE operation may not occur earlier than 512 clocks after V_{REFDQ} is valid
- All other self refresh mode exit timing requirements are met

Figure 6: Refresh Mode



Notes:

1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during the PRECHARGE, ACTIVATE, and REFRESH commands, but may be inactive at other times.
2. The second REFRESH is not required, but two back-to-back REFRESH commands are shown.
3. "Don't Care" if A10 is HIGH at this point; however, A10 must be HIGH if more than one bank is active (must precharge all active banks).
4. For operations shown, DM, DQ, and DQS signals are all "Don't Care"/High-Z.
5. Only NOP and DES commands are allowed after a REFRESH command and until ^{t}RFC (MIN) is satisfied.

PARTIAL ARRAY SELF REFRESH (PASR)

The PARTIAL ARRAY SELF REFRESH command is used to retain data in a portion of DRAM array as specified by Mode Register 2 and not refreshing the full array as a means to conserve power. Just as standard REFRESH modes, the DRAM retains data without external clocking.

PARTIAL ARRAY SELF REFRESH supports the following array refresh options, selected via A0, A1 and A2 of the Mode Register:

1/8 Array A[2:0] = 111, BA[2:0] = 111
1/4 Array A[2:0] = 110, BA[2:0] = 110 & 111
1/2 Array A[2:0] = 101, BA[2:0] = 100, 101,110,& 111
3/4 Array A[2:0] = 100, BA[2:0] = 010, 011, 100, 101, 110 & 111
1/8 Array A[2:0] = 011, BA[2:0] = 000
1/4 Array A[2:0] = 010, BA[2:0] = 000, 001
1/2 Array A[2:0] = 001, BA[2:0] = 000, 001, 010 & 011
1/1 Array A[2:0] = 000

DLL Disable Mode

If the DLL is disabled by the mode register (MR1[0] can be switched during initialization or later), the DRAM is targeted, but not guaranteed, to operate similarly to the normal mode, with a few notable exceptions:

- The DRAM supports only one value of CAS latency (CL=6) and one value of CAS WRITE latency (CWL=6).
- DLL disable mode affects the read data clock-to-data strobe relationship (^{t}DQSCK), but not the read data-to-data strobe relationship (^{t}DQSQ, ^{t}QH). Special attention is required to line up the read data with the controller time domain when the DLL is disabled.
- In normal operation (DLL on), ^{t}DQSCK starts from the rising clock edge AL + CL cycles after the READ command. In DLL disable mode, ^{t}DQSCK starts AL + CL-1 cycles after the READ command. Additionally, with the DLL disabled, the value of ^{t}DQSCK could be larger than ^{t}CK.

The ODT feature (including dynamic ODT) is not supported during DLL disable mode. The ODT resistors must be disabled by continuously registering the ODT ball LOW by programming R_{TT},nom MR1[9, 6, 2] and $R_{TT(WR)}$ MR2[10, 9] to 0 while in the DLL disable mode.

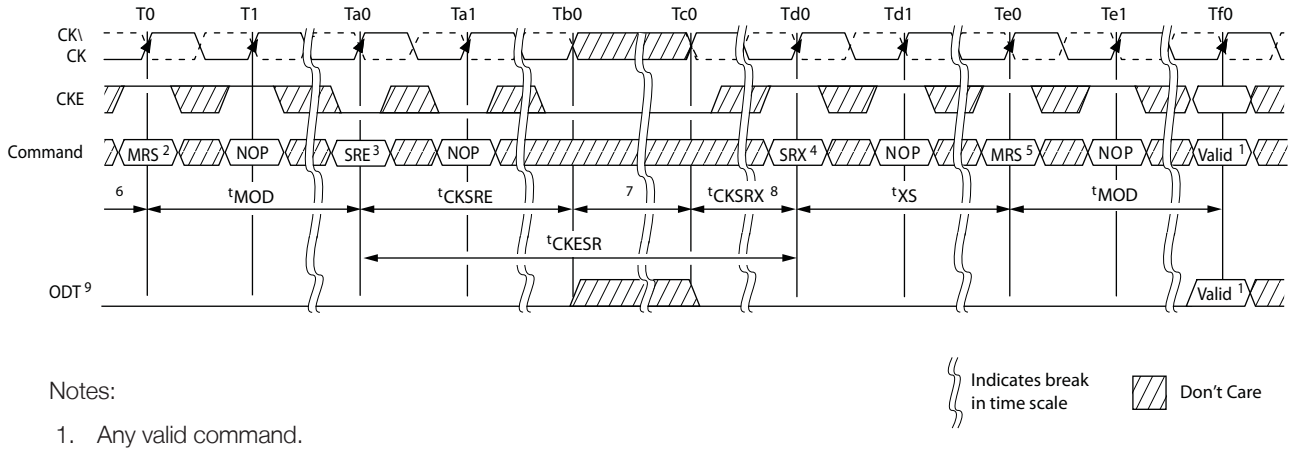
Specific steps must be followed to switch between the DLL enable and DLL disable modes due to a gap in the allowed clock rates between the two modes (^{t}CK [AVG] MAX and ^{t}CK [DLL_DIS] MIN, respectively). The only time the clock is allowed to cross this clock rate gap is during self refresh mode. Thus, the required procedure for switching from the DLL enable mode to the DLL disable mode is to change frequency during self refresh:

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and R_{TT},nom and $R_{TT(WR)}$ are High-Z), set MR1[0] to 1 to disable the DLL.
2. Enter self refresh mode after tMOD has been satisfied.
3. After ^{t}CKSRE is satisfied, change the frequency to the desired clock rate.
4. Self refresh may be exited when the clock is stable with the new frequency for ^{t}CKSRX. After ^{t}XS is satisfied, update the mode registers with appropriate values.
5. The DRAM will be ready for its next command in the DLL disable mode after the greater of ^{t}MRD or ^{t}MOD has been satisfied. A ZQCL command should be issued with appropriate timings met.

Table 6: READ Electrical Characteristics, DLL Disable Mode

Functions	Symbol	Min	Max	Unit
Access window of DQS from CK, CK\	^{t}DQSCK (DLL_DIS)	1	10	na

Figure 7: DLL Enable Mode to DLL Disable Mode



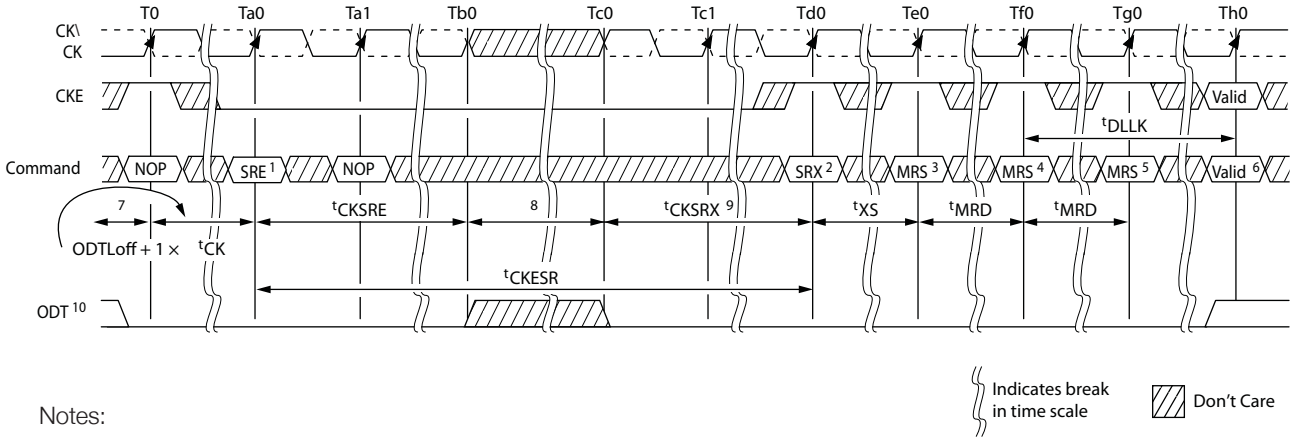
Notes:

1. Any valid command.
2. Disable DLL by setting MR1[0] to 1.
3. Enter SELF REFRESH.
4. Exit SELF REFRESH.
5. Update the mode registers with the DLL disable parameters setting.
6. Starting with the idle state, R_{TT} is in the High-Z state.
7. Change frequency.
8. Clock must be stable ^{t}CKSRX.
9. Static LOW in the case that $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; otherwise, static LOW or HIGH.

A similar procedure is required for switching from the DLL disable mode back to the DLL enable mode. This also requires changing the frequency during self refresh mode.

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and $R_{TT,nom}$ and $R_{TT(WR)}$ are High-Z), enter self refresh mode.
2. After ^{t}CKSRE is satisfied, change the frequency to the new clock rate.
3. Self refresh may be exited when the clock is stable with the new frequency for ^{t}CKSRX. After ^{t}XS is satisfied, update the mode registers with the appropriate values. At a minimum, set MR1[0] to 0 to enable the DLL. Wait ^{t}MRD, then set MR0[8] to 1 to enable DLL RESET.
4. After another ^{t}MRD delay is satisfied, update the remaining mode registers with the appropriate values.
5. The DRAM will be ready for its next command in the DLL enable mode after the greater of ^{t}MRD or ^{t}MOD has been satisfied. However, before applying any command or function requiring a locked DLL, a delay of ^{t}DLLK after DLL RESET must be satisfied. A ZQCL command should be issued with the appropriate timings met.

Figure 8: DLL Disable Mode to DLL Enable Mode



Notes:

1. Enter SELF REFRESH.
2. Exit SELF REFRESH.
3. Wait ^{t}XS, then set MR1[0] to 0 to enable DLL.
4. Wait ^{t}MRD, then set MR0[8] to 1 to begin DLL RESET.
5. Wait ^{t}MRD, update registers (CL, CWL, and write recovery may be necessary).
6. Wait ^{t}MOD, any valid command.
7. Starting with the idle state.
8. Change frequency.
9. Clock must be stable at least ^{t}CKSRX.
10. Static LOW in the case that $R_{TT,nom}$ or $R_{TT(WR)}$ is enabled; otherwise, static LOW or HIGH.

The clock frequency range for the DLL disable mode is specified by the parameter ^{t}CK (DLL_DIS). Due to latency counter and timing restrictions, only CL = 6 and CWL = 6 are supported.

DLL disable mode will affect the read data clock to data strobe relationship (^{t}DQSCK) but not the data strobe to data relationship (^{t}DQSQ, ^{t}QH). Special attention is needed to line up read data to the controller time domain.

Compared to the DLL on mode where ^{t}DQSCK starts from the rising clock edge AL + CL cycles after the READ command, the DLL disable mode ^{t}DQSCK starts AL + CL - 1 cycles after the READ command.

WRITE operations function similarly between the DLL enable and DLL disable modes; however, ODT functionality is not allowed with DLL disable mode.

Input Clock Frequency Change

When the DDR3 SDRAM is initialized, the clock must be stable during most normal states of operation. This means that after the clock frequency has been set to the stable state, the clock period is not allowed to deviate, except for what is allowed by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another under two conditions: self refresh mode and precharge power-down mode. It is illegal to change the clock frequency outside of those two modes. For the self refresh mode condition, when the DDR3 SDRAM has been successfully placed into self refresh mode and ^{t}CKSRE has been satisfied, the state of the clock becomes a “Don’t Care.” When the clock becomes a “Don’t Care,” changing the clock frequency is permissible if the new clock frequency is stable prior to ^{t}CKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met.

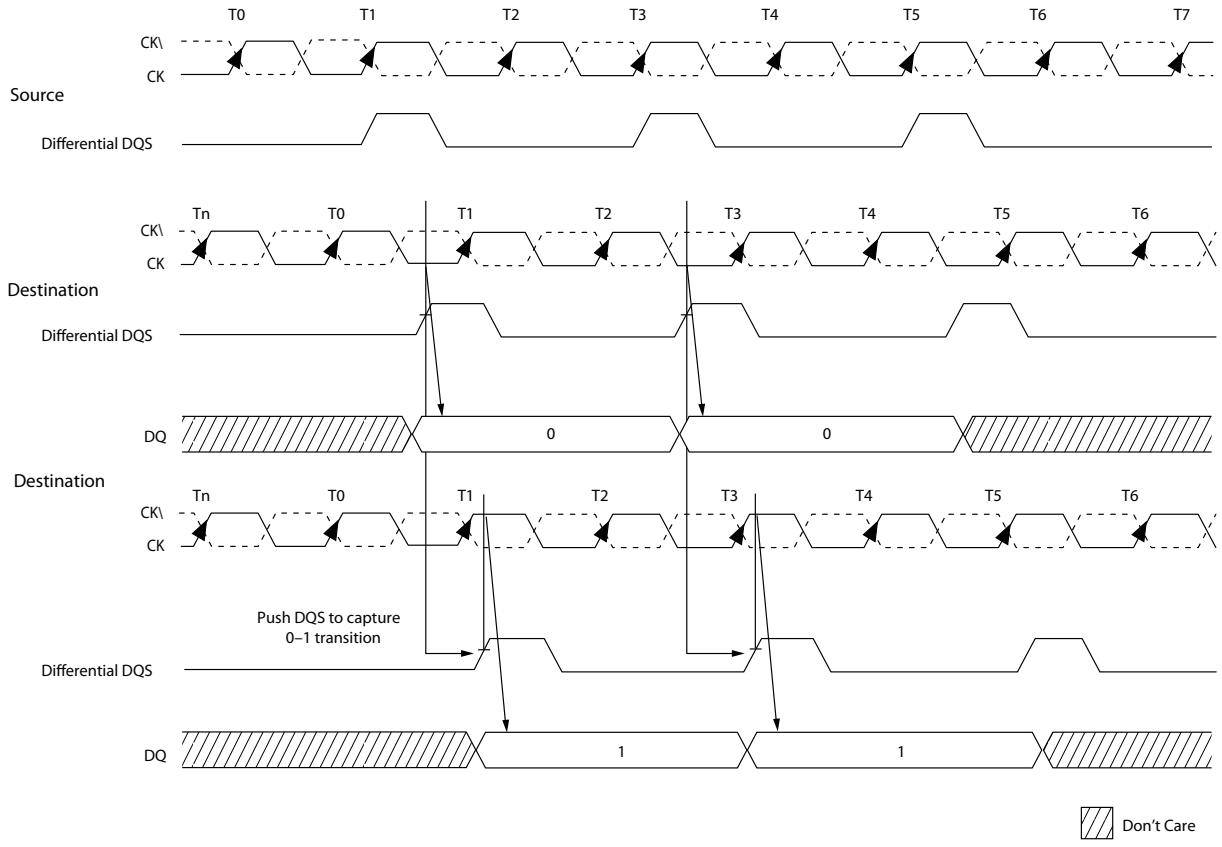
The precharge power-down mode condition is when the DDR3 SDRAM is in precharge power-down mode (either fast exit mode or slow exit mode). Either ODT must be at a logic LOW or R_{TT},nom and $R_{TT(WR)}$ must be disabled via MR1 and MR2. This ensures R_{TT},nom and $R_{TT(WR)}$ are in an off state prior to entering precharge power-down mode, and CKE must be at a logic LOW. A minimum of ^{t}CKSRE must occur after CKE goes LOW before the clock frequency can change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade (^{t}CK [AVG] MIN to ^{t}CK [AVG] MAX). During the input clock frequency change, CKE must be held at a stable LOW level. When the input clock frequency is changed, a stable clock must be provided to the DRAM ^{t}CKSRX before precharge power-down may be exited. After precharge power-down is exited and ^{t}XP has been satisfied, the DLL must be reset via the MRS. Depending on the new clock frequency, additional MRS commands may need to be issued. During the DLL lock time, R_{TT},nom and $R_{TT(WR)}$ must remain in an off state. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

Write Leveling

For better signal integrity, DDR3 SDRAM memory modules have adopted fly-by topology for the commands, addresses, control signals, and clocks. Write leveling is a scheme for the memory controller to adjust or de-skew the DQS strobe (DQS, DQS\) to CK relationship at the DRAM with a simple feedback feature provided by the DRAM. Write leveling is generally used as part of the initialization process, if required. For normal DRAM operation, this feature must be disabled. This is the only DRAM operation where the DQS functions as an input (to capture the incoming clock) and the DQ function as outputs (to report the state of the clock). Note that nonstandard ODT schemes are required.

The memory controller using the write leveling procedure must have adjustable delay settings on its DQS strobe to align the rising edge of DQS to the clock at the DRAM pins. This is accomplished when the DRAM asynchronously feeds back the CK status via the DQ bus and samples with the rising edge of DQS. The controller repeatedly delays the DQS strobe until a CK transition from 0 to 1 is detected. The DQS delay established by this procedure helps ensure ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications in systems that use fly-by topology by de-skewing the trace length mismatch. Refer to Figure 9.

Figure 9: Write Leveling Concept



Write Leveling Procedure

A memory controller initiates the DRAM write leveling mode by setting MR1[7] to 1, assuming the other programmable features (MR0, MR1, MR2, and MR3) are first set and the DLL is fully reset and locked. The DQ balls enter the write leveling mode going from a High-Z state to an undefined driving state, so the DQ bus should not be driven. During write leveling mode, only the NOP or DES commands are allowed. The memory controller should attempt to level only one rank at a time; thus, the outputs of other ranks should be disabled by setting MR1[12] to 1 in the other ranks. The memory controller may assert ODT after a ^{t}MOD delay, as the DRAM will be ready to process the ODT transition. ODT should be turned on prior to DQS being driven LOW by at least ODTLon delay (WL - 2 tCK), provided it does not violate the aforementioned ^{t}MOD delay requirement.

The memory controller may drive DQS LOW and DQS\ HIGH after ^{t}WLDQSEN has been satisfied. The controller may begin to toggle DQS after ^{t}WLMRD (one DQS toggle is DQS transitioning from a LOW state to a HIGH state with DQS\ transitioning from a HIGH state to a LOW state, then both transition back to their original states). At a minimum, ODTLon and ^{t}AON must be satisfied at least one clock prior to DQS toggling.

After ^{t}WLMRD and a DQS LOW preamble (^{t}WPRE) have been satisfied, the memory controller may provide either a single DQS toggle or multiple DQS toggles to sample CK for a given DQS-to-CK skew. Each DQS toggle must not violate ^{t}DQSL (MIN) and ^{t}DQSH (MIN) specifications. ^{t}DQSL (MAX) and ^{t}DQSH (MAX) specifications are not applicable during write leveling mode. The DQS must be able to distinguish the CK's rising edge within ^{t}WLS and ^{t}WLH. The prime DQ will output the CK's status asynchronously from the associated DQS rising edge CK capture within ^{t}WLO. The remaining DQ that always drive LOW when DQS is toggling must be LOW within ^{t}WLOE after the first ^{t}WLO is satisfied (the prime DQ going LOW). As previously noted, DQS is an input and not an output during this process.

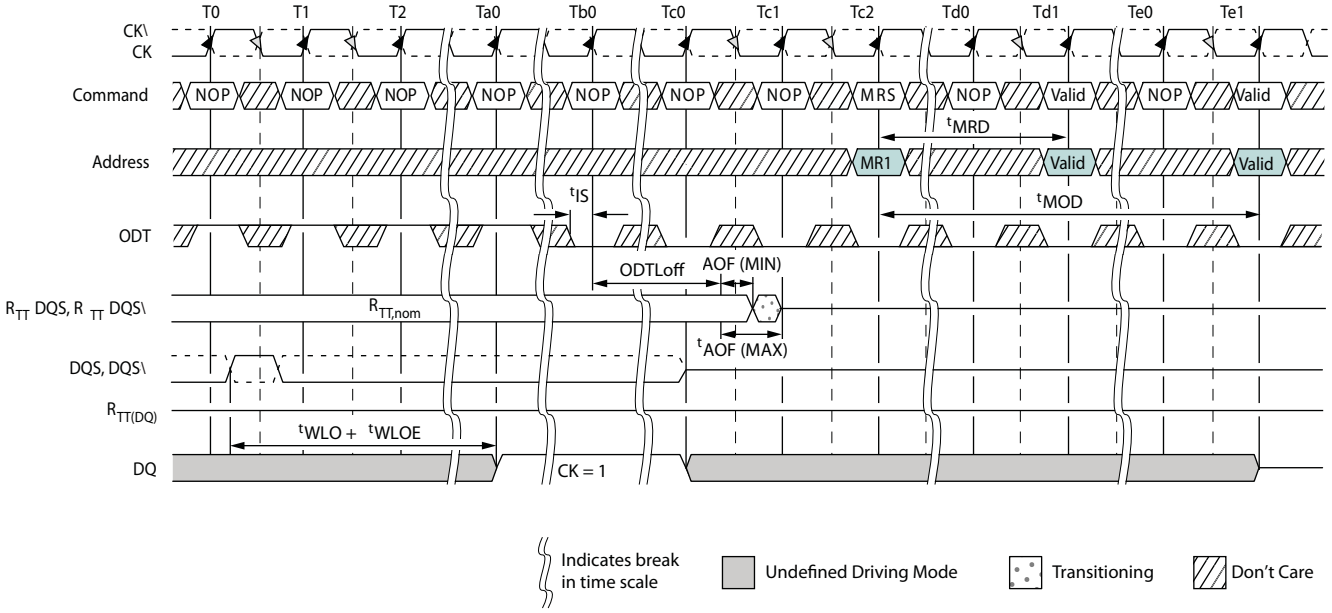
The memory controller will most likely sample each applicable prime DQ state and determine whether to increment or decrement its DQS delay setting. After the memory controller performs enough DQS toggles to detect the CK's 0-to-1 transition, the memory controller should lock the DQS delay setting for that DRAM. After locking the DQS setting is locked, leveling for the rank will have been achieved, and the write leveling mode for the rank should be disabled or reprogrammed (if write leveling of another rank follows).

Write Leveling Mode Exit Procedure

After the DRAM are leveled, they must exit from write leveling mode before the normal mode can be used. Figure 10 depicts a general procedure for exiting write leveling mode. After the last rising DQS (capturing a 1 at T0), the memory controller should stop driving the DQS signals after ^{t}WLO (MAX) delay plus enough delay to enable the memory controller to capture the applicable prime DQ state (at ~Tb0). The DQ balls become undefined when DQS no longer remains LOW, and they remain undefined until ^{t}MOD after the MRS command (at Te1).

The ODT input should be de-asserted LOW such that ODTLoff (MIN) expires after the DQS is no longer driving LOW. When ODT LOW satisfies ^{t}IS, ODT must be kept LOW (at ~Tb0) until the DRAM is ready for either another rank to be leveled or until the normal mode can be used. After DQS termination is switched off, write level mode should be disabled via the MRS command (at Tc2). After ^{t}MOD is satisfied (at Te1), any valid command may be registered by the DRAM. Some MRS commands may be issued after ^{t}MRD (at Td1).

Figure 10: Write Leveling Exit Procedure



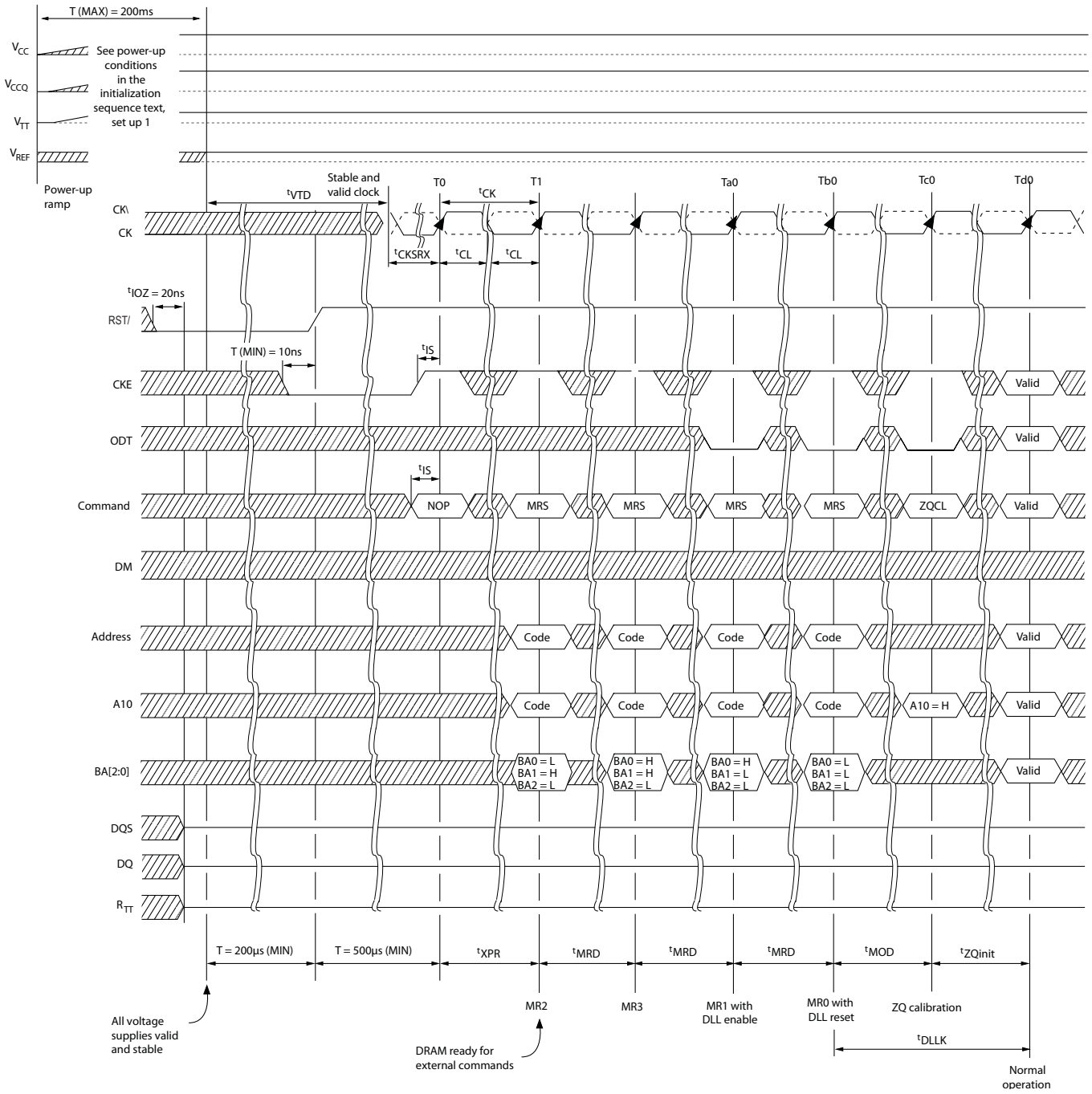
Note: The DQ result, = 1, between Ta0 and Tc0, is a result of the DQS, DQS\ signals capturing CK HIGH just after the T0 state.

Initialization

The following sequence is required for power-up and initialization, as shown in Figure 11:

1. Apply power. RST\ is recommended to be below 0.2 × V_{CC} during power ramp to ensure the outputs remain disabled (High-Z) and ODT off (R_{TT} is also High-Z). All other inputs, including ODT, may be undefined. During power-up, either of the following conditions may exist and must be met:
   - Condition A:
     - V_{CC} is driven from a single-power converter output. Slope reversal of any power supply signal is allowed. The voltage levels on all balls other than V_{CC} and V_{SS} must be less than or equal to V_{CC} on one side, and must be greater than or equal to V_{SS} on the other side.
     - V_{CC} power supply ramps to V_{CC},min and $^{t}V_{CCPR}$ = 200ms.
     - V_{REFDQ} tracks V_{CC} × 0.5, V_{REFCA} tracks V_{CC} × 0.5.
     - V_{TT} is limited to 0.95V when the power ramp is complete and is not applied directly to the device; however, ^{t}VTD should be greater than or equal to 0 to avoid device latchup.
   - Condition B:
     - V_{CC} may be applied before or at the same time as V_{TT}, V_{REFDQ}, and V_{REFCA}.
     - No slope reversals are allowed in the power supply ramp for this condition.
2. Until stable power, maintain RST\ LOW to ensure the outputs remain disabled (High-Z). After the power is stable, RST\ must be LOW for at least 200µs to begin the initialization process. ODT will remain in the High-Z state while RESET\ is LOW and until CKE is registered HIGH.
3. CKE must be LOW 10ns prior to RST\ transitioning HIGH.
4. After RST\transitions HIGH, wait 500µs (minus one clock) with CKE LOW.
5. After the CKE LOW time, CKE may be brought HIGH (synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns (and a minimum of five clocks) and ODT must be driven LOW at least tIS prior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.
6. After CKE is registered HIGH and after tXPR has been satisfied, MRS commands may be issued. Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).
7. Issue an MRS command to MR3 with the applicable settings.
8. Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring ODT.
9. Issue an MRS command to MR0 with the applicable settings, including a DLL RESET command. ^{t}DLLK (512) cycles of clock input are required to lock the DLL.
10. Issue a ZQCL command to calibrate R_{TT} and R_{ON} values for the process voltage temperature (PVT). Prior to normal operation, ^{t}ZQinit must be satisfied.
11. When ^{t}DLLK and ^{t}ZQinit

Figure 11: Initialization Sequence



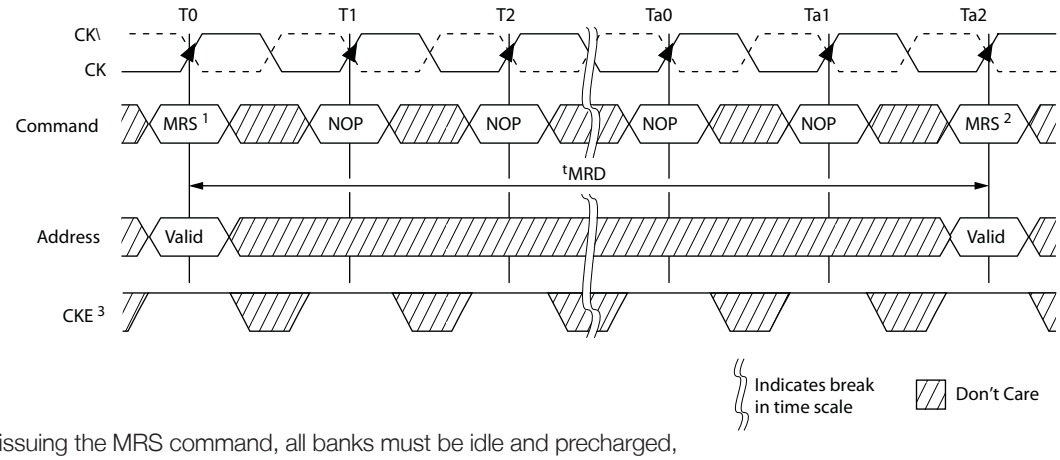
Mode Registers

Mode registers (MR0–MR3) are used to define various modes of programmable operations of the DDR3 SDRAM. A mode register is programmed via the mode register set (MRS) command during initialization, and it retains the stored information (except for MR0[8], which is self-clearing) until it is reprogrammed, RST\ goes LOW, the device loses power.

Contents of a mode register can be altered by re-executing the MRS command. Even if the user wants to modify only a subset of the mode register's variables, all variables must be programmed when the MRS command is issued. Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The MRS command can only be issued (or re-issued) when all banks are idle and in the precharged state (^{t}RP is satisfied and no data bursts are in progress). After an MRS command has been issued, two parameters must be satisfied: ^{t}MRD and ^{t}MOD. The controller must wait ^{t}MRD before initiating any subsequent MRS commands.

Figure 12: MRS to MRS Command Timing (^{t}MRD)

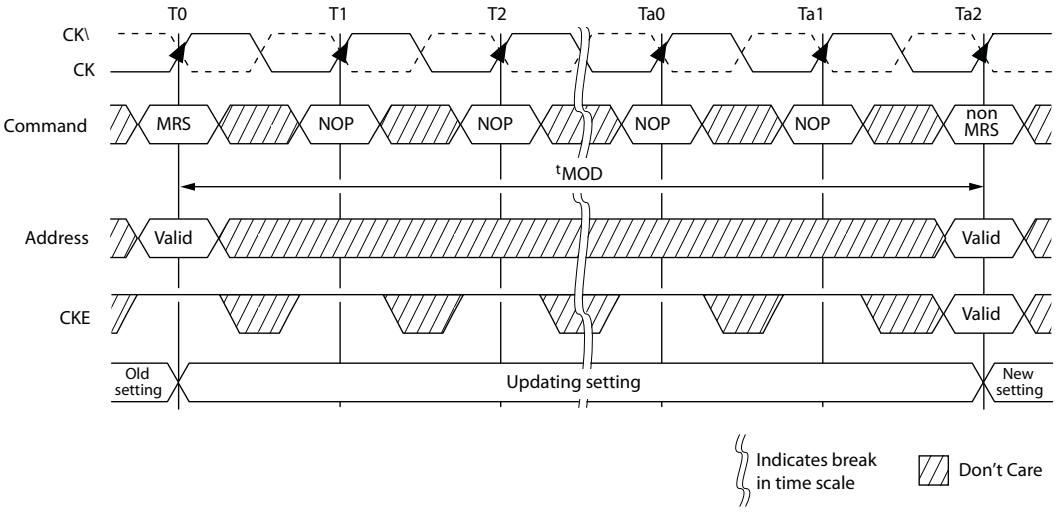


Notes:

1. Prior to issuing the MRS command, all banks must be idle and precharged, ^{t}RP (MIN) must be satisfied, and no data bursts can be in progress.
2. ^{t}MRD specifies the MRS to MRS command minimum cycle time.
3. CKE must be registered HIGH from the MRS command until ^{t}MRSPDEN (MIN).
4. For a CAS latency change, ^{t}XPDLL timing must be met before any non-MRS command.

The controller must also wait ^{t}MOD before initiating any non-MRS commands (excluding NOP and DES). The DRAM requires ^{t}MOD in order to update the requested features, with the exception of DLL RESET, which requires additional time. Until ^{t}MOD has been satisfied, the updated features are to be assumed unavailable.

Figure 13: MRS to nonMRS Command Timing (tMOD)



Notes:

1. Prior to issuing the MRS command, all banks must be idle (they must be precharged, tRP must be satisfied, and no data bursts can be in progress).
2. Prior to Ta2 when tMOD (MIN) is being satisfied, no commands (except NOP/DES) may be issued.
3. If R_{TT} was previously enabled, ODT must be registered LOW at T0 so that ODTL is satisfied prior to Ta1. ODT must also be registered LOW at each rising CK edge from T0 until tMODmin is satisfied at Ta2.
4. CKE must be registered HIGH from the MRS command until tMRSPDEN (MIN), at which time power-down may occur.

Mode Registers

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to the following figure.

Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 14. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 7 . The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

Figure 14: Mode Register 0 (MR0) Definitions

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	**0*[1]**	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL		Address Field / Mode Register 0

A8	DLL Reset
0	No
1	Yes

A7	mode
0	Nomal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge Power-Down (PPD)
0	Slow exit (DLL off)
1	Fast exit (DLL on)

BA1	BA0	MR Select
0	**0**	**MR0**
0	1	MR1
1	0	MR2
1	1	MR3

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5*[2]
0	1	0	6*[2]
0	1	1	7*[2]
1	0	0	8*[2]
1	0	1	10*[2]
1	1	0	12*[2]
1	1	1	14*[2]

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14
0	1	1	1	Reserved
1	0	0	1	Reserved
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

1. A15,A14 and A13 must be programmed to 0 during MRS.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table only shows the encoding for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency
4. The table only shows the encoding for Write Recovery. For actual Write recovery timing, please refer to AC timing table.

Table 7: Burst Order

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		10	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		11	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		100	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		101	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		110	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		111	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		10	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		11	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		101	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		110	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		111	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

Notes:
1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

DLL RESET

DLL RESET is defined by MR0[8] (see Figure 14). Programming MR0[8] to 1 activates the DLL RESET function. The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

Precharge Power-Down (Precharge PD)

The precharge power-down (PD) bit applies only when precharge powerdown mode is being used. When MR0[12] is set to 0, the DLL is off during precharge power-down, providing a lower standby current mode; however, ^{t}XPDLL must be satisfied when exiting. When MR0[12] is set to 1, the DLL continues to run during precharge power-down mode to enable a faster exit of precharge power-down mode; however, ^{t}XP must be satisfied when exiting.

Write Recovery

WRITE recovery time is defined by MR0[11:9]and is used for the Auto Precharge feature along with tRP to determine tDAL.. Write recovery values of 5, 6, 7, 8, 10, 12, or 14 may be used by programming MR0[11:9]. The user is required to program the correct value of write recovery, is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal to or larger than tWR(min).

CAS Latency (CL)

CAS latency (CL) is defined by MR0[2] & MR0[6:4], as shown in Figure 14. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The CL can be set to 5, 6, 7, 8, 9, 10, 11, 12, 13 or 14. DDR3 SDRAM do not support half-clock latencies.

Mode Register 1 (MR1)

The mode register 1 (MR1) controls additional features and functions not available in the other mode registers: DLL ENABLE/DISABLE, output drive strength, OUTPUT ENABLE/DISABLE (Q OFF), on-die termination (ODT) resistance value R_{TT},nom, WRITE LEVELING, and posted CAS additive latency (AL). These features and functions are controlled via the bits shown in the Figure 15. The MR1 register is programmed via the MRS command and retains the stored information until it is reprogrammed, RESET\ goes LOW, or the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided it is reprogrammed correctly.

The MR1 register must be loaded when all banks are idle and no bursts are in progress. The controller must satisfy the specified timing parameters ^{t}MRD and ^{t}MOD before initiating a subsequent operation.

DLL ENABLE/DISABLE

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command (see Figure 15). The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation, after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering self refresh mode, the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled and reset upon exit of the SELF REFRESH operation. If the DLL is disabled prior to entering self refresh mode, the DLL remains disabled, even upon exit of the SELF REFRESH operation until it is re-enabled and reset.

The DRAM is not tested to check nor does Micross warrant compliance with normal mode timings or functionality when the DLL is disabled. An attempt has been made to have the DRAM operate in the normal mode where reasonably possible when the DLL has been disabled; however, by industry standard, a few known exceptions are defined:

- ODT is not allowed to be used.
- The output data is no longer edge-aligned to the clock.
- CL and CWL can only be six clocks.

When the DLL is disabled, timing and functionality can vary from the normal operation specifications when the DLL is enabled (see DLL Disable Mode). Disabling the DLL also implies the need to change the clock frequency.

Output Drive Strength, Impedance Control

The DDR3 SDRAM uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5,1]. RZQ/7 (34Ω[NOM]) is the primary output driver impedance setting for DDR3 SDRAM devices. To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and V_{SSQ}. The value of the resistor must be 240Ω ±1%.

The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation, and all data sheet timings and current specifications are met during an update.

Figure 15: Mode Register 1 (MR1) Definition

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0	0	**1**	**0*[1]**	Qoff	TDQS	**0*[1]**	Rtt	**0*[1]**	Level	Rtt	D.I.C	AL		Rtt	D.I.C	DLL	Mode Register 1

A11	TDQS enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A9	A6	A2	Rtt_Nom *3
0	0	0	ODT disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, DQSs, DQS#s.

BA1	BA0	MR Select
0	0	MR0
0	**1**	**MR1**
1	0	MR2
1	1	MR3

Note: RZQ = 240 Ω
*3:In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
*4:If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

A5	A1	Output Driver Impedance Control
0	0	RZQ/6 (40 ohm NOM)
0	1	RZQ/7 (34 ohm NOM)
1	0	Reserved
1	1	Reserved

* 1 : A8, A10, A13, A14, and A15 must be programmed to 0 during MRS.
* TDQS must be disabled for x16 option.

To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up, the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE/DISABLE function is defined by MR1[12] (see Figure 15). When enabled (MR1[12] = 0), all outputs (DQ, DQS, DQS\) function when in the normal mode of operation. When disabled (MR1[12] = 1), all DDR3 SDRAM outputs (DQ and DQS, DQS\) are High-Z. The output disable feature is intended to be used during I_{CC} characterization of the READ current and during ^{t}DQSS margining (write leveling) only.

On-Die Termination (ODT)

On-die termination (ODT) resistance $R_{TT,nom}$ is defined by MR1[9, 6, 2] (see Figure 15). The R_{TT} termination resistance value applies to the DQ, DM, DQS, and DQS\ balls. DDR3 supports multiple R_{TT} termination resistance values based on RZQ/n where n can be 2, 4, 6, 8, or 12 and RZQ is 240Ω

Unlike DDR2, DDR3 ODT must be turned off prior to reading data out and must remain off during a READ burst. $R_{TT,nom}$ termination is allowed any time after the DRAM is initialized, calibrated, and not performing read accesses, or when it is not in self refresh mode. Additionally, write accesses with dynamic ODT ($R_{TT(WR)}$) enabled temporarily replaces $R_{TT,nom}$ with $R_{TT(WR)}$.

The effective termination, $R_{TT(EFF)}$, may be different from R_{TT} targeted due to nonlinearity of the termination.

The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on/off ODT for any or all devices. The ODT input control pin is used to determine when RTT is turned on (ODTLon) and off (ODTLoff), assuming ODT has been enabled

WRITE LEVELING

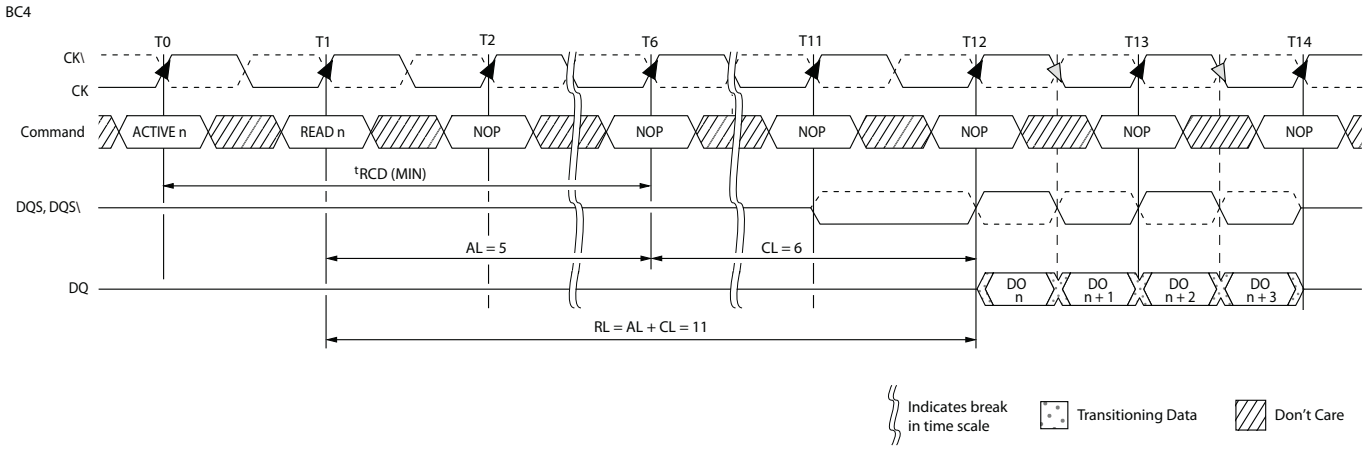
The WRITE LEVELING function is enabled by MR1[7] (see Figure 15). Write leveling is used (during initialization) to deskew the DQS strobe to clock offset as a result of fly-by topology designs. For better signal integrity, DDR3 SDRAM memory modules adopted fly-by topology for the commands, addresses, control signals, and clocks.

The fly-by topology benefits from a reduced number of stubs and their lengths. However, fly-by topology induces flight time skews between the clock and DQS strobe (and DQ) at each DRAM on the DIMM. Controllers will have a difficult time maintaining tDQSS, tDSS, and tDSH specifications without supporting write leveling in systems that use fly-by topology-based modules.

Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. MR1[4, 3] define the value of AL (see Figure 16). MR1[4, 3] enable the user to program the DDR3 SDRAM with AL = 0, CL - 1, or CL - 2. With this feature, the DDR3 SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank prior to tRCD (MIN). The only restriction is ACTIVATE to READ or WRITE + AL ≥ tRCD (MIN) must be satisfied. Assuming tRCD (MIN) = CL, a typical application using this feature sets AL = CL - 1tCK = tRCD (MIN) - 1 tCK. The READ or WRITE command is held for the time of the AL before it is released internally to the DDR3 SDRAM device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL), RL = AL + CL. WRITE latency (WL) is the sum of CAS WRITE latency and AL, WL = AL + CWL (see Mode Register 2 (MR2). Examples of READ and WRITE latencies are shown in Figure 16 and Figure 18.

Figure 16: READ Latency (AL = 5, CL = 6)



Mode Register 1 (MR1)

The mode register 2 (MR2) controls additional features and functions not available in the other mode registers. These addional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT), and DYNAMIC ODT ($R_{TT(WR)}$). These functions are controlled via the bits shown in the Figure 17. MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided it is reprogrammed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time tMRD and tMOD before initiating a subsequent operation.

Figure 17: Mode Register 2 (MR2) Definition

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	**0**	**0*1**			**Rtt_WR**		**0*1**	SRT	ASR	CWL			PASR			Mode Register 2

A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended operating temperature range

A6	Auto Self-Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable

A2	A1	A0	Partial Array Self-Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0] = 000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0] = 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt_WR *2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≥ 2.5 ns)
0	0	1	6 (2.5 ns > tCK(avg) ≥ 1.875 ns)
0	1	0	7 (1.875 ns > tCK(avg) ≥ 1.5 ns)
0	1	1	8 (1.5 ns > tCK(avg) ≥ 1.25 ns)
1	0	0	9 (1.25 ns > tCK(avg) ≥ 1.07ns)
1	0	1	10 (1.07 ns > tCK(avg) ≥ 0.935 ns)
1	1	0	Reserved
1	1	1	Reserved

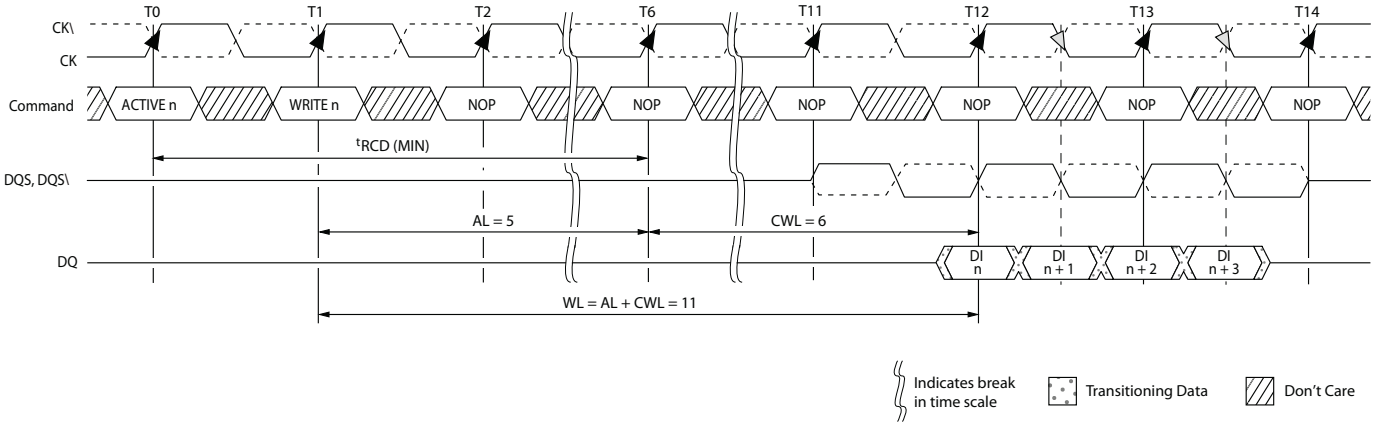
BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	**0**	**MR2**
1	1	MR3

* 1 : A5, A8, A11 ~ A15 must be programmed to 0 during MRS.
* 2 : The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

CAS WRITE Latency (CWL)

CAS write latency (CWL) is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal write to the latching of the first data in. CWL must be correctly set to the corresponding operating clock frequency (see Figure 17). The overall WRITE latency (WL) is equal to CWL + AL (Figure 18).

Figure 18: CAS WRITE Latency



AUTO SELF REFRESH (ASR)

Mode register MR2[6] is used to disable/enable the ASR function. When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1x refresh rate). In the disabled mode, ASR requires the user to ensure the DRAM never exceeds a case temperature (T_C) of 85°C while in self refresh, unless the user enables the SRT function when T_C is between 85°C and 95°C.

Enabling ASR assumes the DRAM self refresh rate is changed automatically from 1x to 2x when T_C exceeds 85°C. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode.

SELF REFRESH TEMPERATURE (SRT)

Mode register MR2[7] is used to disable/enable the SRT function. When SRT is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85°C limit (sometimes referred to as 1x refresh rate). In the disabled mode, SRT requires the user to ensure the DRAM never exceeds a T_C of 85°C while in self refresh mode, unless the user enables ASR.

When SRT is enabled, the DRAM self refresh is changed internally from 1x to 2x, regardless of T_C. This enables the user to operate the DRAM beyond the standard 85°C limit up to the optional extended temperature range of 95°C while in self refresh mode. The standard self refresh current test specifies test conditions for normal T_C (85°C) only, meaning that if SRT is enabled, the standard self refresh current specifications do not apply.

SRT versus ASR

If the normal TC limit of 85°C is not exceeded, then neither SRT nor ASR is required, and both can be disabled throughout operation. However, if the extended temperature option of 105°C is needed, the user is required to provide a 2x refresh rate during manual refresh and to enable either the SRT or the ASR to ensure self refresh is performed at the 2x rate. SRT forces the DRAM to switch the internal self refresh rate from 1x to 2x. Self refresh is performed at the 2x refresh rate regardless of the case temperature.

ASR automatically switches the DRAM's internal self refresh rate from 1x to 2x. However, while in self refresh mode, ASR enables the refresh rate to automatically adjust between 1x and 2x over the supported temperature range. One other disadvantage of ASR is the DRAM cannot always switch from a 1x to 2x refresh rate at an exact TC of 85°C. Although the DRAM will support data integrity when it switches from a 1x to 2x refresh rate, it may switch at a temperature lower than 85°C.

Since only one mode is necessary, SRT and ASR cannot be enabled at the same time.

Dynamic On-Die Termination (ODT)

The dynamic ODT (RTT(WR)) feature is defined by MR2 [10, 9]. Dynamic ODT is enabled when a value is selected for the dynamic ODT resistance RTT(WR). This new DDR3 SDRAM feature enables the ODT termination resistance value to change without issuing an MRS command, essentially changing the ODT termination on-the-fly.

With dynamic ODT (RTT(WR)) enabled, the DRAM switches from nominal ODT (RTT,nom) to dynamic ODT (RTT(WR)) when beginning a WRITE burst, and subsequently switches back to normal ODT (RTT,nom) at the completion of the WRITE burst. If RTT,nom is disabled, the RTT,nom value will be High-Z. Special timing parameters must be adhered to when dynamic ODT (RTT(WR)) is enabled: ODTLcnw, ODTLcwn4, ODTLcwn8, ODTH4, ODTH8, and tADC.

Dynamic ODT is only applicable during WRITE cycles. If normal ODT (RTT,nom) is disabled, dynamic ODT (RTT(WR)) is still permitted. RTT,nom and RTT(WR) can be used independent of one another. Dynamic ODT is not available during write leveling mode, regardless of the state of ODT (RTT,nom).

Table 8: Auto/Self Refresh Mode Register Description

Field	Bits	Description
ASR	MR2 (A6)	Auto Self-Refresh (ASR) when enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation 0 = Manual SR Reference (SRT) 1 = ASR enable
SRT	MR2 (A7)	Self-Refresh Temperature (SRT) Range If ASR = 0, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation If ASR = 1, SRT bit must be set to 0b 0 = Normal operating temperature range 1 = Extended operating temperature range

Self-Refresh Temperature Range Mode Summary

Table 9: Self-Refresh Mode

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0 to 85 ºC)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal (0 to 85 ºC) and Extended (85 to 105 ºC)
1	0	ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-Refresh power consumption is temperature dependent	Normal (0 to 85 ºC)
1	0	ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-Refresh power consumption is temperature dependent	Normal (0 to 85 ºC) and Extended (85 to 105 ºC)
1	1	Illegal	

Mode Register 3 (MR3)

The mode register 3 (MR3) controls additional features and functions not available in the other mode registers. Currently defined is the MULTIPURPOSE REGISTER (MPR). This function is controlled via the bits shown in the Figure 19. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed again or operates in normal mode. However, if MR3[2] = 1, then the DRAM no longer outputs normal read data but outputs MPR data as defined by MR3[0, 1]. If MR3[0, 1] = 00, then a predefined read pattern for system calibration is selected.

Figure 19: Mode Register 3 (MR3) Definition

BA2	BA1	BA0	A15-A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	1	**0*1**											MPR	MPR Loc		Mode Register 3

MRP Operation

A2	MPR
0	Normal operation *3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern *2
0	1	RFU
1	0	RFU
1	1	RFU

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	**1**	**MR3**

* 1 : A3 - A15 must be programmed to 0 during MRS.
* 2 : The predefined pattern will be used for read synchronization.
* 3 : When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.

MULTIPURPOSE REGISTER (MPR)

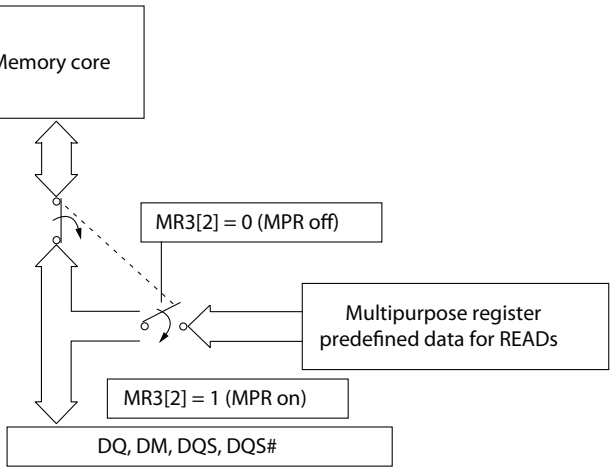
The MULTIPURPOSE REGISTER (MPR) function is used to output a predefined system timing calibration bit sequence. Bit 2 is the master bit that enables or disables access to the MPR register, and bits 1 and 0 determine which mode the MPR is placed in. The basic concept of the multipurpose register is shown in Figure 20.

If MR3[2] = 0, then MPR access is disabled, and the DRAM

until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided it is reprogrammed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress, and the controller must wait the specified time ^{t}MRD and ^{t}MOD before initiating a subsequent operation.

To enable the MPR, the MRS command is issued to MR3, and MR3[2] = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks are precharged, and tRP is met). When the MPR is enabled, any subsequent READ or RDAP commands are redirected to the multipurpose register. The resulting operation when a READ or RDAP command is issued, is defined by MR3[1:0] when the MPR is enabled (see Table 23). When the MPR is enabled, only READ or RDAP commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3[2] = 0). Power-down mode, self refresh, and any other non-READ/RDAP commands are not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Figure 20: MPR Block Diagram



Notes:

1. A predefined data pattern can be read out of the MPR with an external READ command.
2. MR3[2] defines whether the data flow comes from the memory core or the MPR. When the data flow is defined, the MPR contents can be read out continuously with a regular READ or RDAP command.

Table 10: MPR Functional Description of MR3 Bits

MR3[2]	MR3[1:0]	Function
MPR	MPR READ Function	
0	"Don't Care"	Normal operation, no MPR transaction. All subsequent READs come from the DRAM memory array. All subsequent WRITEs go to the DRAM memory array.
1	A[1:0] (see Table 23)	Enable MPR mode, subsequent READ/RDAP commands defined by bits 1 and 2

MPR Functional Description

The JEDEC MPR definition enables either a prime DQ (DQ0 on x4 and x8; on x16, DQ0 = lower byte and DQ8 = upper byte) to output the MPR data with the remaining DQ driven LOW, or all DQ to output the MPR data. The MPR readout supports fixed READ burst and READ burst chop (MRS and OTF via A12/BC#) with regular READ latencies and AC timings applicable, provided the DLL is locked as required.

MPR addressing for a valid MPR read is as follows:

- A[1:0] must be set to 00 as the burst order is fixed per nibble.
- A2 selects the burst order: BL8, A2 is set to 0, and the burst order is fixed to 0, 1, 2, 3, 4, 5, 6, 7.
- For burst chop 4 cases, the burst order is switched on the nibble base along with the following:
  - A2 = 0; burst order = 0, 1, 2, 3
  - A2 = 1; burst order = 4, 5, 6, 7
- Burst order bit 0 (the first bit) is assigned to LSB, and burst order bit 7 (the last bit) is assigned to MSB.
- A[9:3] are "Don't Care."
- A10 is "Don't Care."
- A11 is "Don't Care."
- A12: Selects burst chop mode on-the-fly, if enabled within MR0.
- A13 is a "Don't Care"
- BA[2:0] are "Don't Care."

MPR Address Definitions and Bursting Order

The MPR currently supports a single data format. This data format is a predefined read pattern for system calibration. The predefined pattern is always a repeating 01 bit pattern.

Table 11: MPR Readouts and Burst Order Bit Mapping

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1	00	Read predefined pattern for system Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1	01	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1	10	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1	11	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7

NOTE: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent

MPR Read Predefined Pattern

The predefined read calibration pattern is a fixed pattern of 01010101. The following is an example of using the predetermined read calibration pattern. The example is to perform multiple reads from the MPR to do system-level read timing calibration based on the predefined standard pattern.

The following protocol outlines the steps used to perform the read calibration:

1. Precharge all banks.
2. After ^{t}RP is satisfied, set MRS, MR3[2] = 1 and MR3[1:0] = 00. This redirects all subsequent reads and loads the predefined pattern into the MPR. As soon as ^{t}MRD and ^{t}MOD are satisfied, the MPR is available.
3. Data WRITE operations are not allowed until the MPR returns to the normal DRAM state.
4. Issue a READ with burst order information (all other address pins are “Don’t Care”):
   - A[1:0] = 00 (data burst order is fixed starting at nibble)
   - A2 = 0 (for BL8, burst order is fixed as 0, 1, 2, 3, 4, 5, 6, 7)
   - A12 = 1 (use BL8)
5. After RL = AL + CL, the DRAM bursts out the predefined read calibration pattern (01010101).
6. The memory controller repeats the calibration reads until read data capture at memory controller is optimized.
7. After the last MPR read burst and after tMPRR has been satisfied, issue MRS, MR3[2] = 0, and MR3[1:0] = “Don’t Care” to the normal DRAM state. All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
8. When ^{t}MRD and ^{t}MOD are satisfied from the last MRS, the regular DRAM commands (such as activating a memory bank for regular read or write access) are permitted.

MODE REGISTER SET (MRS) Command

The mode registers are loaded via inputs BA[2:0], A[13:0]. BA[2:0] determine which mode register is programmed:

- BA2 = 0, BA1 = 0, BA0 = 0 for MR0
- BA2 = 0, BA1 = 0, BA0 = 1 for MR1
- BA2 = 0, BA1 = 1, BA0 = 0 for MR2
- BA2 = 0, BA1 = 1, BA0 = 1 for MR3

The MRS command can only be issued (or re-issued) when all banks are idle and in the precharged state (^{t}RP is satisfied and no data bursts are in progress). The controller must wait the specified time ^{t}MRD before initiating a subsequent operation such as an ACTIVATE command. There is also a restriction after issuing an MRS command with regard to when the updated functions become available. This parameter is specified by ^{t}MOD. Violating either of these requirements will result in unspecified operation.

ZQ CALIBRATION Operation

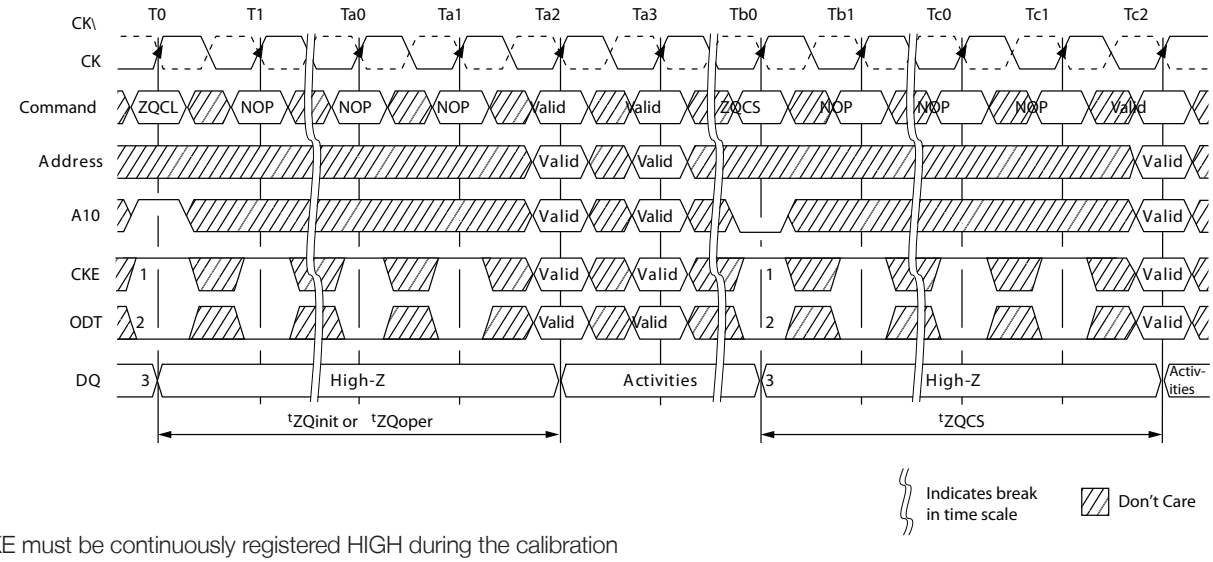
The ZQ CALIBRATION command is used to calibrate the DRAM output drivers (R_{ON}) and ODT values (R_{TT}) over process, voltage, and temperature, provided a dedicated 240Ω(±1%) external resistor is connected from the DRAM's ZQ ball to V_{SSQ}.

DDR3 SDRAM require a longer time to calibrate R_{ON} and ODT at power-up initialization and self refresh exit, and a relatively shorter time to perform periodic calibrations. DDR3 SDRAM defines two ZQ CALIBRATION commands: ZQCL and ZQCS. An example of ZQ calibration timing is shown below.

All banks must be precharged and ^{t}RP must be met before ZQCL or ZQCS commands can be issued to the DRAM. No other activities (other than issuing another ZQCL or ZQCS command) can be performed on the DRAM channel by the controller for the duration of ^{t}ZQinit or ^{t}ZQoper. The quiet time on the DRAM channel helps accurately calibrate RON and ODT. After DRAM calibration is achieved, the DRAM should disable the ZQ ball's current consumption path to reduce power.

ZQ CALIBRATION commands can be issued in parallel to DLL RESET and locking time. Upon self refresh exit, an explicit ZQCL is required if ZQ calibration is desired.

Figure 21: ZQ CALIBRATION Timing (ZQCL and ZQCS)



Notes:

1. CKE must be continuously registered HIGH during the calibration procedure.
2. ODT must be disabled via the ODT signal or the MRS during the calibration procedure.
3. All devices connected to the DQ bus should be High-Z during calibration.

ACTIVATE Operation

Before any READ or WRITE commands can be issued to a bank within the DRAM, a row in that bank must be opened (activated). This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row, subject to the tRCD specification. However, if the additive latency is programmed correctly, a READ or WRITE command may be issued prior to tRCD (MIN). In this operation, the DRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank, but prior to tRCD (MIN) with the requirement that (ACTIVATE-to-READ/WRITE) + AL ≥ tRCD (MIN) (see Posted CAS Additive Latency). tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles.

When at least one bank is open, any READ-to-READ command delay or WRITE-to-WRITE command delay is restricted to tCCD (MIN). A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by tRC.

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by tRRD. No more than four bank ACTIVATE commands may be issued in a given tFAW (MIN) period, and the tRRD (MIN) restriction still applies. The tFAW (MIN) parameter applies, regardless of the number of banks already opened or closed.

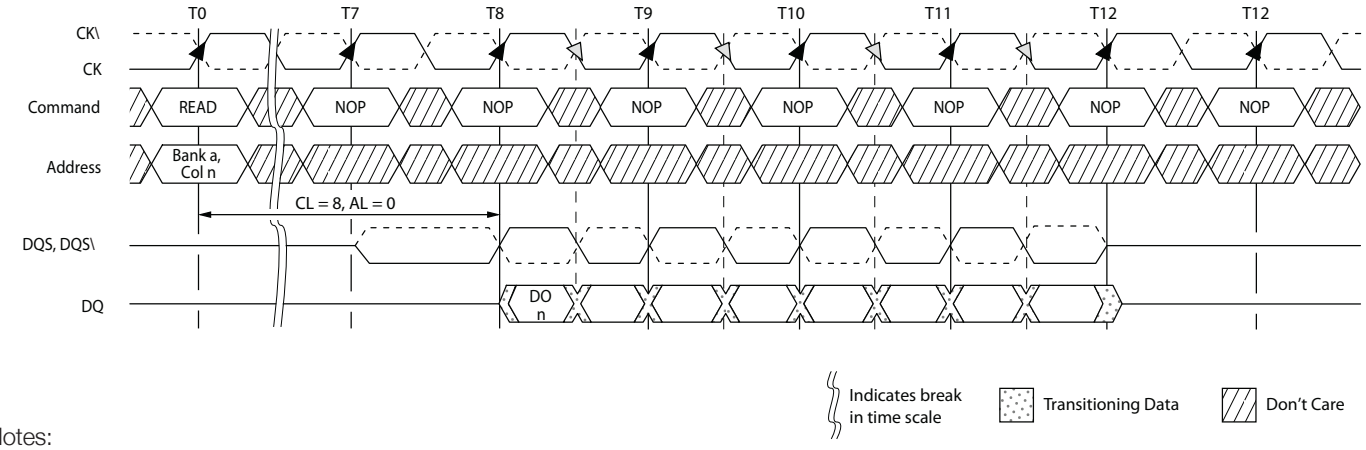
READ Operation

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access.

If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst. During READ bursts, the valid data-out element from the starting column address is available, READ latency (RL) clocks later. RL is defined as the sum of posted CAS additive latency (AL) and CAS latency (CL) (RL = AL + CL). The value of AL and CL is programmable in the mode register via the MRS command. Each subsequent data-out element is valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK\). Figure 19 shows an example of RL based on a CL setting of 8 and an AL setting of 0.

READ Operation (continued)

Figure 22: READ Latency



Notes:

1. DO n = data-out from column *n*.
2. Subsequent elements of data-out appear in the programmed order following DO *n*.

DQS, DQS\ is driven by the DRAM along with the output data. The initial LOW state on DQS and HIGH state on DQS\ is known as the READ preamble (^{t}RPRE). The LOW state on DQS and the HIGH state on DQS\, coincident with the last data-out element, is known as the READ postamble (^{t}RPST). Upon completion of a burst, assuming no other commands have been initiated, the DQ goes High-Z.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued ^{t}CCD cycles after the first READ command. If BC4 is enabled, ^{t}CCD must still be met, which will cause a gap in the data output. DDR3 SDRAM does not allow interrupting or truncating any READ burst.

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. To ensure the READ data is completed before the WRITE data is on the bus, the minimum READ-to-WRITE timing is RL + ^{t}CCD - WL + 2^{t}CK.

A READ burst may be followed by a PRECHARGE command to the same bank, provided auto precharge is not activated. The minimum READ-to-PRECHARGE command spacing to the same bank is four clocks and must also satisfy a minimum analog time from the READ command. This time is called ^{t}RTP (READ-to-PRECHARGE). ^{t}RTP starts AL cycles later than the READ command. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. The PRECHARGE command followed by another PRECHARGE command to the same bank is allowed. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

If A10 is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The DRAM starts an auto precharge operation on the rising edge, which is AL + ^{t}RTP cycles after the READ command. DRAM support a ^{t}RAS lockout feature. If ^{t}RAS (MIN) is not satisfied at the edge, the starting point of the auto precharge operation will be delayed until ^{t}RAS (MIN) is satisfied. If ^{t}RTP (MIN) is not satisfied at the edge, the starting point of the auto precharge operation is delayed until ^{t}RTP (MIN) is satisfied. In case the internal precharge is pushed out by ^{t}RTP, ^{t}RP starts at the point at which the internal precharge happens (not at the next rising clock edge after this event). The time from READ with auto precharge to the next ACTIVATE command to the same bank is AL + (^{t}RTP + ^{t}RP)*, where * means rounded up to the next integer. In any event, internal precharge does not start earlier than four clocks after the last 8*n*-bit prefetch.

Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while an MRS, MPR, ZQCAL, READ, or WRITE operation is in progress. CKE is allowed to go LOW while any of the other legal operations (such as ROW ACTIVATION, PRECHARGE, auto precharge, or REFRESH) are in progress. However, the power-down I_{CC} specifications are not applicable until such operations have completed. Depending on the previous DRAM state and the command issued prior to CKE going LOW, certain timing constraints must be satisfied.

Entering power-down disables the input and output buffers, excluding CK, CK\, ODT, CKE, and RST\. NOP or DES commands are required until ^{t}CPDED has been satisfied, at which time all specified input/output buffers are disabled. The DLL should be in a locked state when power-down is entered for the fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation as well as synchronous ODT operation.

During power-down entry, if any bank remains open after all in-progress commands are complete, the DRAM will be in active power-down mode. If all banks are closed after all in-progress commands are complete, the DRAM will be in precharge power-down mode. Precharge power-down mode must be programmed to exit with either a slow exit mode or a fast exit mode. When entering precharge power-down mode, the DLL is turned off in slow exit mode or kept on in fast exit mode.

The DLL also remains on when entering active power-down. ODT has special timing constraints when slow exit mode precharge power-down is enabled and entered.

While in either power-down state, CKE is held LOW, RST\ is held HIGH, and a stable clock signal must be maintained. ODT must be in a valid state but all other input signals are “Don’t Care.” If RST\ goes LOW during power-down, the DRAM will switch out of power-down mode and go into the reset state. After CKE is registered LOW, CKE must remain LOW until ^{t}PD (MIN) has been satisfied. The maximum time allowed for powerdown duration is ^{t}PD (MAX) (9 × ^{t}REFI).

The power-down states are synchronously exited when CKE is registered HIGH (with a required NOP or DES command). CKE must be maintained HIGH until ^{t}CKE has been satisfied. A valid, executable command may be applied after power-down exit latency, ^{t}XP, and ^{t}XPDLL have been satisfied. A summary of the power-down modes is listed below.

For specific CKE-intensive operations, such as repeating a power-down-exit-to-refresh-to-power-down-entry sequence, the number of clock cycles between power-down exit and power-down entry may not be sufficient to keep the DLL properly updated. In addition to meeting ^{t}PD when the REFRESH command is used between power-down exit and power-down entry, two other conditions must be met. First, ^{t}XP must be satisfied before issuing the REFRESH command. Second, ^{t}XPDLL must be satisfied before the next power-down may be entered.

Electrical Specifications - Absolute Ratings

Stresses greater than those listed in Table 12 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 12: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	V_{CC} supply voltage relative to V_{SS}	-0.4	1.975	V	1
V_{IN}, V_{OUT}	Voltage on any ball relative to V_{SS}				
T_C	Industrial	-40	+85	°C	
	Extended	-40	+105	°C	
	Mil-Temp	-55	+125	°C	
T_{STG}	Storage temperature	-55	+150	°C	

Table 13: iPEM Thermal Resistance

Description	Symbol	Typical	Units	Notes
Junction to Ball	ΘJB	4.5	°C/W	**2**
Junction to Case (Top)	ΘJC	2.2		

The JEDEC JESD51 specifications are used as the default modeling environment and conditions. Using the JESD51 defined 2s2p substrate, horizontal component mounting, published material properties, the thermal characteristics of the module are derived. Application conditions vary and will most likely differ from the JESD51, 2s2p board definition specifications. Micross Components recommends your application and thermal resistances be fully evaluated.

Notes:

1. V_{CC} = VCCQ, and V_{REF} must not be greater than 0.6 x V_{CC}. When V_{CC} is <500mV, V_{REF} can be ≤300mV.
2. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.

DC Operating Conditions

Table 14: DC Electrical Characteristics and Operating

Conditions All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
Supply voltage	V_{CC}	1.283	1. 35	1.45	V	1,2
I/O Supply voltage	V_{CC}					
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{CC}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (all other pins not under test = 0V)	I_I	-10		10	µA	
V_{REF} supply leakage current V_{REFDQ} = V_{CC}/2 or V_{REFCA} = V_{CC}/2 (all other pins not under test = 0V)	I_{VREF}	5		5		4

Notes:

1. V_{CCQ}=V_{CC}, V_{SSQ}=V_{SS}. Core and IO supplies are tied together on device.
2. V_{CC} may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{CC} must be at same level for valid AC timing parameters.
3. V_{REF} (see Table 6).
4. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.

Input Operating Conditions

Table 15: DC Electrical Characteristics and Input Conditions

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
V_{IN} low; DC/commands/address busses	V_{IL}	V_{SS}		See Table 7	V	
V_{IN} high; DC/commands/address busses	V_{IH}	See Table 7		V_{CC}		
Input reference voltage command/address bus	$V_{REFCA(DC)}$	0.49 × V_{CC}	0.5 × V_{CC}	0.51 × V_{CC}		1, 2
I/O reference voltage DQ bus	$V_{REFCA(DC)}$					2, 3
I/O reference voltage DQ bus in SELF REFRESH	$V_{REFDQ(SR)}$	V_{SS}		V_{CC}		4
Command/address termination voltage (system level, not direct DRAM input)	VTT		0.5 × V_{CCQ}			5

Notes:

1. $V_{REFCA(DC)}$ is expected to be approximately 0.5 × V_{CC} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFCA} may not exceed ±1% × V_{CC} around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed ±2% of $V_{REFCA(DC)}$.
2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
3. $V_{REFDQ(DC)}$ is expected to be approximately 0.5 × V_{CC} and to track variations in the DC level. Externally generated peak noise (noncommon mode) on V_{REFDQ} may not exceed ±1% × V_{CC} around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed ±2% of $V_{REFDQ(DC)}$.
4. $V_{REFDQ(DC)}$ may transition to $V_{REFDQ(SR)}$ and back to $V_{REFDQ(DC)}$ when in SELF REFRESH,within restrictions outlined in the SELF REFRESH section.
5. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. Minimum and maximum values are system-dependent.

Table 16: Input Switching Conditions

Parameter/Condition	Symbol	DDR3-800	DDR3-1066	DDR3-1333/1600	Units
Command and Address					
Input high AC voltage: Logic 1 @ 175mV	$V_{IH(AC160)min}$	160	160	160	mV
Input high AC voltage: Logic 1 @ 150mV	$V_{IH(AC135)min}$	135	135	135	
Input high DC voltage: Logic 1 @ 100 mV	$V_{IH(DC90)min}$	90	90	90	
Input low DC voltage: Logic 0 @ –100mV	$V_{IL(DC90)max}$	-90	-90	-90	
Input low AC voltage: Logic 0 @ –150mV	$V_{IL(AC135)max}$	-135	-135	-135	
Input low AC voltage: Logic 0 @ –175mV	$V_{IL(AC160max}$	-160	-160	-160	
DQ and DM					
Input high AC voltage: Logic 1	$V_{IH(AC160)min}$	160	160	160	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}$	135	135	135	
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	
Input low DC voltage: Logic 0	$V_{IL(DC90)max}$	-90	-90	-90	
Input low AC voltage: Logic 0	$V_{IL(AC135)max}$	-135	-135	-165	
Input low AC voltage: Logic 0	$V_{IL(AC160)max}$	-160	-160	-160	

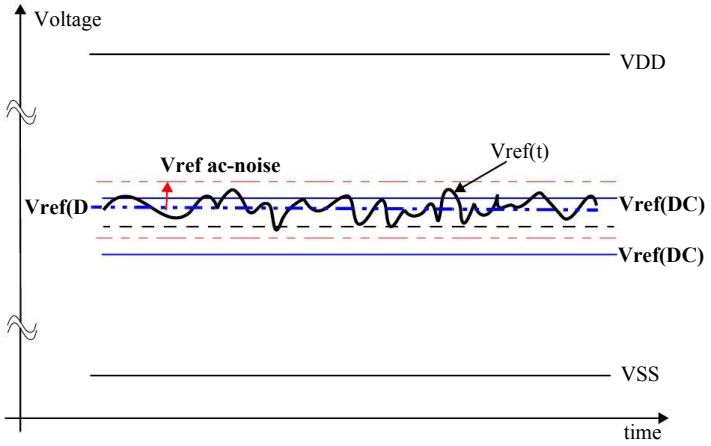
Notes:

1. All voltages are referenced to V_{REF}. V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
2. Input setup timing parameters (^{t}IS and ^{t}DS) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
3. Input hold timing parameters (^{t}IH and ^{t}DH) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).
5. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs. For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH\ AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/command inputs must use either $V_{IH(AC175),min}$ with ^{t}IS AC175) of 200ps or $V_{IH(AC150),min}$ with ^{t}IS(AC150) of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with ^{t}DS(AC175) of 75ps or $V_{IH(AC150),min}$ with ^{t}DS(AC150) of 125ps.

V-REF Tolerances

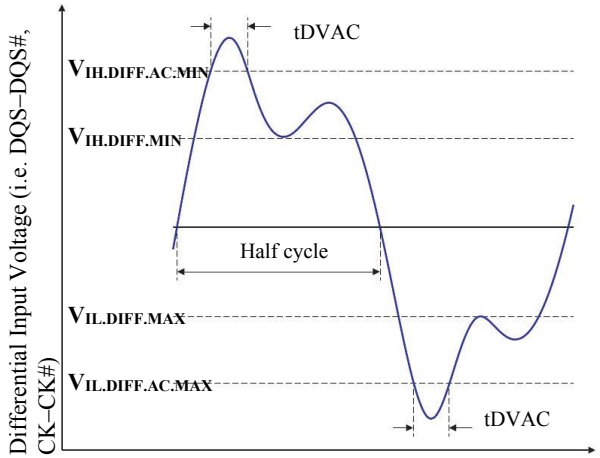
The DC-tolerance limits and AC-Noise limits for the reference voltages VrefCA and VrefDQ are illustrated in the following figure. It shows a valid reference voltage Vref(t) as a function of time. Vref(DC) is the linear average of Vref(t) over a very long period of time (e.g., 1 sec.). This average has to meet the min/max requirement . Furthermore, Vref(t) may temporarily deviate from Vref(DC) by no more than +/- 1% VDD. The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on Vref. "Vref" shall be understood as Vref(DC). This states that DC variations of Vref affect the absolute voltage a signal has to reach to achieve a valid HIGH or LOW level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for Vref(DC) deviations from the optimum position within the data-eye of the input signals. This also clarifies that the DRAM setup and hold specification and derating values need to include time/voltage offsets associated with Vref(AC) noise.

Figure 23: Vref(DC) tolerance and Vref(AC) noise limits



Differential Signal Definition

Figure 24: Definition of differential ac-swing and “time above ac-level”



Single Ended requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#) has also to comply with certain requirements for single-ended signals. CK and CK# have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(ac) / VIL(ac)) for ADD/CMD signals) in every half-cycle. DQS, DQSL, DQSU, DQS#, DQSL# have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH(ac) / VIL(ac)) for DQ signals) in every half-cycle preceding and following a valid transition.

Table 17: Single-ended levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#

Symbol	Parameter	DDR3/DDR3L-800, 1066, 1333, & 1600		Unit	Notes
		Min	Max		
VSEH	Single-ended high-level for strobes	(VDDQ/2) + 0.175	note3	V	1, 2
	Single-ended high-level for CK, CK	(VDDQ/2) + 0.175	note3	V	1, 2
VSEL	Single-ended low-level for strobes	note3	(VDDQ/2) - 0.175	V	1, 2
	Single-ended Low-level for CK, CK	note3	(VDDQ/2) - 0.175	V	1, 2

Notes:
1. For CK, CK# use VIH/VIL(ac) of ADD/CMD; for strobes (DQS, DQS#, DQSL, DQSL#, DQSU, DQSU#) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

Differential Input Cross-Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK and DQS, DQS) must meet the requirements in the following table. The differential input cross point voltage Vix is measured from the actual cross point of true and completement signal to the midlevel between of VDD and VSS.

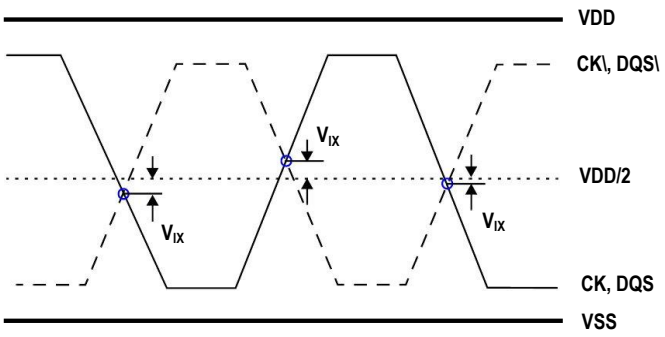


Table 18: Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter		DDR3/DDR3L-800, 1066, 1333, 1600, 1866, 2133		Unit	Note
			Min.	Max.		
Vix	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK	DDR3	-150	150	mV	2
			-175	175	mV	1
		DDR3L	-150	150	mV	2
	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS	DDR3	-150	150	mV	2
		DDR3L	-150	150	mV	2

Notes:
1. Extended range for Vix is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - CK# is larger than 3 V/ns.
2. The following must be true: $(V_{DD}/2) + Vix(min) - V_{SEL} \geq 25$ mV and $V_{SEH} - ((V_{DD}/2) + Vix(max.)) \geq 25$mV.

Slew-Rate Definition, Single Ended Input Signals

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value . If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to VREF (dc) level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF (dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition, a valid input signal is still required to complete the transition and reach VIH/IL(ac). For slew rates in between the values listed in the tables, the derating values may obtained by linear interpolation.

Figure 25: Differential Input Slew Rate for DQS, DQS\, CK & CK\

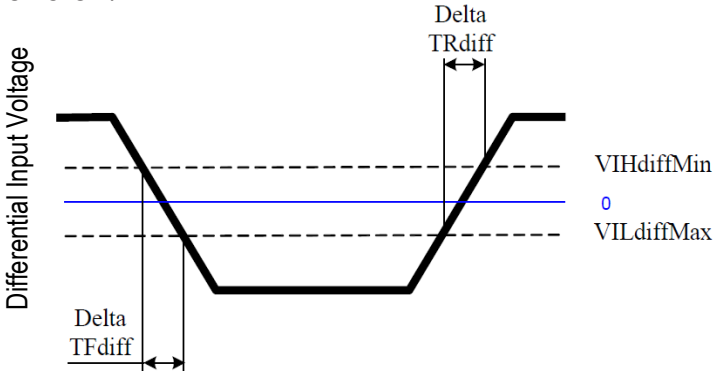


Table 19: Differential Input Slew Rate

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-CK# & DQS-DQS#)	VILdiffmax	VIHdiffmin	[VIHdiffmin-VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK-CK# & DQS-DQS#)	VIHdiffmin	VILdiffmax	[VIHdiffmin-VILdiffmax] / DeltaTFdiff

Note : The differential signal (i.e., CK-CK# & DQS-DQS#) must be linear between these thresholds.

Table 20: Single Ended AC and DC output Levels

Symbol	Parameter	Value	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8xVDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5xVDDQ	V	
VOL(DC)	DC output low measurement level (fro IV curve linearity)	0.2xVDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT+0.1xVDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT-0.1xVDDQ	V	1

NOTE 1. The swing of ± 0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2.

Table 21: Differential AC and DC Output levels

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC)-VOL(AC)] / DeltaTRse
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC)-VOL(AC)] / DeltaTFse

Figure 26: Single Ended Output Slew Rate

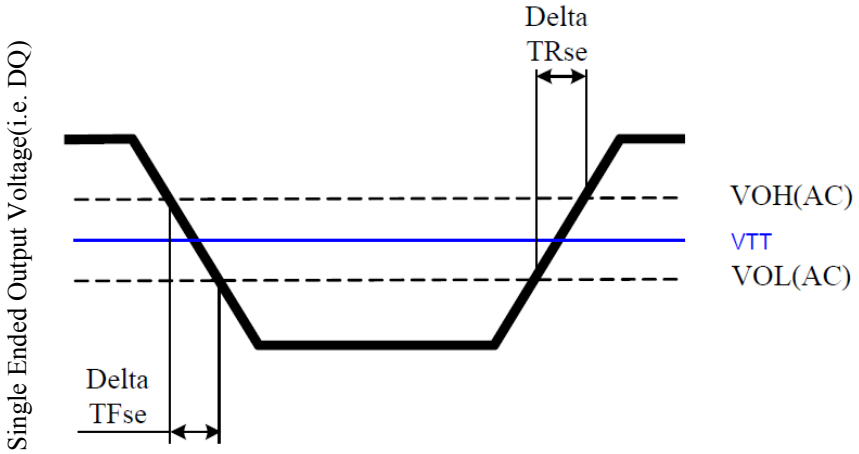


Table 22: Single Ended AC and DC output Levels

Parameter		Symbol	DDR-800		DDR-1066		DDR3-1333		DDR3-1600		DDR3-1866		DDR3-2133		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Single-ended Output Slew Rate	DDR3	SRQse	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5	V/ns
	DDR3L		1.75	5	1.75	5	1.75	5	1.75	5	1.75	5	1.75	5	

Table 23: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)]/DeltaTRdiff
Differential output slew rate for falling	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)]/DeltaTFdiff

Note: Output slew rate is verified by design and characterization, and not 100% tested in production.

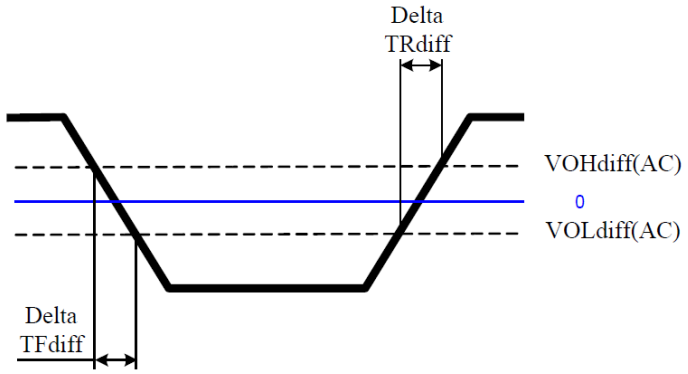


Figure 27: Single Ended Output Slew Rate

Table 24: Differential Output Slew Rate

Parameter		Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Differential Output Slew Rate	DDR3	SRQdiff	5	10	5	10	5	10	5	10	V/ns
	DDR3L		3.5	12	3.5	12	3.5	12	3.5	12	

Description: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: Differential Signals, For Ron = RZQ/7 setting

Reference Load for AC Timing and Output Slew Rate

The following figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements. It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

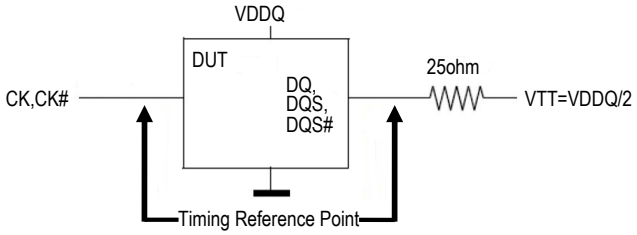


Figure 28: Reference Load for AC Timing and Output Slew Rate

AC Overshoot/Undershoot Specification

Table 25: Control and Address Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure 4)	0.4 V			
Maximum peak amplitude allowed for undershoot area (see Figure 5)				
Maximum overshoot area above V_{CC} (see Figure 4)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns
Maximum undershoot area below V_{SS} (see Figure 5)				

Table 26: Clock, Data, Strobe, and Mask Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure 4)	0.4 V			
Maximum peak amplitude allowed for undershoot area (see Figure 5)				
Maximum overshoot area above V_{CC} (see Figure 4)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns
Maximum undershoot area below V_{SS} (see Figure 5)				

Figure 29: Overshoot

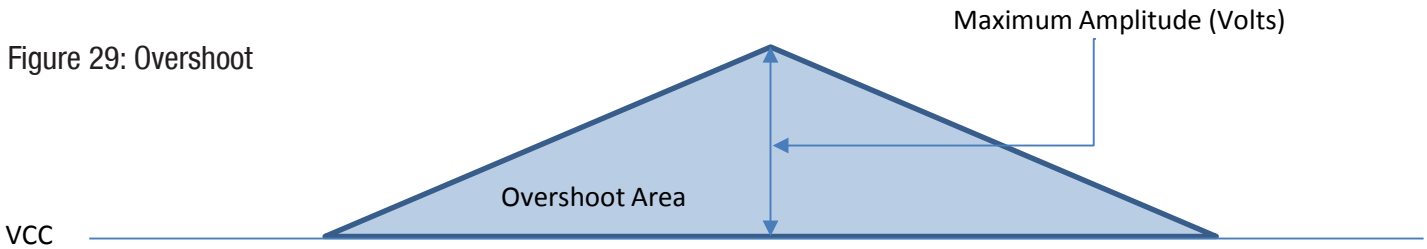
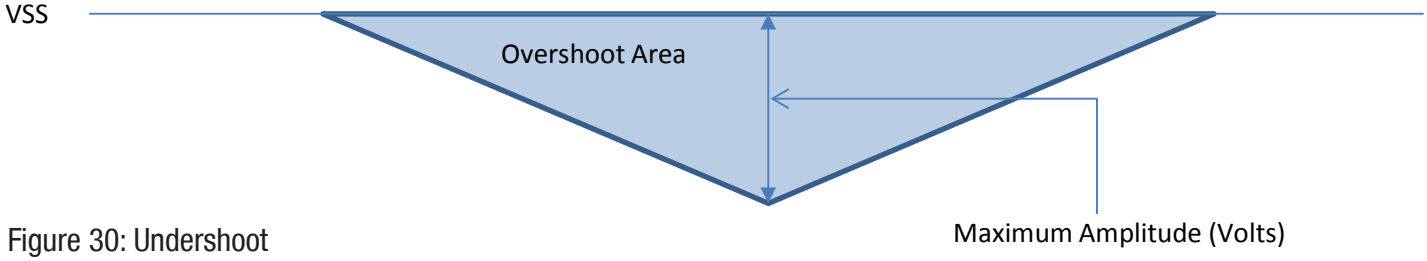


Figure 30: Undershoot



Output Driver DC Characteristics

A Functional representation of the output buffer is shown as below. Output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:
RON34 = RZQ / 7 (nominal 34.4ohms +/-10% with nominal RZQ=240ohms)
The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:
RONPu = [VDDQ-Vout] / | Iout | ---------- under the condition that RONPd is turned off (1)
RONPd = Vout / | Iout | ----------under the condition that RONPu is turned off (2)

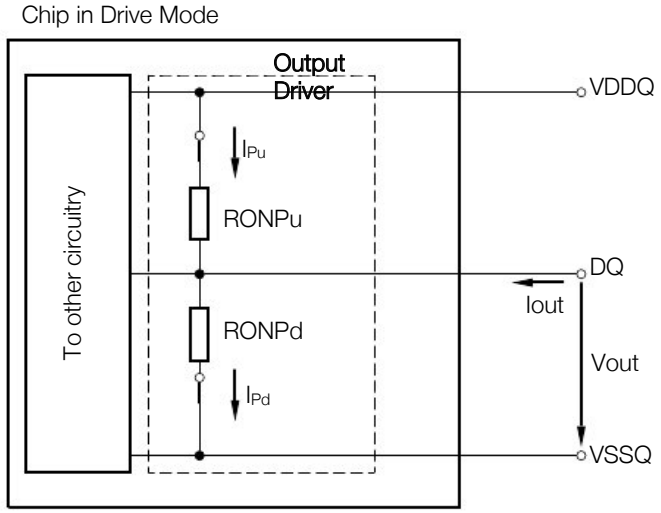


Figure 31: Output Driver: Definition of Voltages and Currents

Table 27: Output Driver DC Electrical Characteristics

DDR3 (assuming 1.5V, RZQ = 240ohms; entire operating temperature range; after proper ZQ calibration)

RONNom	Resistor	Vout	Min	Nom	Max	Unit	Notes
34 ohms	RON34Pd	VOLdc=0.2xVDDQ	0.6	1	1.1	RZQ/7	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.1	RZQ/7	1,2,3
		VOHdc =0.8xVDDQ	0.9	1	1.4	RZQ/7	1,2,3
	RON34Pu	VOLdc=0.2xVDDQ	0.9	1	1.4	RZQ/7	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.1	RZQ/7	1,2,3
		VOHdc=0.8xVDDQ	0.6	1	1.1	RZQ/7	1,2,3
40 ohms	RON40Pd	VOLdc=0.2xVDDQ	0.6	1	1.1	RZQ/6	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.1	RZQ/6	1,2,3
		VOHdc =0.8xVDDQ	0.9	1	1.4	RZQ/6	1,2,3
	RON40Pu	VOLdc=0.2xVDDQ	0.9	1	1.4	RZQ/6	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.1	RZQ/6	1,2,3
		VOHdc=0.8xVDDQ	0.6	1	1.1	RZQ/6	1,2,3
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.5xVDDQ	-10		+10	%	1,2,4

Table 28: Output Driver DC Electrical Characteristics

DDR3 (assuming 1.35V, RZQ = 240ohms; entire operating temperature range; after proper ZQ calibration)

RONNom	Resistor	Vout	Min	Nom	Max	Unit	Notes
34 ohms	RON34Pd	VOLdc=0.2xVDDQ	0.6	1	1.15	RZQ/7	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.15	RZQ/7	1,2,3
		VOHdc =0.8xVDDQ	0.9	1	1.45	RZQ/7	1,2,3
	RON34Pu	VOLdc=0.2xVDDQ	0.9	1	1.45	RZQ/7	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.15	RZQ/7	1,2,3
		VOHdc=0.8xVDDQ	0.6	1	1.15	RZQ/7	1,2,3
40 ohms	RON40Pd	VOLdc=0.2xVDDQ	0.6	1	1.15	RZQ/6	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.15	RZQ/6	1,2,3
		VOHdc =0.8xVDDQ	0.9	1	1.45	RZQ/6	1,2,3
	RON40Pu	VOLdc=0.2xVDDQ	0.9	1	1.45	RZQ/6	1,2,3
		VOMdc=0.5xVDDQ	0.9	1	1.15	RZQ/6	1,2,3
		VOHdc=0.8xVDDQ	0.6	1	1.15	RZQ/6	1,2,3
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.5xVDDQ	-10		+10	%	1,2,4

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ=VDD and that VSSQ=VSS.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5xVDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 * VDDQ and 0.8 x VDDQ.
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd:
   Measure RONPu and RONPd, both at 0.5 x VDDQ:
   MMPuPd = [RONPu - RONPd] / RONNom x 100

Output Driver Temperature and Voltage Sensitivity

Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

Table 29: Output Driver Sensitivity Definition

Items	Min.	Max.	Unit
RONPU@VOHdc	0.6 - dRONdTH*|Delta TI - dRONdVH*|Delta VI	1.1 + dRONdTH*|Delta TI - dRONdVH*|Delta VI	RZQ/7
RON@VOMdc	0.9 - dRONdTM*|Delta TI - dRONdVM*|Delta VI	1.1 + dRONdTM*|Delta TI - dRONdVM*|Delta VI	RZQ/7
RONPD@VOLdc	0.6 - dRONdTL*|Delta TI - dRONdVL*|Delta VI	1.1 + dRONdTL*|Delta TI - dRONdVL*|Delta VI	RZQ/7

Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table 30: Output Driver Voltage and Temperature Sensitivity

Speed Bin	DDR3-800/1066/1333		DDR3-1600/1866/2133		Unit
Items	Min.	Max	Min.	Max	
dRONdTM	0	1.5	0	1.5	%/°C
dRONdVM	0	0.15	0	0.13	%/mV
dRONdTL	0	1.5	0	1.5	%/°C
dRONdVL	0	0.15	0	0.13	%/mV
dRONdTH	0	1.5	0	1.5	%/°C
dRONdVH	0	0.15	0	0.13	%/mV

Note: dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6, and A2 of the MR1 Register.
ODT is applied to the DQ, DM, DQS/DQS, and TDQS/TDQS (x8 devices only) pins.
A functional representation of the on-die termination is shown in the following figure. The individual pull-up and pull-down resistors (RTTPu and RTTPd) are defined as follows:
RTTPu = [VDDQ - Vout] / | Iout | ---------- under the condition that RTTPd is turned off (3)
RTTPd = Vout / | Iout | ---------- under the condition that RTTPu is turned off (4)

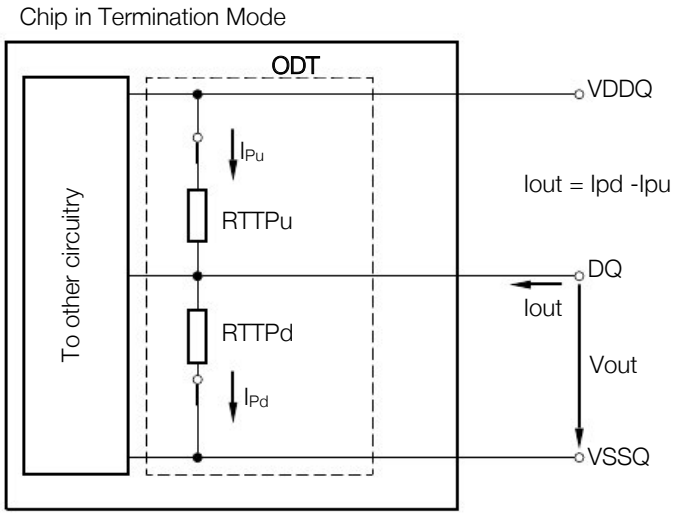


Figure 32: Output Driver: Definition of Voltages and Currents

On-Die Termination (ODT) DC Electrical Characteristics

The following table (Table # 30) provides an overview of the ODT DC electrical characteristics. The values for RTT60Pd120, RTT60Pu120, RTT120Pd240, RTT120Pu240, RTT40Pd80, RTT40Pu80, RTT30Pd60, RTT30Pu60, RTT20Pd40, RTT20Pu40 are not specification requirements, but can be used as design guide lines:

Table 31: ODT Effective Impedance values assuming RZQ = 240 ohm

MR1 A9, A6, A2	RTT	Resistor	Vout	Min	Nom		Max (DDR3L)	Unit	Notes
0,1,0	Ω 120	RTT120Pd240	VOLdc = 0.2 x VDDQ	0.6	1		1.15	RZQ	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1		1.45	RZQ	1,2,3,4
		RTT120Pu240	VOLdc = 0.2 x VDDQ	0.9	1		1.45	RZQ	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1		1.15	RZQ	1,2,3,4
		RTT120	VIL(ac) to VIH(ac)	0.9	1		1.65	RZQ/2	1,2,5
0,0,1	Ω 60	RTT60Pd120	VOLdc = 0.2 x VDDQ	0.6	1		1.15	RZQ/2	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1		1.45	RZQ/2	1,2,3,4
		RTT60Pu120	VOLdc = 0.2 x VDDQ	0.9	1		1.45	RZQ/2	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ/2	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1		1.15	RZQ/2	1,2,3,4
		RTT60	VIL(ac) to VIH(ac)	0.9	1		1.65	RZQ/4	1,2,5
0,1,1	Ω 40	RTT40Pd80	VOLdc = 0.2 x VDDQ	0.6	1		1.15	RZQ/3	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1		1.45	RZQ/3	1,2,3,4
		RTT40Pu80	VOLdc = 0.2 x VDDQ	0.9	1		1.45	RZQ/3	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ/3	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1		1.15	RZQ/3	1,2,3,4
		RTT40	VIL(ac) to VIH(ac)	0.9	1		1.65	RZQ/6	1,2,5
1,0,1	Ω 30	RTT30Pd60	VOLdc = 0.2 x VDDQ	0.6	1		1.15	RZQ/4	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1		1.45	RZQ/4	1,2,3,4
		RTT30Pu60	VOLdc = 0.2 x VDDQ	0.9	1		1.45	RZQ/4	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ/4	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1		1.15	RZQ/4	1,2,3,4
		RTT30	VIL(ac) to VIH(ac)	0.9	1		1.65	RZQ/8	1,2,5
1,0,0	Ω 20	RTT20Pd40	VOLdc = 0.2 x VDDQ	0.6	1		1.15	RZQ/6	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.9	1		1.45	RZQ/6	1,2,3,4
		RTT20Pu40	VOLdc = 0.2 x VDDQ	0.9	1		1.45	RZQ/6	1,2,3,4
			0.5 x VDDQ	0.9	1		1.15	RZQ/6	1,2,3,4
			VOHdc = 0.8 x VDDQ	0.6	1		1.15	RZQ/6	1,2,3,4
		RTT20	VIL(ac) to VIH(ac)	0.9	1		1.65	RZQ/12	1,2,5
Deviation of VM w.r.t VDDQ/2, DVM				-5	-		+5	%	1,2,5,6

Table 31: Notes

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above.
4. Not a specification requirement, but a design guide line.
5. Measurement definition for RTT:
   Apply VIH(ac) to pin under test and measure current I(VIH(ac)), then apply VIL(ac) to pin under test and measure current I(VIL(ac)) respectively.
   RTT = [VIH(ac) - VIL(ac)] / [I(VIH(ac)) - I(VIL(ac))]
6. Measurement definition for VM and DVM:
   Measure voltage (VM) at test pin (midpoint) with no load:
   Delta V_M = [2V_M / VDDQ -1] x 100

On-Die Termination (ODT) Voltage and Temperature Sensitivity

If temperature and/or voltage after calibration, the tolerance limits widen according to the following table.

Delta T = T - T(@calibration); Delta V = VDDQ - VDDQ(@calibration); VDD = VDDQ

Table 32: ODT Sensitivity

	min	max	Unit
RTT	0.9 - dRTTdT*lDelta Tl - dRTTdV*lDelta Vl	1.6 + dRTTdT*lDelta Tl + dRTTdV*lDelta Vl	RZQ/2,4,6,8,12

Table 33: ODT Voltage and Temperature Sensitivity

	Min	Max	Unit
dRTTdT	0	1.5	%/°C
dRTTdV	0	0.15	%/mV

Note: These parameters may not be subject to production test. They are verified by design and characterization

On-Die Termination (ODT) Timing Definition

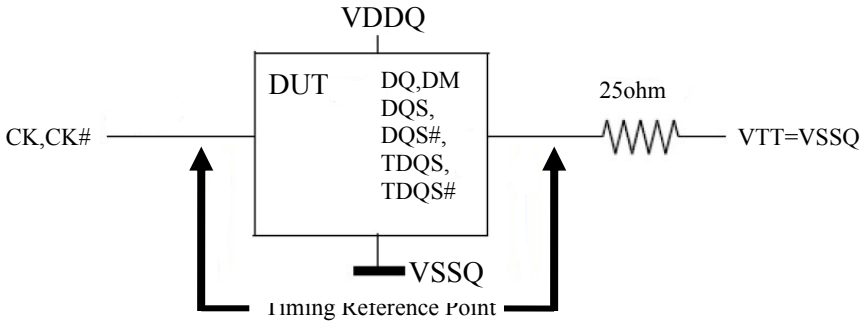


Figure 5.9.1 ODT Timing Reference Load

Figure 33: ODT Timing Reference Load

Table 34: ODT Timing

Symbol	Begin Point Definition	End Point Definition
t_{AON}	Rising edge of CK - CK defined by the end point of ODTLon	Extrapolated point at VSSQ
t_{AONPD}	Rising edge of CK - CK with ODT being first registered high	Extrapolated point at VSSQ
t_{AOF}	Rising edge of CK - CK defined by the end point of ODTLoff	End point: Extrapolated point at V_{RTT_Nom}
t_{AOFPD}	Rising edge of CK - CK with ODT being first registered low	End point: Extrapolated point at V_{RTT_Nom}
t_{ADC}	Rising edge of CK - CK defined by the end point of ODTLcnw, ODTLcwn4, or ODTLcwn8	End point: Extrapolated point at V_{RTT_Wr} and V_{RTT_Nom} respectively

Reference Settings for ODT Timing Measurements

Measured Parameter		RTT_Nom Setting	RTT_Wr Setting	VSW1[V]	VSW2[V]
t_{AON}		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
t_{AONPD}		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
t_{AOFPD}		RZQ/4	NA	0.05	0.10
		RZQ/12	NA	0.10	0.20
t_{ADC}	DDR3	RZQ/12	RZQ/2	0.20	0.30
	DDR3L	RZQ/12	RZQ/2	0.20	0.25

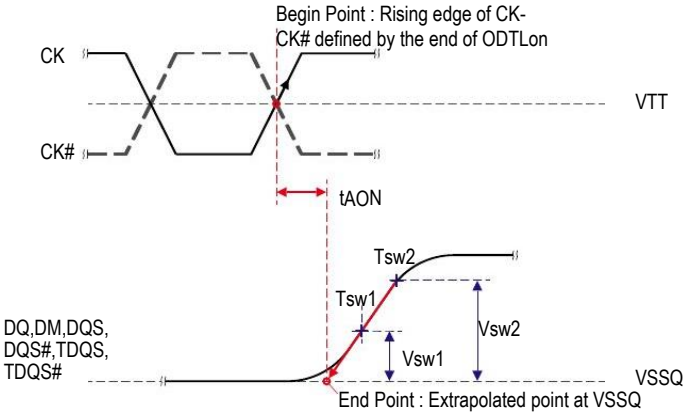


Figure 34: Definition of tAGN

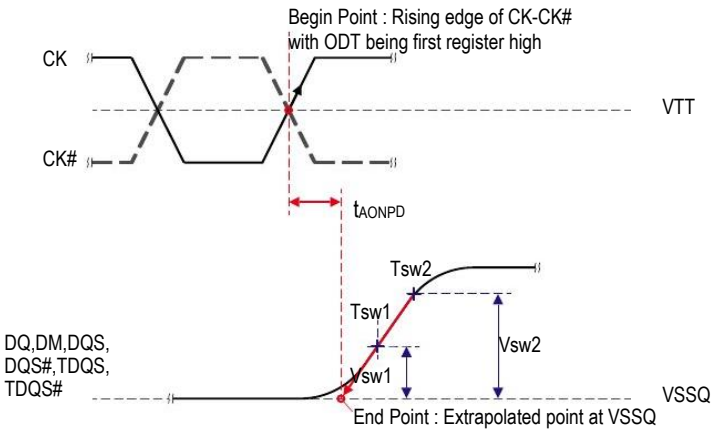


Figure 35: Definition of tAGNPD

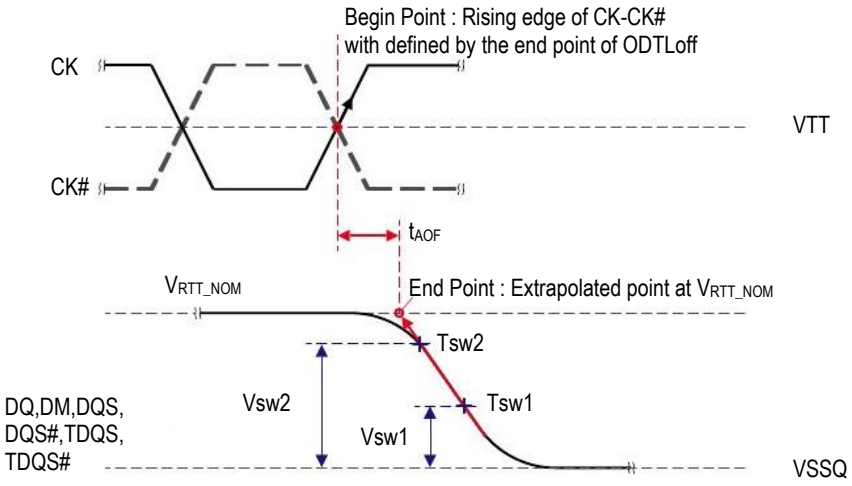


Figure 36: Definition of tADF

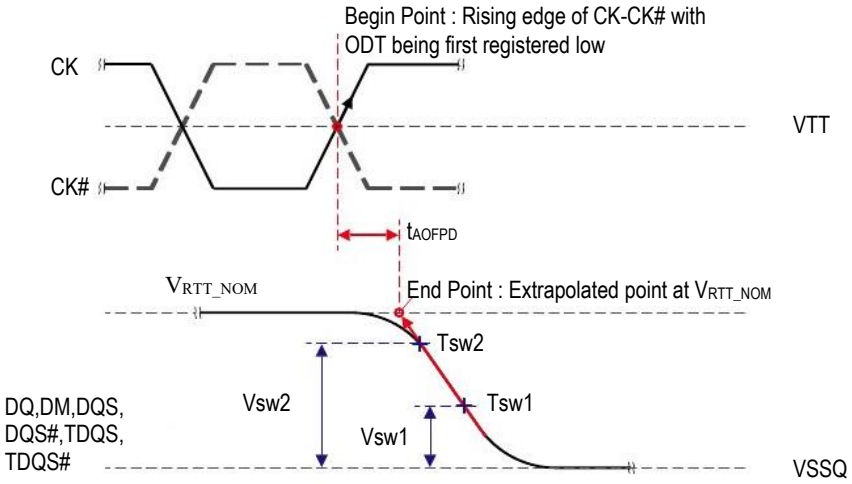


Figure 37: Definition of tAOFPD

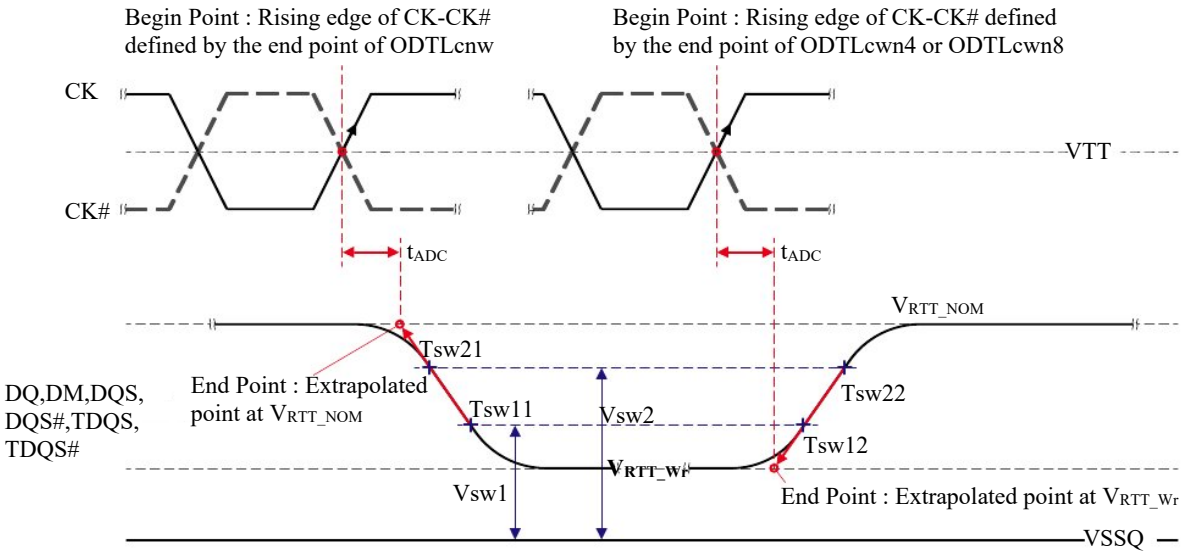


Figure 38: Definition of tADC

Input/Output Capacitance

Table 35: Capacitance Values

Symbol	Parameter		DDR3/ DDR3L-800		DDR3/ DDR3L-1066		DDR3/ DDR3L-1333		DDR3/ DDR3L-1600		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance (DQ, DM, DQS, DQS#,TDQS,TDQS#)	DDR3	1.4	3	1.4	2.7	1.4	2.5	1.4	2.3	pF	1,2,3
		DDR3L	1.4	2.5	1.4	2.5	1.4	2.3	1.4	2.2		
C_{CK}	Input capacitance, CK and CK#		0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2,3
C_{DCK}	Input capacitance delta, CK and CK#		0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
C_{DDQS}	Input/output capacitance delta, DQS and DQS#		0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,5
C_I	Input capacitance, CTRL, ADD, command input-only pins	DDR3	0.75	1.4	0.75	1.35	0.75	1.3	0.75	1.3	pF	2,3,7, 8
		DDR3L	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2		
C_{DI_CTRL}	Input capacitance delta, all CTRL input-only pins		-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	2,3,7, 8
$C_{DI\_ADD\_CMD}$	Input capacitance delta, all ADD/CMD input-only pins		-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	2,3,9, 10
C_{DIO}	Input/output capacitance delta, DQ, DM, DQS, DQS# TDQS,TDQS#		-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
C_{ZQ}	Input/output capacitance of ZQ pin		-	3	-	3	-	3	-	3	pF	2,3,12

Notes:
1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-$C_{CK\#}$
5. Absolute value of C_{IO}(DQS)-C_{IO}(DQS#)
6. C_I applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#,CAS#,WE#.
7. C_{DI_CTRL} applies to ODT, CS# and CKE
8. C_{DI_CTRL}=C_I(CTRL)-0.5*(C_I(CK)+C_I(CK#))
9. $C_{DI\_ADD\_CMD}$ applies to A0-A15, BA0-BA2, RAS#, CAS# and WE#
10. $C_{DI\_ADD\_CMD}$=C_I(ADD_CMD) - 0.5*(C_I(CK)+C_I(CK#))
11. C_{DIO}=C_{IO}(DQ,DM) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS#))
12. Maximum external load capacitance on ZQ pin: 5 pF.

Specifications for I_{DD} Conditions and Limits

Within the following I_{DD} measurement tables, the following definitions and conditions are used, unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(AC)max}$; HIGH: $V_{IN} \geq V_{IH(AC)min}$.
- Midlevel: Inputs are $V_{REF} = V_{DD}/2$.
- R_{ON} set to RZQ/7 (34Ω.)
- $R_{TT,nom}$ set to RZQ/6 (40Ω.)
- $R_{TT(WR)}$ set to RZQ/2 (120Ω.)
- Q_{OFF} is enabled in MR1.
- ODT is enabled in MR1 ($R_{TT,nom}$) and MR2 ($R_{TT(WR)}$).
- TDQS is disabled in MR1.
- External DQ/DQS/DM load resistor is 25Ω to $V_{DDQ}/2$.
- Burst lengths are BL8 fixed.
- AL equals 0 (except in I_{DD7}).
- I_{DD} specifications are tested after the device is properly initialized.
- Input slew rate is specified by AC parametric test conditions.
- Optional ASR is disabled.
- Read burst type uses nibble sequential (MR0[3] = 0).
- Loop patterns must be executed at least once before current measurements begin.

Table 36: Timing Parameters Used for IDD Measurements – Clock Units

I_{DD} Parameter	DDR3L -800	DDR3L -1066	DDR3L -1333	DDR3L -1600	Unit
	-25	-19	-15	-13	
	6-6-6	8-8-8	9-9-9	11-11-11	
^{t}CK (MIN) I_{DD}	2.5	1.875	1.5	1.25	ns
CL I_{DD}	6	8	9	11	CK
^{t}RCD (MIN) I_{DD}	6	8	9	11	CK
^{t}RC (MIN) I_{DD}	21	28	33	39	CK
^{t}RAS (MIN) I_{DD}	15	20	24	28	CK
^{t}RP (MIN)	6	8	9	11	CK
^{t}FAW	20	27	30	32	CK
^{t}RRD I_{DD}	4	6	5	6	CK
^{t}RFC	140	187	234	280	CK

Electrical Characteristics - I_{CC} Specifications

I_{CC} values are for full operating range of voltage and temperature unless otherwise noted.

Table 37: ICC Maximum Limits

Symbol	Conditions	DDR3 800, CL6	DDR3 1066, CL8	DDR3 1333, CL9	DDR3 1600 CL11	Units	Notes
I_{CC0}	Operating Current, one Bank Active Precharge	375	385	405	440	mA	1, 2
I_{CC1}	Operating Current, one Bank Activate, Read, Precharge	420	435	465	505	mA	1, 2
I_{CC2P0} (Slow)	Precharge Power Down current Slow Exit, MR0 bit A12 = 0	165		170		mA	1, 2
I_{CC2P1} (Fast)	Precharge Power Down current Fast Exit, MRO bit A12 = 1	185		195	200	mA	1, 2
I_{CC2Q}	Precharge Quiet Standby current	260	270	285	305	mA	1, 2
I_{CC2N}	Precharge Standby current	270	280	295	320	mA	1, 2
I_{CC2NT}		300		315		mA	1, 2
I_{CC3P}	Active Power Down current, always Fast Exit	250	255	260	280	mA	1, 2
I_{CC3N}	Active Standby current	340	355	375	415	mA	1, 2
I_{CC4R}	Operating Current, Burst Read	500	565	650	750	mA	1, 2
I_{CC4W}	Operating Current, Burst Write	820	735	860	990	mA	1, 2
I_{CC5B}	Burst Refresh current	700	745	760	780	mA	1, 2
I_{CC6}	Self Refresh current: normal temperature range	135				mA	1, 2, 3
I_{CC6ET}	Self Refresh current: extended temperature range	180				mA	2, 4
I_{CC7}	Read current: all banks interleaved	795	825	885	975	mA	1, 2
I_{CC8}		I_{CC2P0} + 10mA				mA	1, 2

Notes:

1. T_C = 85°C; SRT and ASR are disabled.
2. Enabling ASR could increase I_{CCX} by up to an additional 2mA.
3. Restricted to T_C MAX = 85°C.
4. T_C = 85°C; ASR and ODT are disabled; SRT is enabled.
5. The I_{CC} values must be derated (increased) on IT-option devices when operated outside the range 0°C ≤ T_C ≤ +85°C:
   A. When T_C < 0°C: I_{CC2P0}, I_{CC2P1} and I_{CC3P} must be derated by 4%; I_{CC4R} and I_{CC4W} must be derated by 2%; and I_{CC6}, I_{CC6ET} and I_{CC7} must be derated by 7%.

Table 38: Differential Input Operating Conditions (CK, CK\ and DQS, DQS\)

Parameter	Symbol	Min	Max	Unit	Notes
Differential input voltage logic high - slew	$V_{IH,diff}$	180		mV	4
Differential input voltage logic low - slew	$V_{IL,diff}$		-180		
Differential input voltage logic high	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	V_{CC}		5
Differential input voltage logic low	$V_{IL,diff(AC)}$	V_{SS}	$2 \times (V_{IL(AC)}-V_{REF})$		6
Differential input crossing voltage relative to $V_{CC}/2$ for DQS, DQS\; CK, CK\	V_{IX}	$V_{REF(DC)}$ - 150	$V_{REF(DC)}$ + 150		4, 7
Differential input crossing voltage relative to $V_{CC}/2$ for CK, CK\	V_{IX} (175)	$V_{REF(DC)}$ - 175	$V_{REF(DC)}$ + 175		4, 7, 8
Single-ended high level for strobes	V_{SEH}	$V_{CCQ}/2$ + 160	V_{CC}		5
Single-ended high level for CK, CK\					
Single-ended low level for strobes	V_{SEL}	V_{SS}	$V_{CC}/2$ - 160		6
Single-ended low level for CK, CK\					

Notes:

1. Clock is referenced to V_{CC} and V_{SS}. Data strobe is referenced to V_{CC} and V_{SS} as V_{CCQ} is tied to V_{CC} and V_{SSQ} is tied to V_{SS}.
2. Reference is $V_{REFCA(DC)}$ for clock and $V_{REFDQ(DC)}$ for strobe.
3. Differential input slew rate = 2 V/ns
4. Defines slew rate reference points, relative to input crossing voltages.
5. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
6. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.
7. The typical value of $V_{IX(AC)}$ is expected to be about $0.5 \times V_{CC}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{CC}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
8. The V_{IX} extended range (±175mV) is allowed only for the clock; this V_{IX} extended range is only allowed when the following conditions are met: The single-ended input signals are monotonic, have the single-ended swing V_{SEL}, V_{SEH} of at least $V_{CC}/2$ ±250mV, and the differential slew rate of CK, CK\ is greater than 3 V/ns.
9. V_{IX} must provide 25mV (single-ended) of the voltages separation.

Table 39: Minimum Required time before ringback (tDVAC) for CK - CK\

Slew Rate [V/ns]	DDR3L-800/1066/1333/1600	
	tDVAC [ps] @ |VIH/Ldiff(AC)| = 320mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = 270mV
> 4.0	189	201
4	189	201
3	162	179
2	109	134
1.8	91	119
1.6	69	100
1.4	40	76
1.2	Note	44
1	Note	Note
< 1	Note	Note

Definition for tJIT(cc), tJIT(cc, lck)
tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of |{tCKi+1-tCKi}|
tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
tJIT(cc) and tJIT(cc,lck) are not subject to production test.

Definition for tERR(nper)
tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

Refresh Parameters

Table 40: Refresh parameters(1,2)

Parameter	Symbol			Units
All Bank Refresh to active/refresh cmd time	tRFC		350	ns
Average periodic refresh interval	tREFI	-55°C ≤ TCASE ≤ 85°C	7.8	µs
		85°C < TCASE ≤ 105°C	3.9	µs
		105°C < TCASE ≤ 125°C	1.95	µs

Notes:
1. The permissible Tcase (Tc) operating temperature is specified by temperature grade. The maximum Tc is 95°C unless:

2. In general, the Refresh command needs to be issued at the tREFI interval. For flexibility, a maximum of 8 Refresh commands may be postponed or pulled-in (done in advance). However, in either case, the maximum interval between any two consecutive Refresh commands is 9 x tREFI.

Speed Bin Tables

Table 40: DDR3-800 Speed Bin

CL-tRCD-tRP			6-6-6		Units	Notes
Parameter		**Symbol**	**Min**	**Max**		
ACTIVATE to internal READ or WRITE delay time		tRCD	15		ns	
PRECHARGE command period		tRP	15			
ACTIVATE-to-ACTIVATE or REFRESH command period		tRC	52.5			
ACTIVATE-to-PRECHARGE ocommand period		tRAS	37.5	9 x tREFI		1
CL = 6	CWL = 5	tCK (AVG)	2.5	<3.3		2
Supported CL settings			6		CK	
Supported CWL settings			5			

Table 41: DDR3-1066 Speed Bin

CL-tRCD-tRP			8-8-8		Units	Notes
Parameter		**Symbol**	**Min**	**Max**		
Internal READ command to irst data		tAA	15		ns	
ACTIVATE to internal READ or WRITE delay time		tRCD	15			
PRECHARGE command period		tRP	15			
ACTIVATE-to-ACTIVATE or REFRESH command period		tRC	52.5			
ACTIVATE-to-PRECHARGE command period		tRAS	37.5	9 x tREFI		1
CL = 8	CWL = 6	tCK (AVG)	1.875	<2.5		2
Supported CL settings			8		CK	
Supported CWL settings			6			

Notes:

1. tREFI depends on TOPER.
2. The CL and CWL settings result in tCK requirements. When making a selection of tCK, both CL and CWL requirement settings need to be fullfilled.

Table 42: DDR3-1333/1600 Speed Bins

			DDR3-1333		DDR3-1600			
CL-tRCD-tRP			**9-9-9**		**11-11-11**		**Units**	**Notes**
Parameter		**Symbol**	**Min**					
Internal READ command to first data		^tAA	13.5		13.75		ns	
ACTIVATE to internal READ or WRITE delay time		^tRCD	13.5		13.75			
PRECHARGE command period		^tRP	13.5		13.75			
ACTIVATE-to-ACTIVATE or REFRESH command period		^tRC	49.5		48.75			
ACTIVATE-to-PRECHARGE command period		^tRAS	36	9 x tREFI	35	9 x tREFI		1
CL = 6	CWL = 5	^tCK (AVG)	2.5	3.3	2.5	3.3		
CL = 8	CWL = 6		1.875	<2.5	1.875	<2.5		2
CL = 9	CWL = 7		1.5	<1.875	1.5	<1.875		2
CL = 11	CWL = 8		1.5	<1.875	1.25	<1.5		
Supported CL settings			6, 8, 10		6, 8, 10, 11		CK	
Supported CWL settings			5, 6, 7		5, 6, 7, 8			

Notes:

1. ^tREFI depends on TOPER.
2. The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fullfilled.

Electrical Characteristics and AC Operating Conditions

Table 43: Timing Parameter by Speed Bin - DDR3-800, DDR3-1066

Parameter	Symbol	DDR3/DDR3L-800		DDR3/DDR3L-1066		Units	Notes
		Min.	Max.	Min.	Max.		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	5	-	5	-	ns	6
Average Clock Period	tCK(avg)	Refer to Standard Speed Bins				ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min				ps	
		Max.: tCK(avg)max + tJIT(per)max					
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	tCK(avg)	25
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	tCK(avg)	26
Clock Period Jitter	tJIT(per)	-100	100	-90	90	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-90	90	-80	80	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	200	200	180	180	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	180	180	160	160	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-147	147	-132	132	ps	
Cumulative error across 3 cycles	tERR(3per)	-175	175	-157	157	ps	
Cumulative error across 4 cycles	tERR(4per)	-194	194	-175	175	ps	
Cumulative error across 5 cycles	tERR(5per)	-209	209	-188	188	ps	
Cumulative error across 6 cycles	tERR(6per)	-222	222	-200	200	ps	
Cumulative error across 7 cycles	tERR(7per)	-232	232	-209	209	ps	
Cumulative error across 8 cycles	tERR(8per)	-241	241	-217	217	ps	
Cumulative error across 9 cycles	tERR(9per)	-249	249	-224	224	ps	
Cumulative error across 10 cycles	tERR(10per)	-257	257	-231	231	ps	
Cumulative error across 11 cycles	tERR(11per)	-263	263	-237	237	ps	
Cumulative error across 12 cycles	tERR(12per)	-269	269	-242	242	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min				ps	24
		tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max					
Data Timing							
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	tCK(avg)	13,g
DQ low-impedance time from CK, CK#	tLZ(DQ)	-800	400	-600	300	ps	13,14,f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	ps	13,14,f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC175 or AC160	See table for Data Setup and Hold				ps	d,17
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150 or AC135					ps	d,17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100 or DC90					ps	d,17
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	ps	28

Timing Parameter by Speed Bin - DDR3-800, DDR3-1066, Continued

Parameter	Symbol	DDR3/DDR3L-800		DDR3/DDR3L-1066		Units	Notes
		Min.	Max.	Min.	Max.		
Data Strobe Timing							
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	13,19,g
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11,13,g
DQS, DQS# differential output high time	tQSH	0.38	-	0.38	-	tCK(avg)	13,g
DQS, DQS# differential output low time	tQSL	0.38	-	0.38	-	tCK(avg)	13,g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-400	400	-300	300	ps	13,f
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-800	400	-600	300	ps	13,14,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	400	-	300	ps	13,14,f
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)	29,31
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)	30,31
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	tCK(avg)	c,32
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	tCK(avg)	c,32
Command and Address Timing							
DLL locking time	tDLLK	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns) tRTPmax.: -					e
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns) tWTRmax.:					e,18
WRITE recovery time	tWR	15	-	15	-	ns	e,18
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns) tMODmax.:					
ACT to internal read or write delay time	tRCD	Standard Speed Bins					e
PRE command period	tRP	Standard Speed Bins					e
ACT to ACT or REF command period	tRC	Standard Speed Bins					e
CAS# to CAS# command delay	tCCD	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))				nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins					e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 10ns)	-	max(4nCK, 10ns)	-		e
Four activate window for 2KB page size	tFAW	50	-	50	-	ns	e

Timing Parameter by Speed Bin - DDR3-800, DDR3-1066

Parameter	Symbol	DDR3/DDR3L-800		DDR3/DDR3L-1066		Units	Notes
		Min.	Max.	Min.	Max.		
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC175 or AC160	See table for ADD / CMD setup and hold				ps	b, 16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150 or AC135					ps	b, 16, 27
Command and Address setup time to CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base) DC100 or DC90					ps	b, 16
Control and Address Input pulse width for each input	tIPW	900	-	780	-	ps	28
Calibration Timing							
Power-up and RESET calibration time	tZQinit	max (512 nCK, 640ns)	-	max (512 nCK, 640ns)	-		
Normal operation Full calibration time	tZQoper	max (256 nCK, 320ns)	-	max (256 nCK, 320ns)	-		
Normal operation Short calibration time	tZQCS	max (64 nCK, 80ns)	-	max (64 nCK, 80ns)	-		23
Reset Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns)					
		tXPRmax.: -					
Self Refresh Timing							
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns)					
		tXSmax.: -					
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min)				nCK	2
		tXSDLLmax.: -					
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK					
		tCKESRmax.: -					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns)					
		tCKSREmax.: -					
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns)					
		tCKSRXmax.: -					
Self Refresh Timing							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 7.5ns)					
		tXPmax.: -					
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns)					
		tXPDLLmax.: -					
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK 7.5ns)		tCKEmin.: max(3nCK 5.625ns)			
		tCKEmax.: -		tCKEmax.: -			
Command pass disable delay	tCPDED	tCPDEDmin.: 1				nCK	
		tCPDEDmax.: -					
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min)					15
		tPDmax.: 9*tREFI					

***PRELIMINARY information. Subject to change without notice.**

Timing Parameter by Speed Bin - DDR3-800, DDR3-1066

Parameter	Symbol	DDR3/DDR3L-800		DDR3/DDR3L-1066		Units	Notes
		Min.	Max.	Min.	Max.		
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -				nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -				nCK	20
Parameter	**Symbol**	**DDR3-800**		**DDR3-1066**		**Units**	**Notes**
		Min.	**Max.**	**Min.**	**Max.**		
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -				nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -				nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -				nCK	10
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -				nCK	20, 21
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -					
ODT Timing							
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -				nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -				nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-400	400	-300	300	ps	7,f
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timings							
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	325	-	245	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	325	-	245	-	ps	
Write leveling output delay	tWLO	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

Timing Parameter by Speed Bin - DDR3-1333, DDR3-1600

Parameter	Symbol	DDR3/DDR3L-1333		DDR3/DDR3L-1600		Units	Notes
		Min.	Max.	Min.	Max.		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	5	-	5	-	ns	6
Average Clock Period	tCK(avg)	Refer to Standard Speed Bins				ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min.: tCK(avg)min + tJIT(per)min				ps	
		Max.: tCK(avg)max + tJIT(per)max					
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	tCK(avg)	25
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	tCK(avg)	26
Clock Period Jitter	tJIT(per)	-80	80	-70	70	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-70	70	-60	60	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	160	160	140	140	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140	140	120	120	ps	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	-118	118	-103	103	ps	
Cumulative error across 3 cycles	tERR(3per)	-140	140	-122	122	ps	
Cumulative error across 4 cycles	tERR(4per)	-155	155	-136	136	ps	
Cumulative error across 5 cycles	tERR(5per)	-168	168	-147	147	ps	
Cumulative error across 6 cycles	tERR(6per)	-177	177	-155	155	ps	
Cumulative error across 7 cycles	tERR(7per)	-186	186	-163	163	ps	
Cumulative error across 8 cycles	tERR(8per)	-193	193	-169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	-200	200	-175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	-205	205	-180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	-210	210	-184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	-215	215	-188	188	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min				ps	24
		tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max					
Data Timing							
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	tCK(avg)	13,g
DQ low-impedance time from CK, CK#	tLZ(DQ)	-500	250	-450	225	ps	13,14,f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	250	-	225	ps	13,14,f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC150	See table for Data Setup and Hold				ps	d,17
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base) AC135					ps	d,17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100 or DC90					ps	d,17
DQ and DM Input pulse width for each input	tDIPW	400	-	360	-	ps	28

Timing Parameter by Speed Bin - DDR3-1333, DDR3-1600 - Continued

Parameter	Symbol	DDR3/DDR3L-1333		DDR3/DDR3L-1600		Units	Notes
		Min.	Max.	Min.	Max.		
Data Strobe Timing							
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	13,19,g
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11,13,g
DQS, DQS# differential output high time	tQSH	0.4	-	0.4	-	tCK(avg)	13,g
DQS, DQS# differential output low time	tQSL	0.4	-	0.4	-	tCK(avg)	13,g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-255	255	-225	225	ps	13,f
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-500	250	-450	225	ps	13,14,f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	250	-	225	ps	13,14,f
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)	29,31
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)	30,31
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	-0.27	0.27	tCK(avg)	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.18	-	tCK(avg)	c,32
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.18	-	tCK(avg)	c,32
Command and Address Timing							
DLL locking time	tDLLK	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	tRTPmin.: max(4nCK, 7.5ns)					
		tRTPmax.: -					
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin.: max(4nCK, 7.5ns)					
		tWTRmax.:					
WRITE recovery time	tWR	15	-	15	-	ns	e,18
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	tMODmin.: max(12nCK, 15ns)					
		tMODmax.:					
ACT to internal read or write delay time	tRCD	Standard Speed Bins					
PRE command period	tRP	Standard Speed Bins					
ACT to ACT or REF command period	tRC	Standard Speed Bins					
CAS# to CAS# command delay	tCCD	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))				nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	Standard Speed Bins					
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		
Four activate window for 2KB page size	tFAW	45	-	40	-	ns	e

Timing Parameter by Speed Bin - DDR3-1333, DDR3-1600 - Continued

Parameter	Symbol	DDR3/DDR3L-1333		DDR3/DDR3L-1600		Units	Notes
		Min.	Max.	Min.	Max.		
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC175 or AC160	See table for ADD/CMD Setup and Hold				ps	b,16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150 or AC135					ps	b,16,27
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base) DC100 or DC90					ps	b,16
Control and Address Input pulse width for each input	tIPW	620	-	560	-	ps	28
Calibration Timing							
Power-up and RESET calibration time	tZQinit	max (512 nCK, 640ns)	-	max (512 nCK, 640ns)	-		
Normal operation Full calibration time	tZQoper	max (256 nCK, 320ns)	-	max (256 nCK, 320ns)	-		
Normal operation Short calibration time	tZQCS	max (64 nCK, 80ns)	-	max (64 nCK, 80ns)	-		23
Reset Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	tXPRmin.: max(5nCK, tRFC(min) + 10ns)					
		tXPRmax.: -					
Self Refresh Timings							
Exit Self Refresh to commands not requiring a locked DLL	tXS	tXSmin.: max(5nCK, tRFC(min) + 10ns)					
		tXSmax.: -					
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tXSDLLmin.: tDLLK(min)				nCK	2
		tXSDLLmax.: -					
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKESRmin.: tCKE(min) + 1 nCK					
		tCKESRmax.: -					
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	tCKSREmin.: max(5 nCK, 10 ns)					
		tCKSREmax.: -					
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	tCKSRXmin.: max(5 nCK, 10 ns)					
		tCKSRXmax.: -					
Power Down Timings							
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	tXPmin.: max(3nCK, 6ns)					
		tXPmax.: -					
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	tXPDLLmin.: max(10nCK, 24ns)					
		tXPDLLmax.: -					
CKE minimum pulse width	tCKE	tCKEmin.: max(3nCK 5.625ns)		tCKEmin.: max(3nCK 5ns)			
		tCKEmax.: -		tCKEmax.: -			
Command pass disable delay	tCPDED	tCPDEDmin.: 1				nCK	
		tCPDEDmax.: -					
Power Down Entry to Exit Timing	tPD	tPDmin.: tCKE(min)					15
		tPDmax.: 9*tREFI					

Timing Parameter by Speed Bin - DDR3-1333, DDR3-1600 - Continued

Parameter	Symbol	DDR3/DDR3L-1333		DDR3/DDR3L-1600		Units	Notes
		Min.	Max.	Min.	Max.		
Timing of ACT command to Power Down entry	tACTPDEN	tACTPDENmin.: 1 tACTPDENmax.: -				nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	tPRPDENmin.: 1 tPRPDENmax.: -				nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	tRDPDENmin.: RL+4+1 tRDPDENmax.: -				nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: -				nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	tWRPDENmin.: WL + 2 + (tWR / tCK(avg)) tWRPDENmax.: -				nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: -				nCK	10
Timing of REF command to Power Down entry	tREFPDEN	tREFPDENmin.: 1 tREFPDENmax.: -				nCK	20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMRSPDENmin.: tMOD(min) tMRSPDENmax.: -					
ODT Timings							
ODT high time without write command or with write command and BC4	ODTH4	ODTH4min.: 4 ODTH4max.: -				nCK	
ODT high time with Write command and BL8	ODTH8	ODTH8min.: 6 ODTH8max.: -				nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-250	250	-225	225	ps	7,f
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timings							
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	195	-	165	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	195	-	165	-	ps	
Write leveling output delay	tWLO	0	9	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

Timing Notes

Specific Note a
Unit “tCK(avg)” represents the actual tCK(avg) of the input clock under operation. Unit “nCK” represents one clock cycle of the input clock, counting the actual clock edges. ex) tMRD=4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4-Tm) is 4 x tCK(avg) + tERR(4per), min.

Specific Note b
These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc) transition edge to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note c
These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)) crossing to its respective clock signal (CK, CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note d
These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)) crossing.

Specific Note e
For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{tPARAM[ns] / tCK(avg)[ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP =RU{tRP/tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP/tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6-Tm) is less than 15ns due to input clock jitter.

Specific Note f
When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper), act of the input clock, where 2 <= m <=12. (output derating are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = -172ps and tERR(mper),act,max = 193ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = -400ps - 193ps = -593ps and tDQSCK,max(derated) = tDQSCK,max - ERR(mper),act,min = 400ps + 172ps = 572ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = -800ps - 193ps = -993ps and tLZ(DQ),max(derated) = 400ps + 172ps = 572ps.
(Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

Specific Note g
When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act=2500ps, tJIT(per),act,min = -72ps and tJIT(per),act,max = 93ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500ps - 72ps = 2178ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500ps - 72ps = 878ps.
(Caution on the min/max usage!)

Timing Notes - Continued

Timing Parameters

1. Actual value dependent upon measurement level definitions.
2. Commands requiring a locked DLL are: READ (and RAP) are synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rouned-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT-on time tAON See “Timing Parameters”.
8. For definition of RTT-off time tAOF See “Timing Parameters”.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles are programmed in MR0.
11. The maximum read postamble is bonded by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter.
15. tREFI depends on TOPER.
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK differential slew rate. Note for DQ and DM signals, VREF(DC)=VRefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC).
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS differential slew rate. Note for DQ and DM signals, VREF(DC)=VRefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC).
18. Start of internal write transaction is defined as follows:
    a. For BL8 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
    b. For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
    c. For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum preamble is bound by tLZ(DQS)max on the left side and tDQSCK(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
24. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. the interval could be defined by the following formula:

Timing Notes - Continued

ZQ Correction / [Tsens x Tdriftrate) + (VSens x Vdriftrate)], where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5%/C, VSens = 0.15%/mV, Tdriftrate = 1 C/sec and Vdriftrate = 15mV/sec, then the interval between ZQCS commands is calculated as

0.5 / [(1.5x1)+(0.15x15)] = 0.133 ≈ 128ms

25. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
26. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
27. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
28. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100ps of derating to accommodate for the lower altemate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV - 150mV) / 1V/ns].
29. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).
30. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.
31. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.
32. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
33. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the datasheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value, respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value . If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to VREF (dc) level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF (dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition, a valid input signal is still required to complete the transition and reach VIH/IL(ac). For slew rates in between the values listed in the tables, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 44: ADD/CMD Setup and Hold Base-Values for 1V/ns

DDR3/ DDR3L	Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	DDR3-2133	Units
DDR3	tIS(base) AC175	VIH/L(ac)	200	125	65	45	-	-	ps
	tIS(base) AC150	VIH/L(ac)	350	275	190	170	-	-	ps
	tIS(base) AC135	VIH/L(ac)	-	-	-	-	65	60	ps
	tIS(base) AC125	VIH/L(ac)	-	-	-	-	150	135	ps
	tIH(base) DC100	VIH/L(dc)	275	200	140	120	100	95	ps
DDR3L	tIS(base) AC160	VIH/L(ac)	215	140	80	60	-	-	ps
	tIS(base) AC135	VIH/L(ac)	365	290	205	185	65	-	ps
	tIS(base) AC125	VIH/L(ac)	-	-	-	-	150	-	ps
	tIH(base) DC90	VIH/L(dc)	285	210	150	130	110	-	ps

Note:
1. (AC/DC referenced for 1V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate)

Figure 39: Mechanical Diagram (Bottom View)

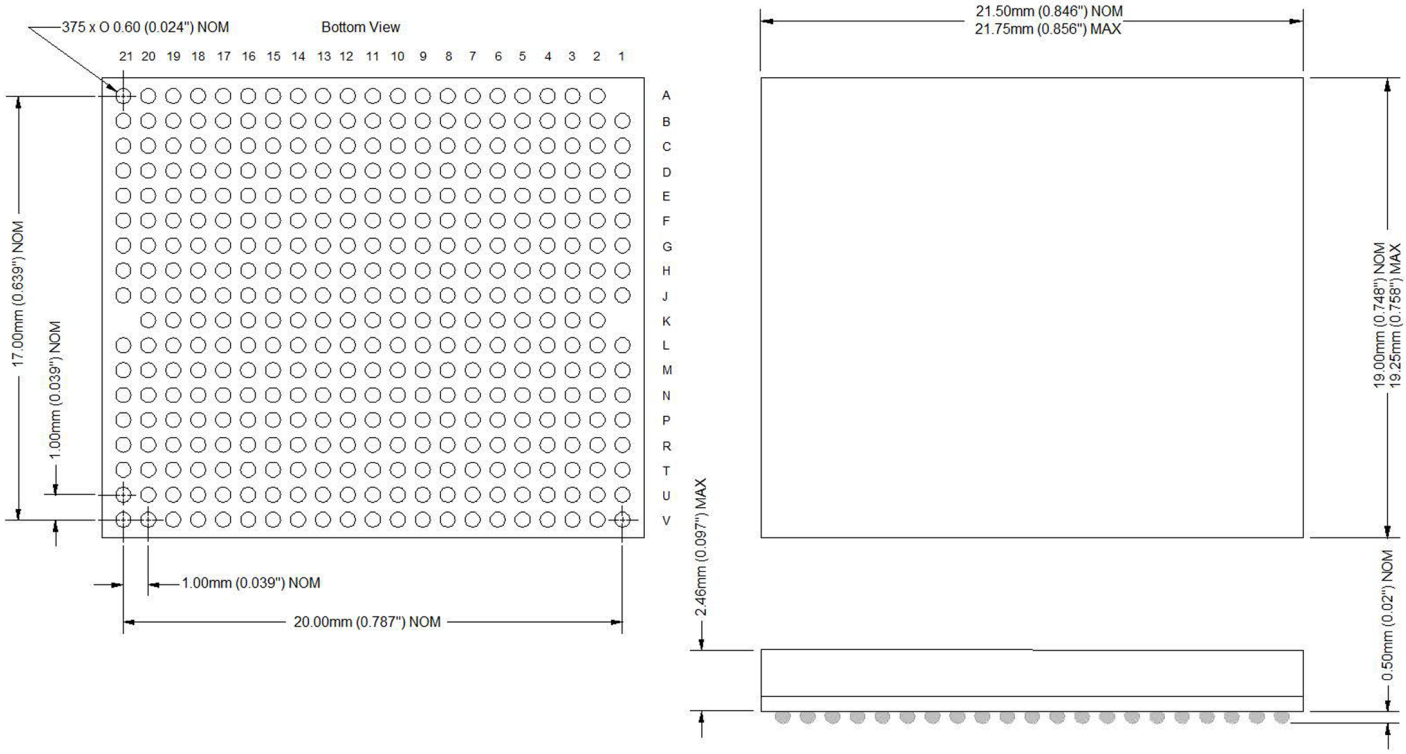


Table 45: DDR3L [1.35V] Ordering Information

Part Number	Core Frequency (MHz)	Data Rate (Mbps)	Device Grade	Availability
MYX4DD3K512M72PBG2-13/IT	800	1600	Industrial	Development
MYX4DD3K512M72PBG2-15/IT	667	1333		
MYX4DD3K512M72PBG2-19/IT	533	1066		
MYX4DD3K512M72PBG2-25/IT	400	800		
MYX4DD3K512M72PBG2-15/ET	667	1333	Enhanced	Development
MYX4DD3K512M72PBG2-19/ET	533	1066		
MYX4DD3K512M72PBG2-25/ET	400	800		
MYX4DD3K512M72PBG2-15/XT	667	1333	Military Temp	Development
MYX4DD3K512M72PBG2-19/XT	533	1066		
MYX4DD3K512M72PBG2-25/XT	400	800		
MYX4DD3K512M72PBG2R-13/IT	800	1600	Industrial - RoHS	Development
MYX4DD3K512M72PBG2R-15/IT	667	1333		
MYX4DD3K512M72PBG2R-19/IT	533	1066		
MYX4DD3K512M72PBG2R-25/IT	400	800	Enhanced - RoHS	Development
MYX4DD3K512M72PBG2R-15/ET	667	1333		
MYX4DD3K512M72PBG2R-19/ET	533	1066		
MYX4DD3K512M72PBG2R-25/ET	400	800	Military - RoHS	Development
MYX4DD3K512M72PBG2R-15/XT	667	1333		
MYX4DD3K512M72PBG2R-19/XT	533	1066		
MYX4DD3K512M72PBG2R-25/XT	400	800		
MYX4DD3K512M72PBG2-13/xx	800	1600	Enhanced, Military Temp	Consult Factory

IT = Industrial = industrial class integrated component, fully operable across -40°C to +85°C
ET = Enhanced = enhanced class integrated component, fully operable across -40°C to +105°C
XT = Military = military class integrated component, fully operable across -55°C to +125°C
* Please contact a Micross sales representative for IBIS or thermal models at sales.americas@micross.com or

Document Title

4GByte DDR3 iPEM, Unbuffered w/ ECC - 512M x 72, 375 PBGA

Revision History

Revision #	History	Release Date	Status
1.0	• Initial Release	February 2016	ADVANCE
2.0	• ADVANCE to PRELIMINARY, ICCx Current updates, added additional descriptions/features, revised to indicate JEDEC speed grade, added Partial Array Refresh for INDUSTRIAL grade product. • Correct package dimensions and number of BGA interconnects • Change release date to September	September 2019	PRELIMINARY