

12-Bit Digital-to-Analog Converter with Two-Wire Interface

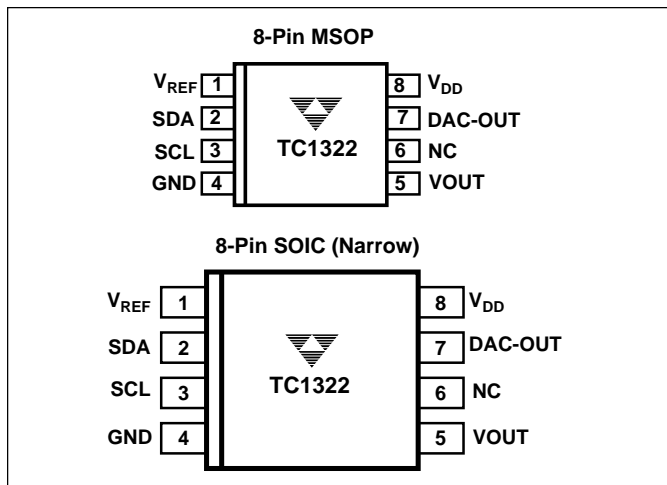
FEATURES

- 12-Bit Digital-Analog Converter
- 8-Pin SOIC and 8-Pin MSOP Packages
- 2.7–5.5V Single-Supply Operation
- Simple SMBus/I²C Serial Interface
- Low Power - 0.35mA Operation, 0.5µA Shutdown
- Guaranteed Monotonicity

TYPICAL APPLICATIONS

- Programmable Voltage Sources
- Digital-Controlled Amplifiers/Attenuators
- Process Monitoring and Control
- Microprocessor- controlled systems

PIN CONFIGURATION



GENERAL DESCRIPTION

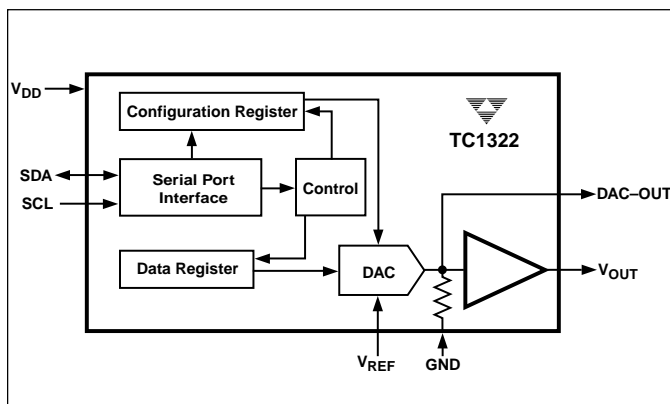
The TC1322 is a serially accessible 12-bit voltage output digital-to-analog converter (DAC). The DAC produces an output voltage that ranges from ground to an externally supplied reference voltage. It operates from a single power supply that can range from 2.7V to 5.5V, making it ideal for a wide range of applications. Built into the part is a power-on reset function that ensures that the device starts at a known condition.

Communication with the TC1322 is accomplished via a simple 2-wire SMBus/I²C compatible serial port with the TC1322 acting as a slave only device. The host can enable the SHDN bit in the CONFIG register to activate the low-power standby mode.

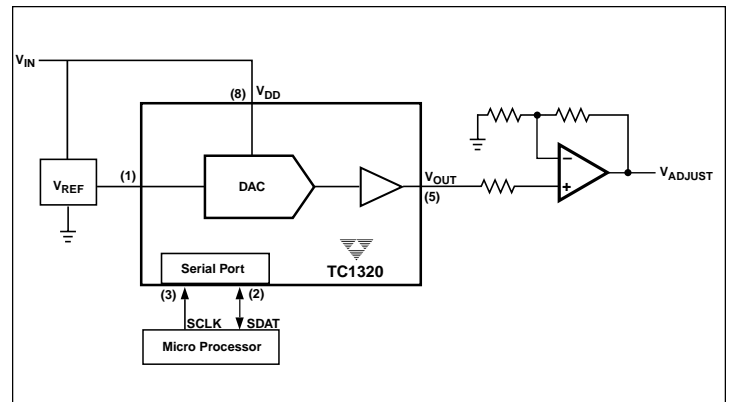
ORDERING INFORMATION

| Part No. | Package | Temp. Range |
|-----------|---------------------|----------------|
| TC1322EOA | 8-Pin SOIC (Narrow) | -40°C to +85°C |
| TC1322EUA | 8-Pin MSOP | -40°C to +85°C |

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS DRAWING



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TC1322

ABSOLUTE MAXIMUM RATINGS*

| | |
|--|------------------------------------|
| Supply Voltage (V_{DD}) | +6V |
| Voltage On Any Pin | (GND – 0.3V) to (V_{DD} + 0.3V) |
| Operating Temperature (T_A) | See Below |
| Storage Temperature (T_{STG}) | – 65°C to +150°C |
| Current On Any Pin | ±50 mA |
| Package Thermal Resistance (θ_{JA}) | 330°C/W |

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_{DD} = 2.7V$ to $5.5V$, $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---------------------|------------------------|---|-----|------|-----|------|
| Power Supply | | | | | | |
| V_{DD} | Supply Voltage | | 2.7 | — | 5.5 | V |
| I_{DD} | Operating Current | $V_{DD} = 5.5V$, $V_{REF} = 1.2V$ Serial Port Inactive (Note 1) | — | 0.35 | 0.5 | mA |
| $I_{DD-STANDBY}$ | Standby Supply Current | $V_{DD} = 3.3V$ Serial Port Inactive (Note 1) | — | 0.1 | 1 | μA |

STATIC PERFORMANCE—ANALOG SECTION: ($V_{DD} = 2.7V$ to $5.5V$, $V_{REF} = 1.2V$, $-40^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|------------|--|--------------------------------|-----|------|----------------|-------|
| | Resolution | | — | — | 12 | Bits |
| INL | Integral Non-Linearity at FS, $T_A = 25^\circ C$ | | — | — | ±16 | LSB |
| FSE | Full Scale Error | | — | — | ±3 | %FS |
| DNL | Differential Non-Linearity, $T_A = 25^\circ C$ | All Codes (Note 2) | -1 | — | +4 | LSB |
| V_{OS} | Offset Error at V_{OUT} | (Note 2) | — | ±0.3 | ±8 | mV |
| TCV_{OS} | Offset Error Tempco at V_{OUT} | | — | 10 | — | μV/°C |
| PSRR | Power Supply Rejection Ratio | V_{DD} at DC | — | 80 | — | dB |
| V_{REF} | Voltage Reference Range | | 0 | — | $V_{DD} - 1.2$ | V |
| I_{REF} | Reference Input Leakage Current | | — | — | ±1.0 | μA |
| V_{SW} | Voltage Swing | $V_{REF} \leq (V_{DD} - 1.2V)$ | 0 | — | V_{REF} | V |
| R_{OUT} | Output Resistance @ V_{OUT} | R_{OUT} (ohmic) | — | 5 | — | Ω |
| I_{OUT} | Output Current (Source or Sink) | | — | 2 | — | mA |
| I_{SC} | Output Short-Circuit Current $V_{DD} = 5.5V$ | Source | — | 30 | 50 | mA |
| | | Sink | — | 20 | 50 | mA |

- NOTES:** 1. SDA and SCL must be connected to V_{DD} or GND.
2. Measured at $V_{OUT} \geq 50mV$ referred to GND to avoid output buffer clipping.

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DYNAMIC PERFORMANCE: ($V_{DD} = 2.7V$ to $5.5V$, $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---------------------|---|-------------------------------|-----|-----|-----|------------|
| SR | Voltage Output Slew Rate | | — | 0.8 | — | V/ μ s |
| t _{SETTLE} | Output Voltage Full Scale Settling Time | | — | 10 | — | μ sec |
| t _{WU} | Wake-up Time | | — | 20 | — | μ s |
| | Digital Feedthrough and Crosstalk | SDA = V_{DD} , SCL = 100kHz | — | 5 | — | nV-s |

SERIAL PORT INTERFACE: ($V_{DD} = 2.7V$ to $5.5V$, $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------------|----------------------------|--|-----|-----|----------|---------|
| V _{IH} | Logic Input High | | 2.4 | — | V_{DD} | V |
| V _{IL} | Logic Input Low | | — | — | 0.6 | V |
| V _{OL} | SDA Output Low | I _{OL} = 3 mA (Sinking Current) I _{OL} = 6 mA | — | — | 0.4 | V |
| | | | — | — | 0.6 | V |
| C _{IN} | Input Capacitance SDA, SCL | | — | 5 | — | pF |
| I _{LEAK} | I/O Leakage | | — | — | ±1 | μ A |

SERIAL PORT AC TIMING: $V_{DD} = 2.7V$ to $5.5V$, $-40^{\circ}C \leq (T_A = T_J) \leq 85^{\circ}C$; C_L = 80pF, unless otherwise noted.)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|------------------------|---------------------------------------|--|-----|-----|------|-----------|
| f _{SMB} | SMBus Clock Frequency | | 10 | — | 100 | kHz |
| t _{IDLE} | Bus Free Time Prior to New Transition | | 4.7 | — | — | μ sec |
| t _{H(START)} | Start Condition Hold Time | | 4.0 | — | — | μ sec |
| t _{SU(START)} | Start Condition Setup Time | 90% SCL to 10% SDA (for repeated Start Condition) | 4.7 | — | — | μ sec |
| t _{SU(STOP)} | Stop Condition Setup Time | | 4.0 | — | — | μ sec |
| t _{H-DATA} | Data In Hold Time | | 100 | — | — | nsec |
| t _{SU-DATA} | Data In Setup Time | | 100 | — | — | nsec |
| t _{LOW} | Low Clock Period | 10% to 10% | 4.7 | — | — | μ sec |
| t _{HIGH} | High Clock Period | 90% to 90% | 4 | — | — | μ sec |
| t _F | SMBus Fall Time | 90% to 10% | — | — | 300 | nsec |
| t _R | SMBus Rise Time | 10% to 90% | — | — | 1000 | nsec |
| t _{POR} | Power-On Reset Delay | $V_{DD} \geq V_{POR}$ (Rising Edge) | — | 500 | — | μ sec |

PIN DESCRIPTION

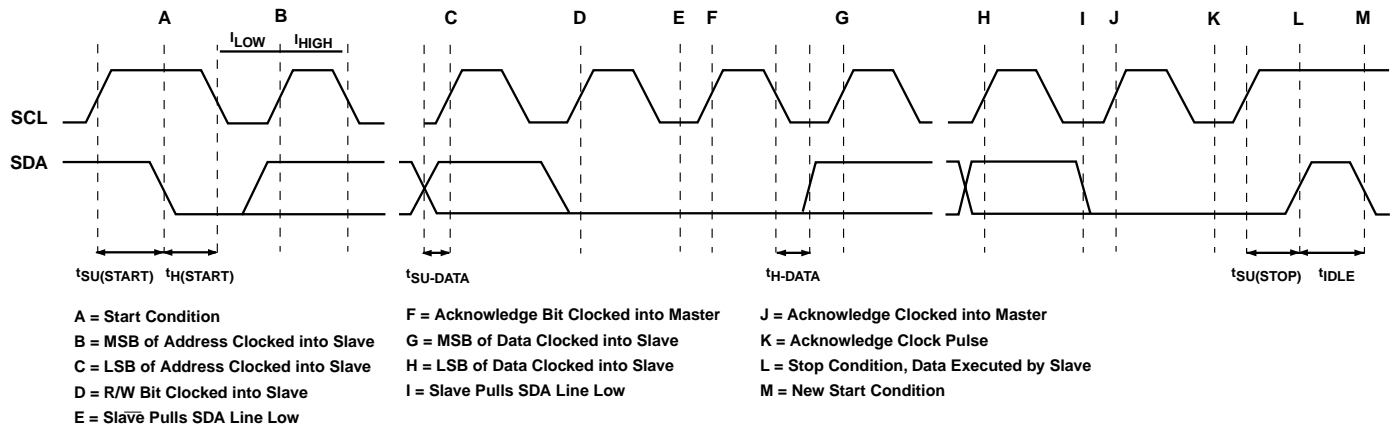
| Pin No. | Symbol | Type | Description |
|---------|------------------|----------------|-----------------------------|
| 1 | V _{REF} | Input | Voltage Reference Input |
| 2 | SDA | Bi-Directional | SMBUS Serial Data |
| 3 | SCL | Input | SMBUS Serial Clock |
| 4 | GND | Input | System Ground |
| 5 | VOUT | Output | Buffered DAC Output |
| 6 | NC | None | Not Connected |
| 7 | DAC_OUT | Output | Unbuffered DAC Output |
| 8 | V _{DD} | Power | Positive Power Supply Input |

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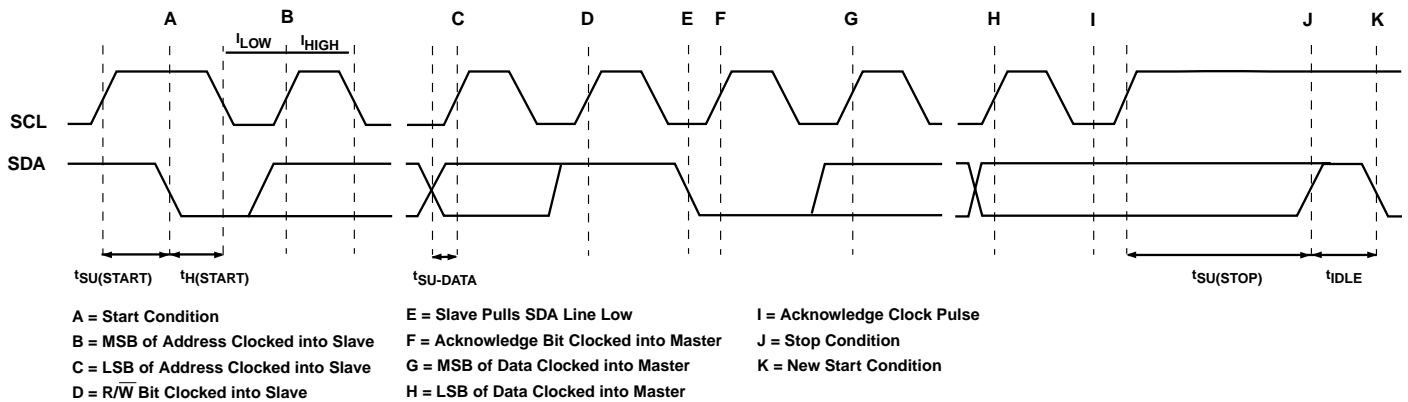
TC1322

TIMING DIAGRAMS

SMBUS Write Timing Diagram



SMBUS READ Timing Diagram



PIN DESCRIPTION

V_{REF}

Input. Voltage Reference Input can range from 0V to 1.2V below V_{DD} .

SDA

Bi-directional. Serial data is transferred on the SMBus in both directions using this pin. See System Management Bus Specification rev. 1.0 for timing diagrams.

SCL

Input. SMBus serial clock. Clocks data into and out of the TC1322. See System Management Bus Specification rev. 1.0 for timing diagrams.

GND

Input. Ground return for all TC1322 functions.

VOUT

Output. Buffered DAC output voltage. This voltage is a function of the reference voltage and the contents of the DATA register. See Functional Description section.

DAC_OUT

Output. Unbuffered DAC output voltage. This voltage is a function of the reference voltage and the contents of the DATA register. However, since it is unbuffered, care must be taken that the pin is connected only to a high impedance node.

V_{DD}

Input. Positive power supply input. See electrical specifications.

DETAILED DESCRIPTION

The TC1322 is a monolithic 12-bit digital-to-analog converter that is designed to operate from a single supply that can range from 2.7V to 5.5V. The DAC consists of a data register (DATA), a configuration register (CONF), and a current output amplifier. The TC1322 uses an external reference which also determines the maximum output voltage.

The TC1322 uses a current-steering DAC based on an array of matched current sources which goes into the precision resistor that converts the contents of the Data Register and V_{REF} into an output voltage, V_{OUT} given by:

$$V_{OUT} = V_{REF} (DATA / 4096)$$

Reference Input

The reference pin, V_{REF} , is a buffered high impedance input and because of this the load regulation of the reference source need only to be able to tolerate leakage levels of current (less than $1\mu A$). V_{REF} accepts a voltage range from 0 to ($V_{DD} - 1.2V$). Input capacitance is typically around 10 pF.

Output Amplifier

The TC1322 DAC output is buffered with an internal unity-gain rail-to-rail input/output amplifier with a typical slew rate of $0.8V/\mu sec$. Maximum full-scale transition settling time is $10\mu sec$ to within $\pm 1/2$ LSB when loaded with $1k\Omega$ in parallel with $100pF$.

Standby Mode

The TC1322 allows the host to put it into a low power ($I_{DD} = 0.5\mu A$, typical) Standby mode. In this mode, the D/A conversion is halted. The SMBus port operates normally. Standby mode is enabled by setting the SHDN bit in the CONFIG register. The table below summarizes this operation.

Standby Mode Operation

| SHDN Bit | Operating Mode |
|----------|----------------|
| 0 | Normal |
| 1 | Standby |

SMBus Slave Address

The TC1322 is internally programmed to have a default SMBus address value of 1001 000b. Seven other addresses are available by custom order (contact factory).

SERIAL PORT OPERATION

The Serial Clock input (SCL) and bi-directional data port (SDA) form a 2-wire bi-directional serial port for programming and interrogating the TC1322. The following conventions are used in this bus architecture:

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Write 1 Byte Format

| S | ADDRESS | WR | ACK | COMMAND | ACK | DATA | ACK | P |
|---|---------|----|-----|---------|-----|--------|-----|---|
| | 7 Bits | | | 8 Bits | | 8 Bits | | |

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Write 2 Byte Format

| S | ADDRESS | WR | ACK | COMMAND | ACK | DATA | ACK | DATA | ACK | P |
|---|---------|----|-----|---------|-----|--------|-----|--------|-----|---|
| | 7 Bits | | | 8 Bits | | 8 Bits | | 8 Bits | | |

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Read 1 Byte Format

| S | ADDRESS | WR | ACK | COMMAND | ACK | S | ADDRESS | RD | ACK | DATA | NACK | P |
|---|---------|----|-----|---------|-----|---|---------|----|-----|--------|------|---|
| | 7 Bits | | | 8 Bits | | | 7 Bits | | | 8 Bits | | |

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data-flow direction.

Data Byte: reads from the register set by the command byte.

Read 2 Byte Format

| S | ADDRESS | WR | ACK | COMMAND | ACK | S | ADDRESS | RD | ACK | DATA | ACK | DATA | NACK | P |
|---|---------|----|-----|---------|-----|---|---------|----|-----|--------|-----|--------|------|---|
| | 7 Bits | | | 8 Bits | | | 7 Bits | | | 8 Bits | | 8 Bits | | |

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data-flow direction.

Data Byte: reads from the register set by the command byte.

Receive 1 Byte Format

| S | ADDRESS | RD | ACK | DATA | NACK | P |
|---|---------|----|-----|--------|------|---|
| | 7 Bits | | | 8 Bits | | |

S = Start Condition

P = Stop Condition

Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last Read Byte or Write Byte transmission.

Receive 1 Byte Format

| S | ADDRESS | RD | ACK | DATA | ACK | DATA | NACK | P |
|---|---------|----|-----|--------|-----|--------|------|---|
| | 7 Bits | | | 8 Bits | | 8 Bits | | |

S = Start Condition

P = Stop Condition

Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last Read Byte or Write Byte transmission.

Figure 1. SMBus Protocols

TC1322 Serial Bus Conventions

| TERM | EXPLANATION |
|-------------|--|
| Transmitter | The device sending data to the bus. |
| Receiver | The device receiving data from the bus. |
| Master | The device which controls the bus: initiating transfers (START), generating the clock, and terminating transfers. (STOP) |
| Slave | The device addressed by the master. |
| Start | A unique condition signaling the beginning of a transfer indicated by SDA falling (High –Low) while SCL is high. |
| Stop | A unique condition signaling the end of a transfer indicated by SDA rising (Low –High) while SCL is high. |
| ACK | A Receiver acknowledges the receipt of each byte with this unique condition. The Receiver drives SDA low during SCL high of the ACK clock-pulse. The Master provides the clock pulse for the ACK cycle. |
| Busy | Communication is not possible because the bus is in use. |
| NOT Busy | When the bus is idle, both SDA and SCL will remain high. |
| Data Valid | The state of SDA must remain stable during the High period of SCL in order for a data bit to be considered valid. SDA only changes state while SCL is low during normal data transfers. (See Start and Stop conditions.) |

All transfers take place under control of a host, usually a CPU or microcontroller, acting as the Master, which provides the clock signal for all transfers. The TC1322 *always* operates as a Slave. The serial protocol is illustrated in Figure 1. All data transfers have two phases; all bytes are transferred MSB first. Accesses are initiated by a start condition (START), followed by a device address byte and one or more data bytes. The device address byte includes a Read/Write selection bit. Each access must be terminated by a Stop Condition (STOP). A convention called *Acknowledge* (ACK) confirms receipt of each byte. Note that SDA can change only during periods when SCL is LOW (SDA changes while SCL is HIGH are reserved for Start and Stop Conditions).

Start Condition (START)

The TC1322 continuously monitors the SDA and SCL lines for a start condition (a HIGH to LOW transition of SDA while SCL is HIGH), and will not respond until this condition is met.

Address Byte

Immediately following the Start Condition, the host must transmit the address byte to the TC1322. The 7-bit SMBus address for the TC1322 is 1001000. The 7-bit address transmitted in the serial bit stream must match for the TC1322 to respond with an Acknowledge (indicating the TC1322 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read-Write Bit. This bit is a 1 for a read operation or 0 for a write operation. During the first phase of any transfer this bit will be set = 0 to indicate that the command byte is being written.

Acknowledge (ACK)

Acknowledge (ACK) provides a positive handshake between the host and the TC1322. The host releases SDA after transmitting eight bits, then generates a ninth clock cycle to allow the TC1322 to pull the SDA line LOW to acknowledge that it successfully received the previous eight bits of data or address.

Data Byte

After a successful ACK of the address byte, the host must transmit the data byte to be written or clock out the data to be read. (See the appropriate timing diagrams.) ACK will be generated after a successful write of a data byte into the TC1322.

Stop Condition (STOP)

Communications must be terminated by a stop condition (a LOW to HIGH transition of SDA while SCL is HIGH). The Stop Condition must be communicated by the transmitter to the TC1322. NOTE: Refer to Timing Diagrams for serial bus timing.

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REGISTER SET AND PROGRAMMER'S MODEL

TC1322 Command Set (SMBus READ_BYTE and WRITE_BYTE)

| COMMAND BYTE DESCRIPTION | | |
|--------------------------|------|-----------------------------------|
| COMMAND | CODE | FUNCTION |
| RWD | 00h | Read/Write Data (DATA) |
| RWCR | 01h | Read/Write Configuration (CONFIG) |

Configuration Register (CONFIG), 8-BITS, READ/WRITE

| CONFIGURATION REGISTER (CONFIG) | | | | | | | |
|---------------------------------|------|------|------|------|------|------|------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| RESERVED | | | | | | | SHDN |

| BIT | POR | FUNCTION | TYPE | OPERATION |
|-----------|-----|---|-----------|----------------------------|
| D[0] | 0 | STANDBY switch | ReadWrite | 1 = standby, 0 = normal |
| D[7]-D[1] | 0 | Reserved - Always returns zero when read. | N/A | N/A |

Data Register (DATA), 12-Bits, READ/WRITE

Data Register (DATA) for 1st BYTE

| D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] |
|-------|-------|------|------|------|------|------|------|
| MSB | X | X | X | X | X | X | LSB |

Data Register (DATA) for 2nd BYTE

| D[3] | D[2] | D[1] | D[0] | X | X | X | X |
|------|------|------|------|---|---|---|---|
| X | X | X | LSB | X | X | X | X |

The DAC output voltage is a function of reference voltage and the binary value of the contents of the register DATA. The transfer function is given by the expression:

$$V_{OUT} = V_{REF} \times \left[\frac{DATA}{4096} \right]$$

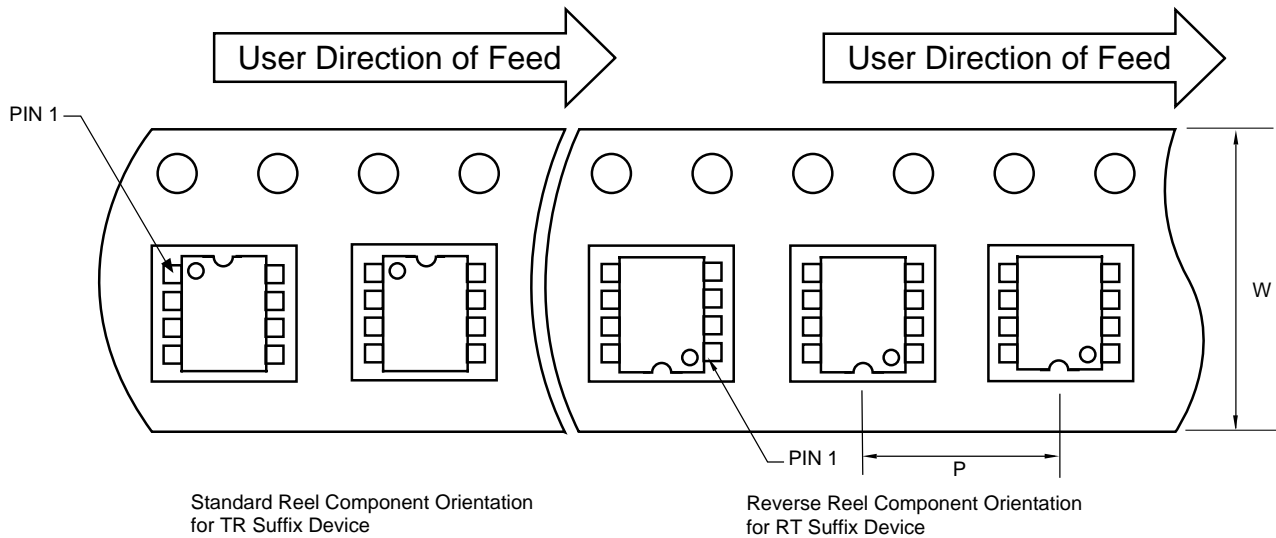
Register Set Summary

The TC1322's register set is summarized below. All registers are 12-bits wide.

| NAME | DESCRIPTION | POR State | READ | WRITE |
|--------|-------------------------------|----------------|------|-------|
| DATA | Data Register (2 BYTE format) | 000000000000b* | ✓ | ✓ |
| CONFIG | CONFIG Register | 0000 0000b | ✓ | ✓ |

TAPING FORM

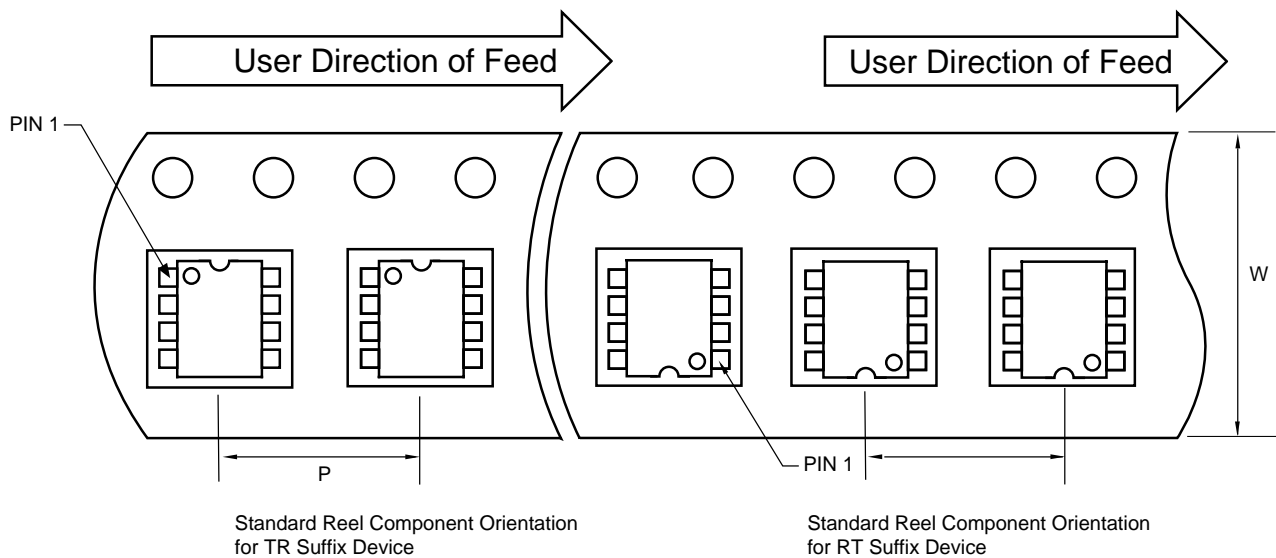
Component Taping Orientation for 8-Pin MSOP Devices



Carrier Tape, Number of Components Per Reel and Reel Size

| Package | Carrier Width (W) | Pitch (P) | Part Per Full Reel | Reel Size |
|------------|-------------------|-----------|--------------------|-----------|
| 8-Pin MSOP | 12 mm | 8 mm | 2500 | 13 in |

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



Carrier Tape, Number of Components Per Reel and Reel Size

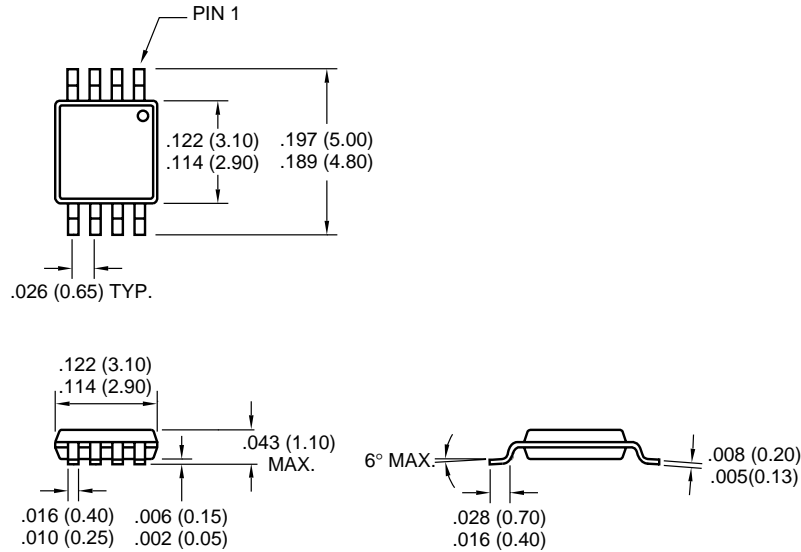
| Package | Carrier Width (W) | Pitch (P) | Part Per Full Reel | Reel Size |
|----------------|-------------------|-----------|--------------------|-----------|
| 8-Pin SOIC (N) | 12 mm | 8 mm | 2500 | 13 in |

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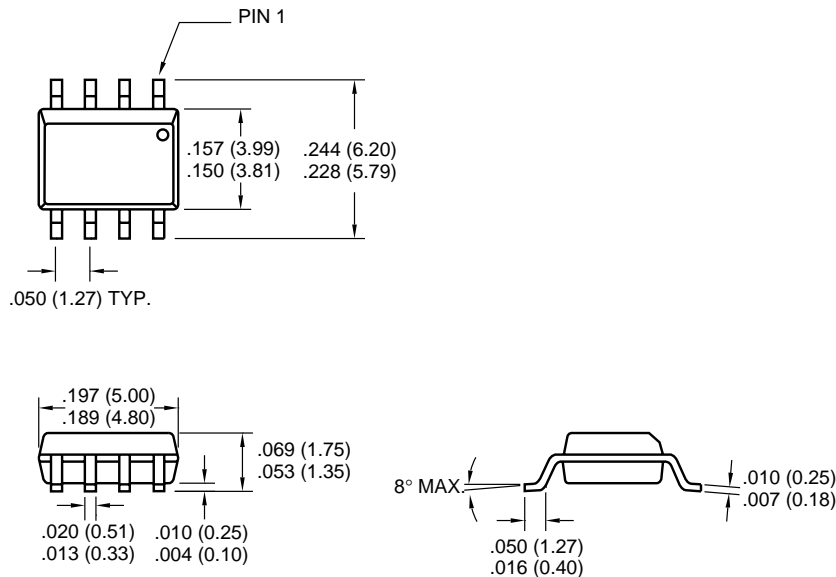
TC1322

PACKAGE DIMENSIONS

8-Pin MSOP



8-Pin SOIC (Narrow)



Dimensions: inches (mm)

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