August 1990
Edition 2.0

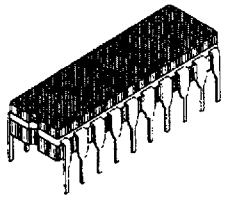
FUJITSU

DATA SHEET

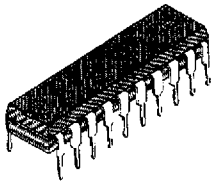
MB40874
CHANNEL 4-BIT D/A CONVERTER

1 CHANNEL 4-BIT D/A CONVERTER WITH LOOK-UP TABLE (50 MSPS)

The Fujitsu MB40874 is a 50-MSPS (mega sample per second) 4-bit digital-to-analog converter with look-up table (LUT). The MB40874 is designed for high-speed video application with video RAM. The LUT is a 16-word, 4-bit memory to store luminance data. Instead of changing video RAM data, LUT data updating makes quick luminance changes in monochrome video application and quick color changes in color video application.



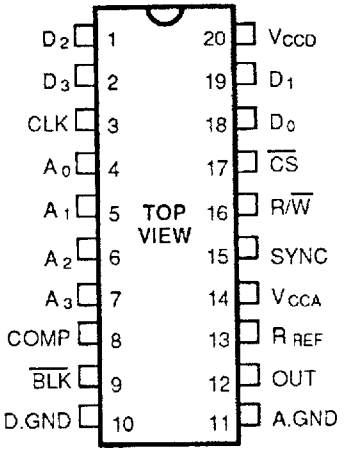
CERAMIC PACKAGE
DIP-20C-C01



PLASTIC PACKAGE
DIP-20P-M02

- Resolution: 4 bits
- Linearity : ±1/2 LSB maximum
- Operation frequency: 50 MSPS minimum
- Analog output voltage: 4.0V to 5.0V
- Digital input: TTL compatible
- Power supply voltage: +5V
- Power dissipation: 430 mW typical
- Package: 20-pin Cerdip (Suffix: -Z)
  20-pin plastic DIP (Suffix: -P)

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see Note)

Rating		Symbol	Value	Unit
Power supply voltage		V_{CCA} V_{CCD}	-0.5 to +7.0	V
Digital input voltage		V_I	-0.5 to +7.0	V
Digital output voltage		V_{INA}	-0.5 to V_{CC} +0.5	V
Storage temperature	Plastic	T_{STG}	-55 to +125	°C
	Ceramic		-65 to + 150	

Note : Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

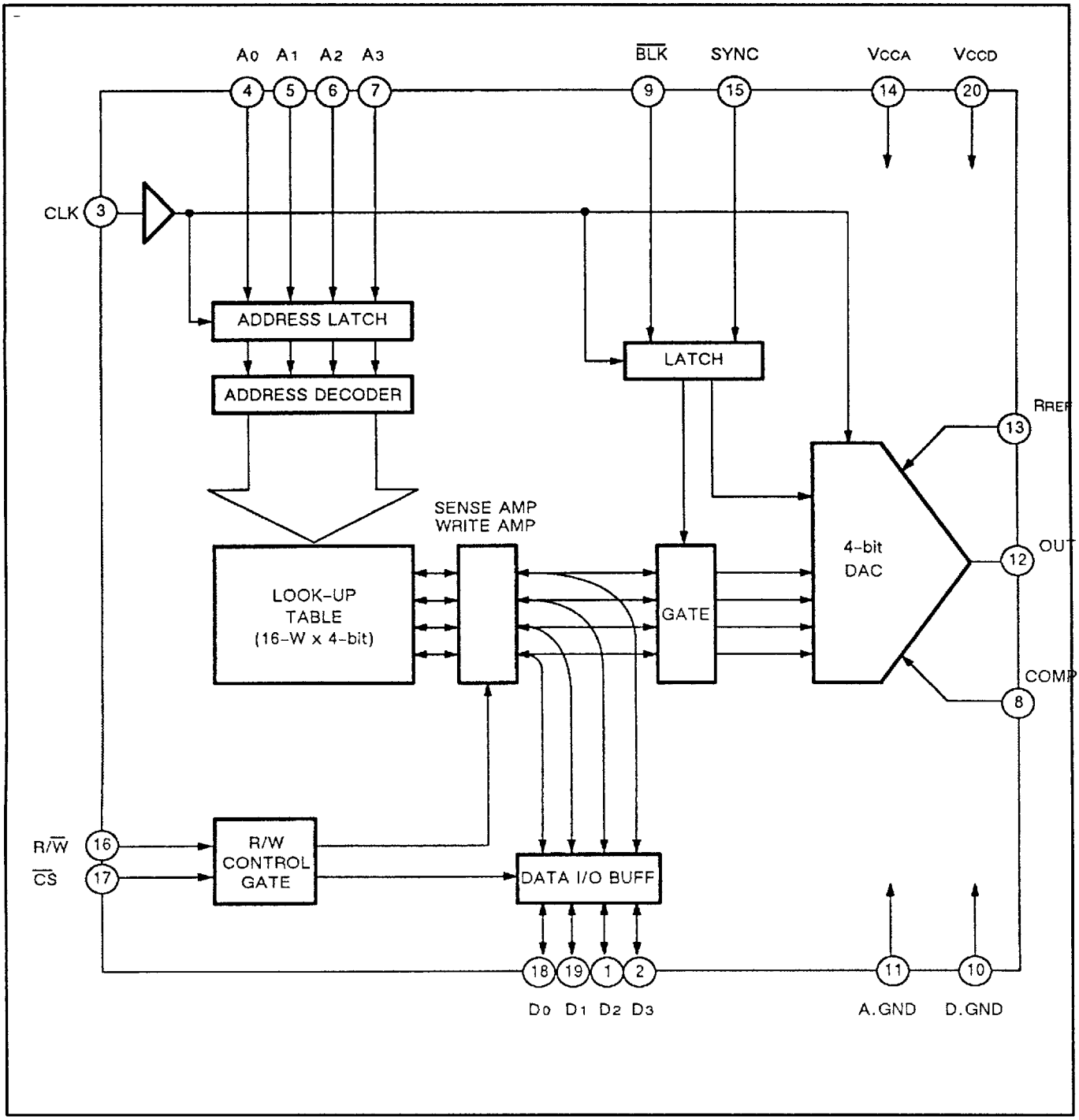


Figure 1. MB40874 Block Diagram

PIN DESCRIPTION

Pin No.	Pin Name	Description
1, 2, 18, 19	D0 to 03	Data input/output to read/write LUT data
3	CLK	Clock Input for digital-to-analog operation; operation speed is dependent on this input. At the rising edge of this input, A0 to A3, $\overline{BLK}$, and SYNC are latched, and converted signal outputs at OUT.
4 to 7	A0 to A3	Address input for LUT; during displaying time, dot data from VRAM is input. During display's flying line period, address is input in order to write or read the data of LUT.
8	COMP	Terminal for phase compensation capacitance; capacitance of 1 μF or more should be inserted between COMP and A.GND.
9	$\overline{BLK}$	Input to make OUT at blank level; when $\overline{BLK}$ is at low level, OUT is at blank level. When $\overline{BLK}$ is at high level, content of LUT is converted and outputs at OUT.
10	A. GND	Ground for analog circuit
11	D.GND	Ground for digital circuit
12	OUT	Output of digital-to-analog converter; load resistance should be inserted between OUT and V_{CC}.
13	R_{REF}	Terminal for reference resistance; reference resistor should be inserted between R_{REF} and V_{CCA}.
15	SYN	C-input for exclusive-ORed vertical/horizontal synchronous signal; this input is used to obtain composite output. SYNC input should be input while $\overline{BLK}$ is at low level.
16	R/$\overline{W}$	Mode switch for read/write of LUT. This input is effective when $\overline{CS}$ is at low level. When R/$\overline{W}$ is at high level, read mode is selected. When R/$\overline{W}$ is at low level, write mode is selected.
17	$\overline{CS}$	Chip select for LUT read/write mode
18	V_{CCA}	Power supply pin for analog circuit
20	V_{CCD}	Power supply pin for digital circuit

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage[1]	V_{CC} V_{CCD}	4.75	5.00	5.25	V
Output high current	I_{OH}			-400	μA
Output low current	I_{OL}			8	mA
CLK frequency	f_{CLK}			50	MHz
Phase compensation capacitance	C_{COMP}*	1			μF
Operating temperature	T_A	0		70	°C

*Phase compensation capacitance should connect between COMP and A.GND.

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC}= +5V ±5%, T_A=0 to 70°C, unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					4	bits
Linearity Error	LE				±1/2	LSB
WHITE level output voltage	V_W		V_{CCA} -15	V_{CCA}	V_{CCA} +15	mV
BLACK level output voltage	V_B	V_{CCA} = 5.000V R_{REF} = 300Ω Output is pulled up to V_{CCA} at 37.5Ω		4.357		V
BLANK level output voltage	V_{BLANK}			4.286		V
SYNC level output voltage	V_{SYNC}			4.000		V
DAC output voltage	ΔV_{DAC}		0.9	1.0	1.1	V
SYNC output voltage	ΔV_{SYNC}		236	286	336	mV
BLANK output voltage	ΔV_{BLANK}		5	10(71 mv)	15	IRE*
GRAY output voltage	ΔV_{GRAY}		85	90(634 mV)	95	IRE*

*IRE: The ratio of a reflection signal composition (V_{BLANK} to V_W) and a syncronous signal composition (V_{SYNC} to V_{BLANK}) is a 100:40 on EIA R5343A standard. 1/140 of the sum (reflection signal composition and synchronous signal composition) is named 1 IRE, which is used as unit of a reflection signal.

ELECTRICAL CHARACTERISTICS (Continued)

DIGITAL DC CHARACTERISTICS

(V_{CC}= +5V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input high voltage	V_{IH}			2.0			V
Input low voltage	V_{IL}					0.8	V
Input cramp voltage	V_{IC}	V_{CC} = 4.75V, I_I = -18mA				-1.5	V
Input high current	I_{IH}	V_{CC} = 5.25V	V_I = 7V			100	µA
			V_I = 2.7V			20	
Input low current	I_{IL}	V_{CC} = 5.25V				0.4	V
Output high voltage[1]	V_{OH}	V_{CC} = 4.75V, I_{OH} = −400 µA		2.7	3.4		V
Output low voltage	V_{OL}	V_{CC} = 4.75V	I_{OL} = 4mA		0.25[2]	0.4	V
			I_{OL} = 8mA		0.35[2]	0.5	
Output short current	I_{OS}	V_{CC} = 5.25V[3]		-20		-100	mA
Output current Off condition (Hi-Z)	I_{OZ}	V_{CC} = 5.25V	V_O = 2.4V			100	µA
			V_O = 0.4V			-20	
Power Supply Current	I_{CC}	V_{CC} = 5.25V				120	mA

[1] Except common I/O of D_0 to D_3
[2] V_{CC} =+5V, T_A = 25°C
[3] Time of output short should be within 1 second

SWITCHING CHARACTERISTICS

VIDEO OUTPUT

(V_{CC} = +5.0V ±5%, T_A = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
CLK cycle time	t_{CLK}	20			ns
CLK high pulse width	t_{WCLK+}	7			ns
CLK low pulse width	t_{WCLK-}	7			ns
Address. $\overline{BLK}$, SYNC high pulse width	t_{WV+}	18			ns
Address. $\overline{BLK}$. SYNC low pulse width	t_{WV-}	18			ns
Address, $\overline{BLK}$, SYNC setup time	t_{SV}	6			ns
Address, $\overline{BLK}$. SYNC hold time	t_{HV}	3			ns
Propagation time	t_{PD}			25	ns

ELECTRICAL CHARACTERISTICS, continued

SWITCHING CHARACTERISTICS, continued

LUT Access (Read)

(V_{CC} = +5.0V ±5%, T_A = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CS}$ pulse width low level time	t_{WCSR}	100			ns
R/$\overline{W}$ setup time	t_{SRWR}	10			ns
R/$\overline{W}$ hold time	t_{HRWR}	10			ns
$\overline{BLK}$ setup time	t_{SBR}	$2 \cdot t_{CLK}+6$			ns
$\overline{BLK}$ hold time	t_{HBR}	$t_{CLK}+3$			ns
Address setup time	t_{SAR}	$2 \cdot t_{CLK}+6$			ns
Address hold time	t_{HAR}	$t_{CLK}+3$			ns
Data setup time	t_{DEN}			50	ns
Data hold time	t_{DDIS}	15		50	ns

LUT Access (Write)

(V_{CC} = +5.0V ±5%, T_A = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CS}$ pulse width low level time	t_{WCSW}	100			ns
R/$\overline{W}$ setup time	t_{SRWW}	10			ns
R/$\overline{W}$ hold time	t_{HRWW}	10			ns
$\overline{BLK}$ setup time	t_{SBW}	$2 \cdot t_{CLK}+6$			ns
$\overline{BLK}$ hold time	t_{HBW}	$t_{CLK}+3$			ns
Address setup time	t_{SAW}	$2 \cdot t_{CLK}+6$			ns
Address hold time	t_{HAW}	$t_{CLK}+3$			ns
Data setup time	t_{SD}	10			ns
Data hold time	t_{HD}	10			ns

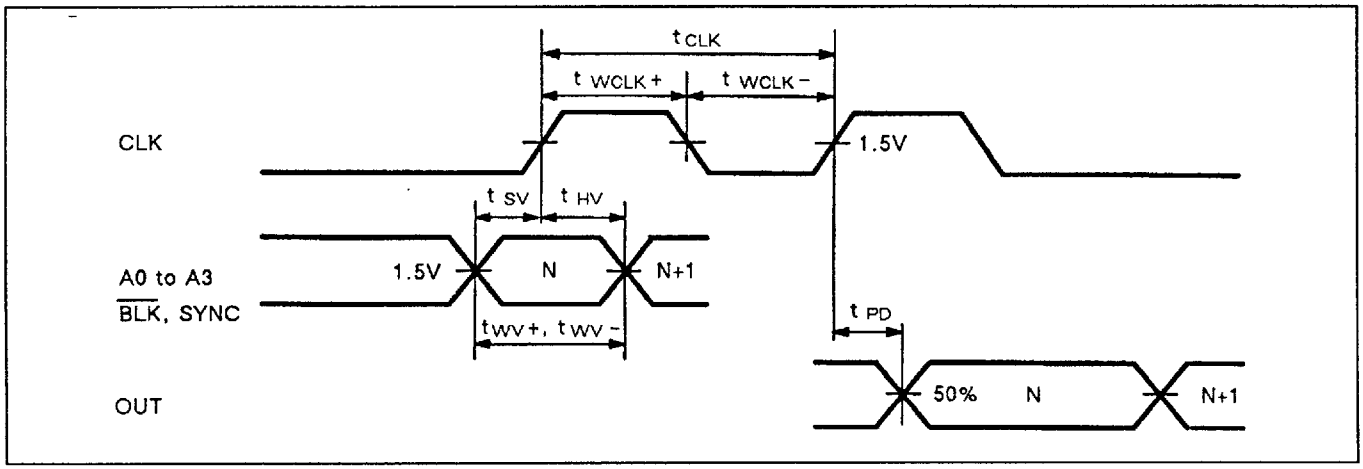


Figure 2. Video Output Timing Diagram

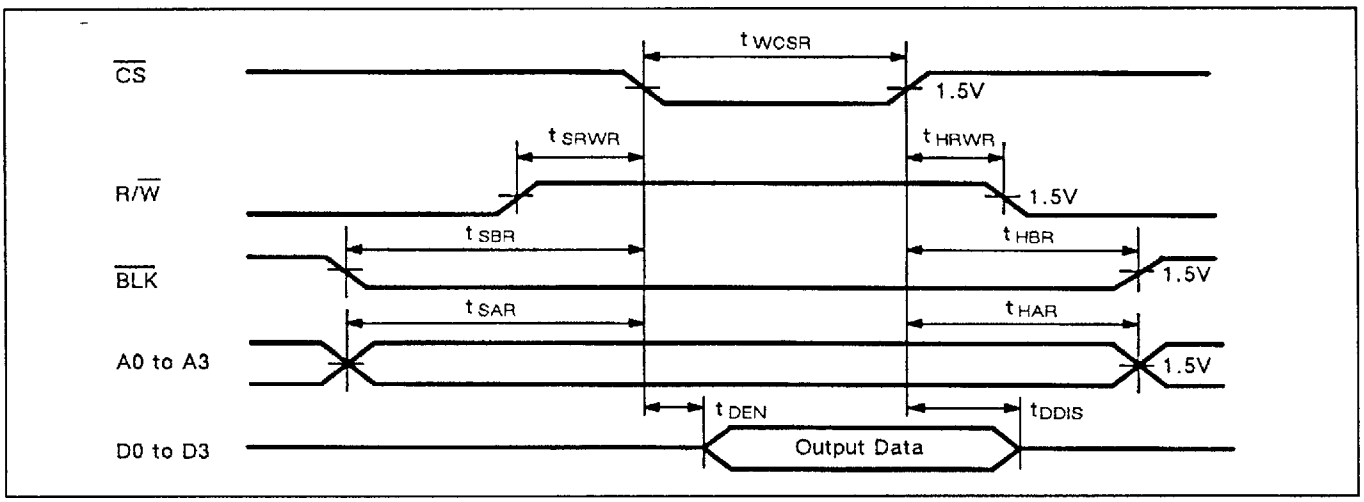


Figure 3. LUT Access (Read) Timing Diagram

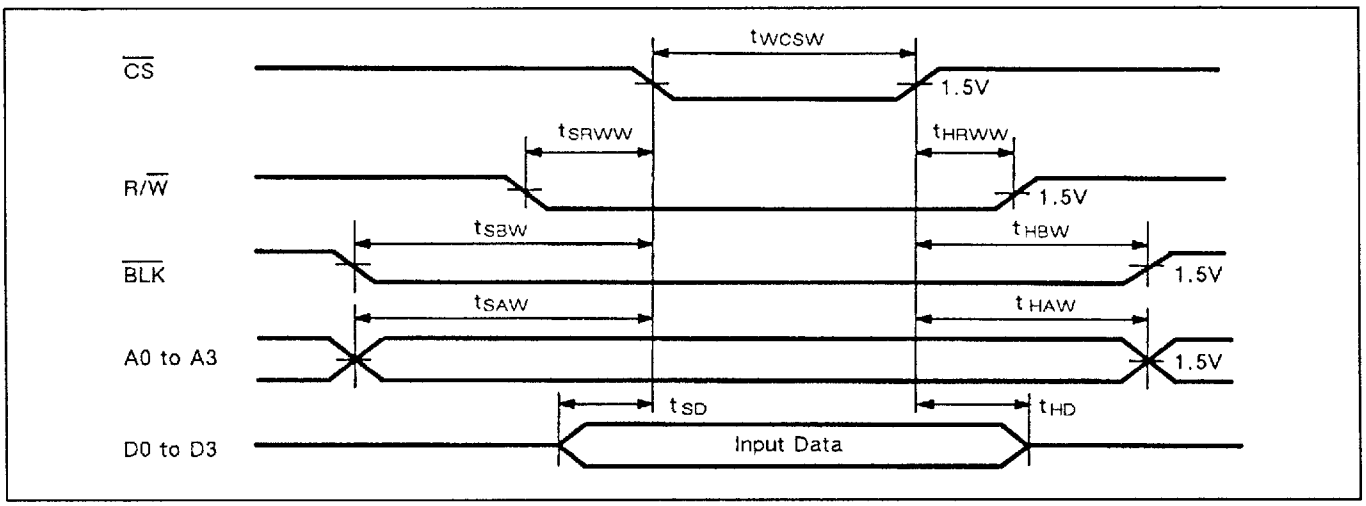
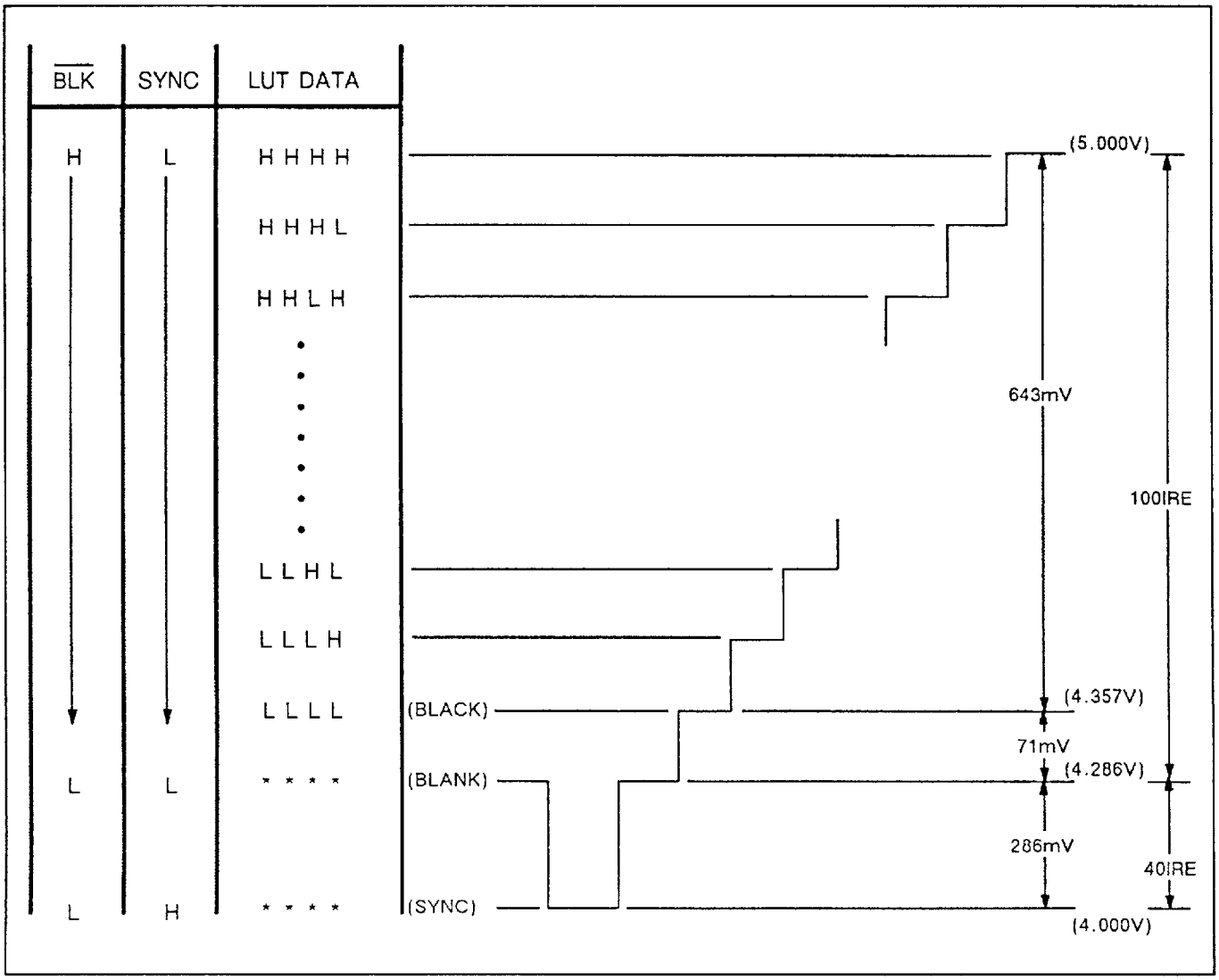


Figure 4. LOT Access (Write) Timing Diagram



* Don't Care
Output is pulled up to V_{CCA} at 37.5Ω

Figure 5. DAC Output Voltage

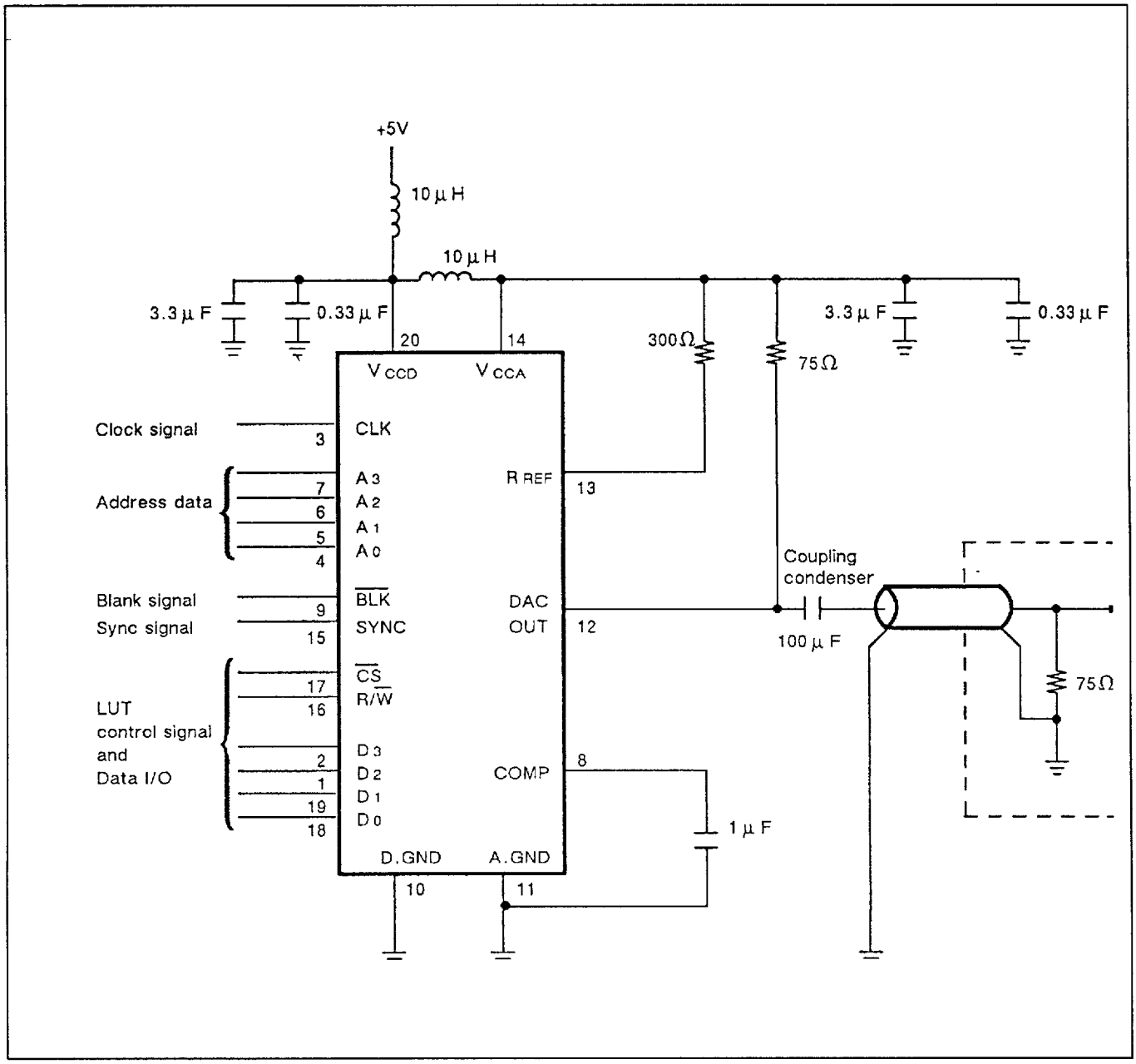


Figure 6. MB40874 Connection Circuit Example

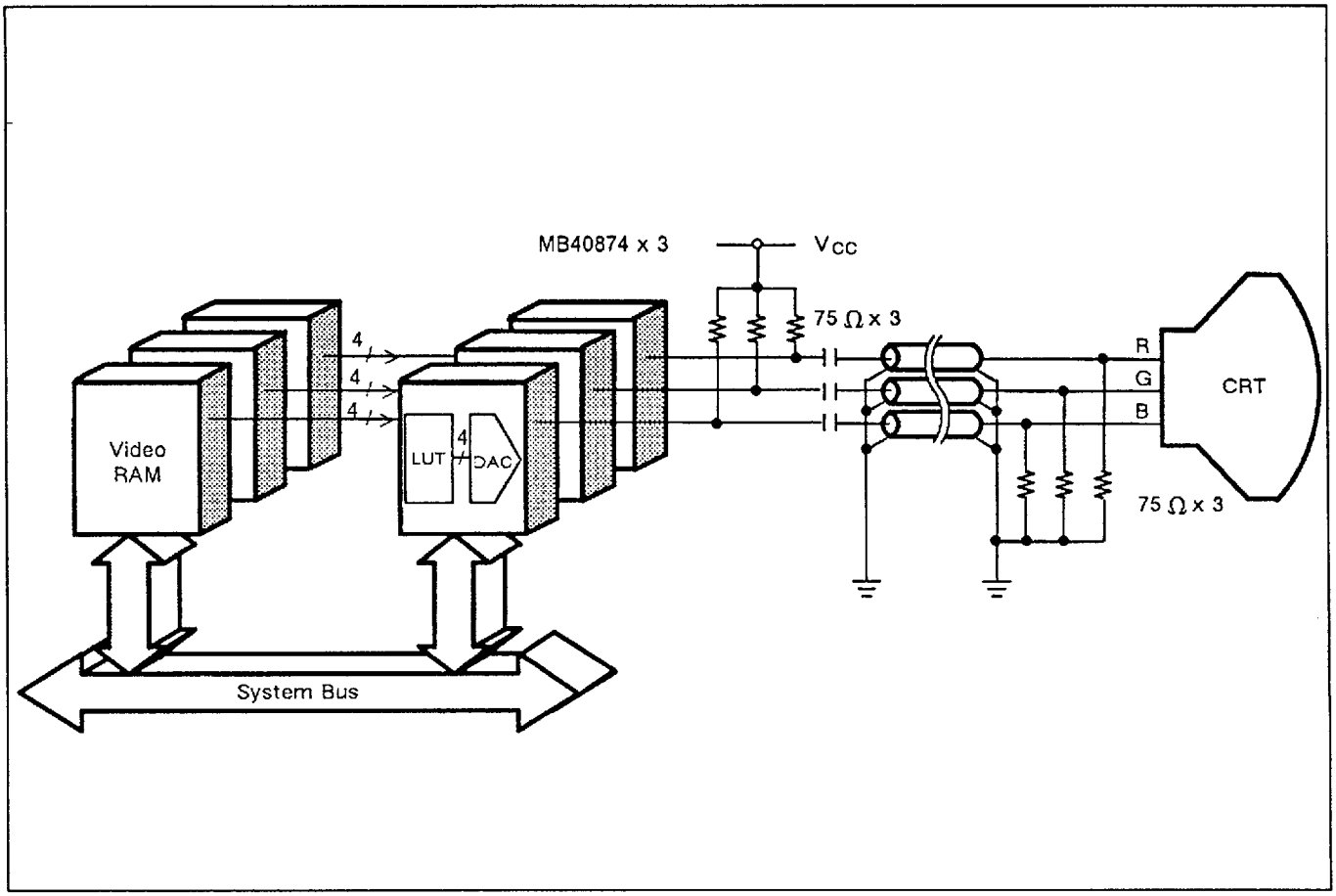
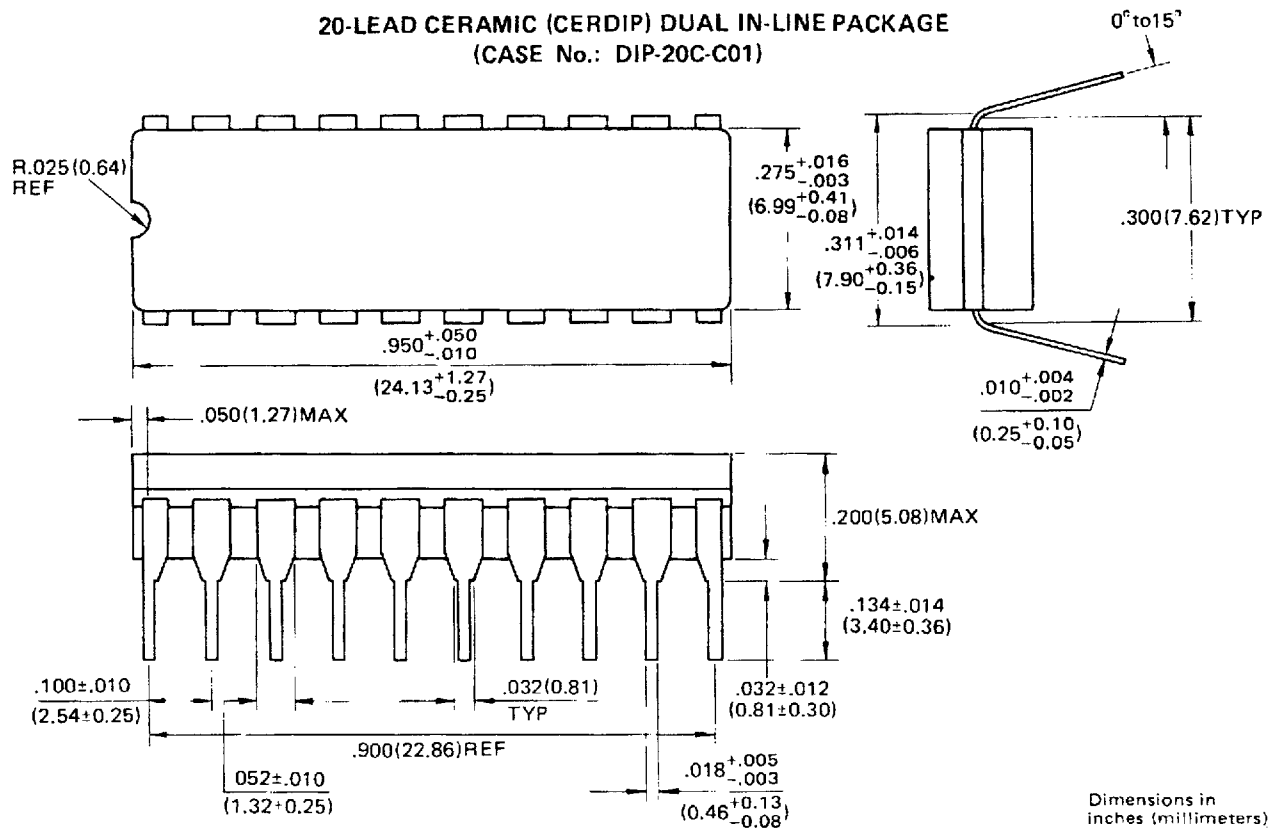


Figure 7. Application Information

The above application is an example of RGB system using three pieces of MB40874. The system allows user to simultaneously display whole 4096 type of color defined by the bit number of LUT and D/A converter and promptly change color tone.

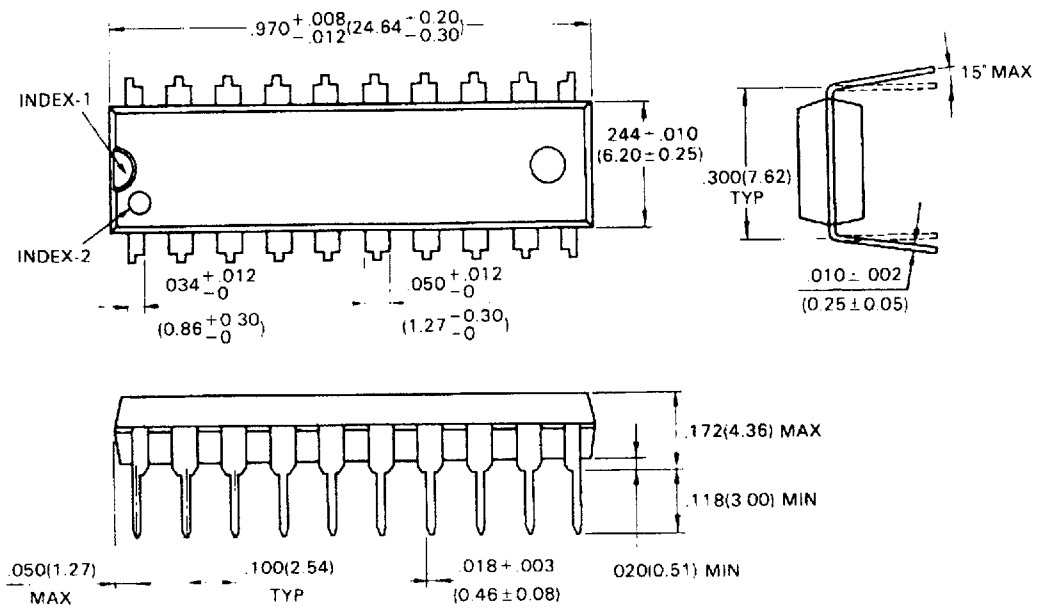
PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C01)



20-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-20P-M02)



Dimensions in inches (millimeters)

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