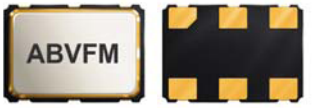
# CMOS/PECL/LVDS SMD VOLTAGE CONTROLLED CRYSTAL CLOCK OSCILLATOR

## ABVFM SERIES




RoHS Compliant

5.0 x 7.0 x 2.0mm

### FEATURES:

- Based on a proprietary analog multiplier
- Tri-State Output
- Ultra low Phase Jitter
- 2.5V or 3.3V +/- 10% operation
- Ceramic SMD, low profile package

### APPLICATIONS:

- xDSL, Cable Modems
- Customer Premise Equipment (CPE)
- ATM, SONET, SDH, STB
- LAN / WAN Data Communications Equip.
- 155.52MHz, 311.04MHz, 622.08MHz applications

### STANDARD SPECIFICATIONS:

| PARAMETERS | |
|---|---|
| ABRACON P/N: | ABVFM Series |
| Frequency range: | 1.544MHz to 80 MHz (Fund or 3rd OT), Up to 200MHz (Mutiplier) CMOS<br>12MHz to 800 MHz (Fund, or Multiplier) PECL or LVDS |
| Operating temperature: | 0 °C to + 70 °C (see options) |
| Storage temperature: | - 55° C to + 125° C |
| Overall frequency stability: | ± 100 ppm max. (see options) |
| Supply voltage (Vdd): | 3.3V ±10% (See options) |
| Control voltage (Vc): | 1.25±1.0V (2.5Vdd), 1.65±1.35V (3.3Vdd) |
| Linierity: | +10% |
| Pullability: | ±50ppm minimum (see options) |
| RMS Phase Jitter (12KHz - 20MHz): | 0.6ps typical, 1ps max. |
| Period Jitter (Peak to peak): | 35 ps max. |
| Low Phase Noise: | -120 dBc/Hz @ 1kHz Offset from 251.2MHz<br>-125 dBc/Hz @ 10kHz Offset from 251.2MHz<br>-130 dBc/Hz @ 100KHz Offset from 251.2MHz |
| Tristate Function: | "1" ($V_{IH}$≥0.7*Vdd) or open: Oscillation<br>"0" ($V_{IL}$< 0.3*Vdd): No Oscillation / Hi Z |
| Aging (First year): | ± 3 ppm max. |
| **PECL:** Supply current ($I_{DD}$): | 25mA max (for Fo<24MHz),60mA max (for 24.01MHz<Fo<100MHz)<br>70mA max (100.01MHz<Fo<800MHz) |
| Output Logic High: | 1.475V min (2.5Vdd), 2.275V min. (3.3Vdd) |
| Output Logic Low: | 1.095V max (2.5Vdd), 1.680V max. (3.3Vdd) |
| Symmetry (Duty Cycle): | 50±5% |
| Rise time: | 1.0ns (12 to 100MHz), 0.5ns (100.01 to 800MHz) |
| Fall time: | 1.0ns (12 to 100MHz), 0.5ns (100.01 to 800MHz) |
| Tristate function (See options) : | "1" (VIH >= 0.7*Vdd) or open: Oscillation<br>"0" (VIL < 0.3*Vdd) : Hi Z |
| **LVDS:** Supply current ($I_{DD}$): | 25mA max (for Fo<24MHz),60mA max (for 24.01MHz<Fo<100MHz)<br>60mA max (100.01MHz<Fo<800MHz) |
| Output Differential Voltage ($V_{OD}$) | 247mV min, 355mV typical, 454mV max |
| Output High Voltage ($V_{OH}$): | 1.4V typical, 1.6V max. |
| Output Low Voltage ($V_{OL}$): | 0.9V min, 1.1V typical |
| Symmetry (Duty Cycle): | 50±5% |
| Offset Voltage [$R_L$= 100Ω,] $V_{OS}$: | 1.125V min, 1.2V typical, 1.375V max |
| Rise Time ($t_r$) [$R_L$= 100Ω, CL=10pF]: | 1.0ns (12 to 100MHz), 0.5ns (100.01 to 800MHz) |
| Fall Time ($t_f$) [$R_L$= 100Ω, CL=10pF]: | 1.0ns (12 to 100MHz), 0.5ns (100.01 to 800MHz) |
| Tristate function (See options) : | "1" (VIH >= 0.7*Vdd) or open: Oscillation<br>"0" (VIL < 0.3*Vdd) : Hi Z |



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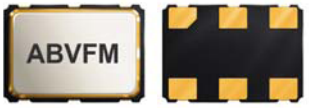


5.0 x 7.0 x 2.0mm

## PARAMETERS - continued

| | | |
|---|---|---|
| **CMOS:** | Supply current ($I_{DD}$): | 3mA max (for Fo<24MHz),30mA max (for 24.01MHz<Fo<80MHz), 60mA max (80.01MHz<Fo<200MHz) |
| | Output Logic High: | 0.9*Vdd |
| | Output Logic Low: | 0.1*Vdd |
| | Symmetry (Duty Cycle): | 50±5% |
| | Rise time: | 5.0ns (1.54 to 24MHz), 4ns (24.01 to 80MHz), 3ns (80.01 to 200MHz) |
| | Fall time: | 5.0ns (1.54 to 24MHz), 4ns (24.01 to 80MHz), 3ns (80.01 to 200MHz) |
| | Output load: | 15 pF max. |
| | Tristate function (See options) : | "1" (VIH >= 0.7*Vdd) or open: Oscillation<br>"0" (VIL < 0.3*Vdd) : Hi Z |
| | Start-up time: | 6ms max |

## OPTIONS AND PART IDENTIFICATION:

(Left blank if standard)

**ABVFM□-Frequency-□-□-□-□-□**

| Supply Voltage | |
|---|---|
| Blank* | 3.3V |
| 2 | 2.5V |

* 3.3V: Standard

| Freq. Stability | |
|---|---|
| Blank* | ±100ppm |
| R | ±25ppm |
| C | ±50ppm |

| Packaging | |
|---|---|
| T | Tape and Reel (1000pcs) |

| Operating Temperture Options | |
|---|---|
| Blank* | 0°C to +70°C |
| D | -10°C to +60°C |
| E | -20°C to +70°C |
| F | -30°C to +70°C |
| N | -30°C to +85°C |
| L | -40°C to +85°C |

*Standard Specification

| Output | |
|---|---|
| PE | PECL |
| LV | LVDS |
| CM | CMOS |

| Pullability | |
|---|---|
| Blank | ±50ppm |
| N100 | ±100ppm |
| N150 | ±150ppm |

**TRI-STATE PIN OUT DESCRIPTION:**

| OUTPUT TYPE OPTION | | PIN 1 logic level* | Output State |
|---|---|---|---|
| **PE** | **PECL** | 0 | Enabled |
| | | 1 | Tri-state |
| **LV** | **LVDS** | 0 | Tri-state |
| | | 1 | Enabled |
| **CM** | **CMOS** | 0 | Tri-state |
| | | 1 | Enabled |

*Connect to VDD for logic level "1", connect to ground for logic level "0".



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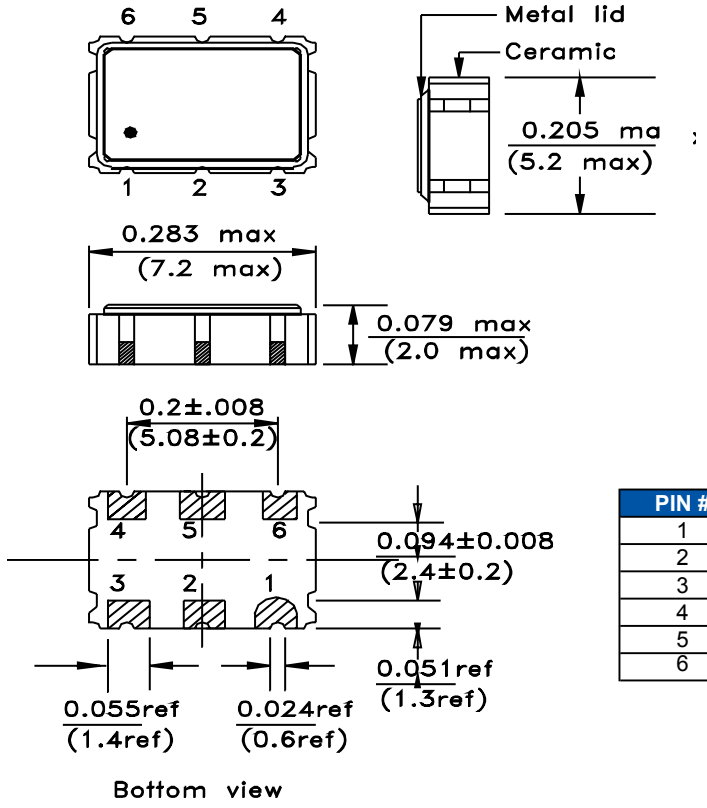
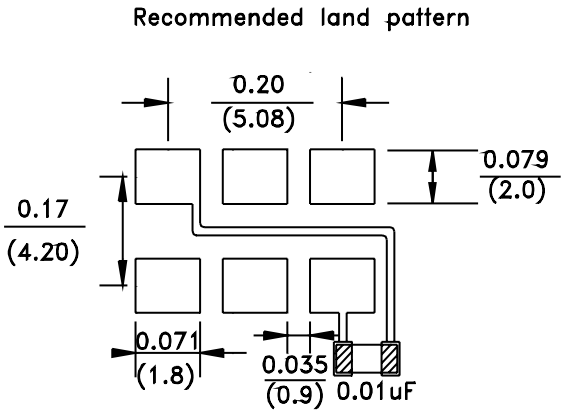
## OUTLINE DIMENSIONS:



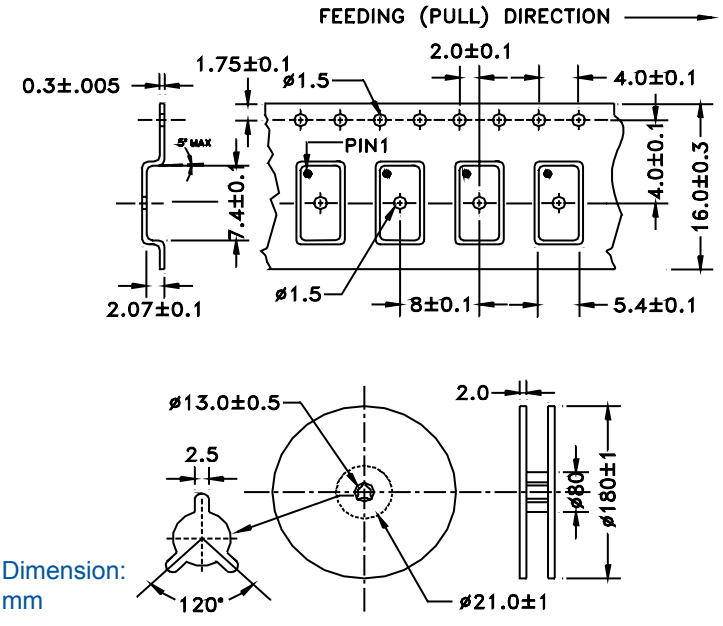




| PIN # | Name | DESRIPTION |
|---|---|---|
| 1 | Vc | Controll voltage |
| 2 | NC / Tristate | No Connect / Tristate |
| 3 | GND | Ground |
| 4 | Q | PECL, LVDS, or CMOS Output. |
| 5 | $\overline{Q}$ | Complimentary PECL,LVDS, or NC. |
| 6 | $V_{DD}$ | VDD Connection. |

Note: Recommend using an approximately 0.01uF bypass capacitor between PIN 3 and 6.

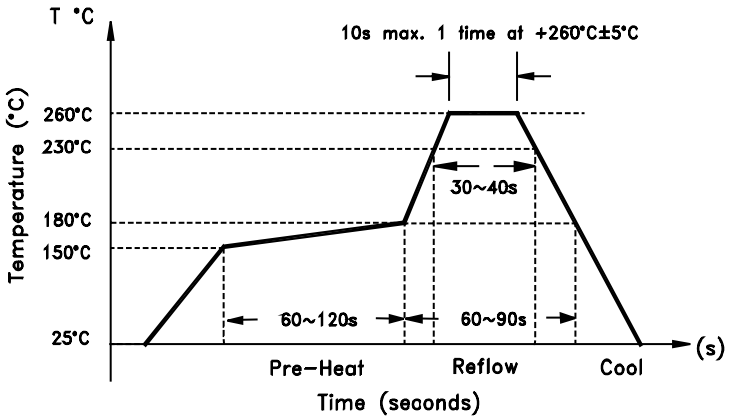
Dimension : Inches (mm)

## TAPE AND REEL: T= tape and reel (1,000pcs/reel)




Dimension: mm

## REFLOW PROFILE:





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