Z89121
Z89921* (*ROMLESS)
16-BIT MIXED SIGNAL PROCESSOR

FEATURES

- Z8® Microcontroller with 43 I/O Lines (27 I/O Lines for the Z89921)
- 24 Kbytes of Z8 Program ROM (Z89121)
- 256 Bytes On-Chip Z8 RAM
- Watch-Dog Timer and Power-On Reset
- Low Power STOP Mode
- On-Chip Oscillator which Accepts a Crystal or External Clock Drive
- Two 8-Bit Z8 Counter/Timers with 6-Bit Prescaler
- Low Power Consumption - 200 mW (typical)
- Two Comparators with Programmable Interrupt Priority
- Six Vectored, Z8 Prioritized Interrupts
- RAM and ROM Protect
- Clock Speed of 20.48 MHz
- 16-Bit Digital Signal Processor (DSP)
- 6K Words DSP Program ROM
- 512 Words On-Chip DSP RAM
- 10-Bit PWM D/A Converter (4 kHz to 64 kHz)
- Z8 and DSP Operation in Parallel
- Three Vectored, Prioritized DSP Interrupts
- IBM® PC-Based Development Tools
- Interface for Two Codecs with 8 kHz and 6.66 kHz Sampling Rate and 2.048 MHz Clock
- Two DSP Timers to Support Different Sampling Rates for Codecs and PWM
- Built-in DRAM Interface. Direct Support of up to 48 Mbit DRAM with 4-Bit Wide Data Bus

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GENERAL DESCRIPTION

The Z89121/921 is a dual CPU 16-bit mixed signal processor designed for digital audio compression plus storage systems. The I/O control processor is a Z8® with 24 Kbytes of program memory, two 8-bit counter timers, a DRAM controller with up to 48 Mbit accessibility and up to 43 I/O pins. The DSP is a 16-bit processor with a 24-bit ALU and accumulator, 512 x 16 bits of RAM, single cycle instructions, and 6K word program ROM. The chip also contains a 10-bit PWM D/A converter and interface for two Codecs. The sampling rates for the PWM and Codec interface are programmable.

The Z8 and DSP processors are coupled by mailbox registers and an interrupt system. DSP or Z8 programs may be directed by events in each other's domain.

The Z89921 is the ROMless version of the Z89121. The DSP is not ROMless. The DSP's program memory is always the internal ROM.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

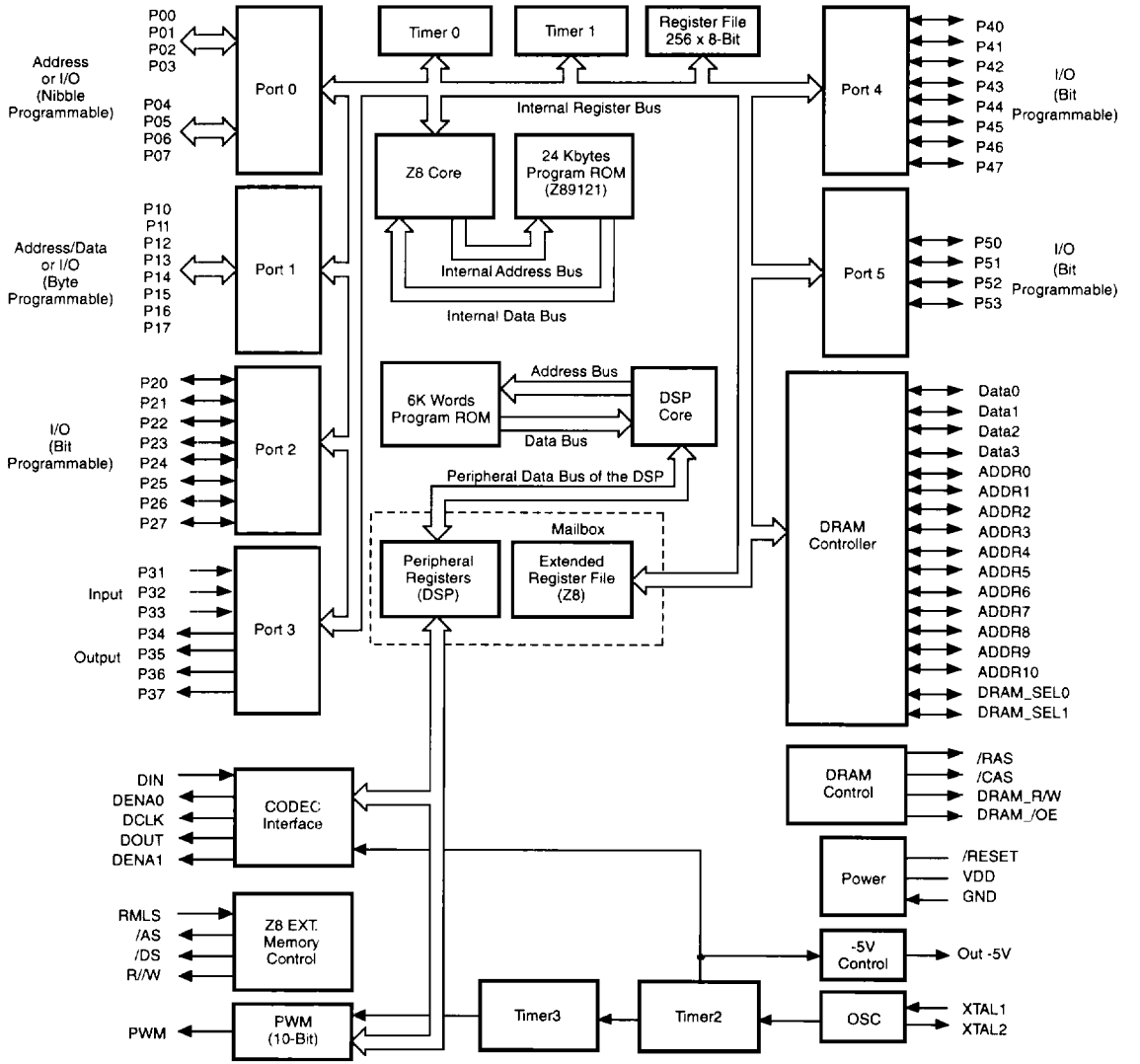

Figure 1. Functional Block Diagram

Z8 Core Processor

The Z8 is Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripheral and I/O circuits. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features. The Z8 also excels in many industrial uses, high-volume processing, peripheral controllers and consumer applications.

For applications demanding powerful I/O capabilities, the Z89121/921 has 43 pins dedicated to input and output. These lines are grouped into six ports. Each port is configurable under software control to provide timing, status signals and parallel I/O with or without handshake.

Four basic memory resources for the Z8 are available to support a wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File. The Z8 core processor is characterized by an efficient register file that allows any of 256 on-board data and control registers to be the source and/or the destination of almost any instruction. Traditional microprocessor Accumulator bottlenecks are eliminated.

The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The Expanded Register File consists of mailbox registers, WDT mode register, DSP Control register, Stop-Mode Recovery register, Port Configuration register, and the control and data registers for Port 4 and Port 5.

To unburden the software from supporting real-time problems, such as counting/timing and data communication, the Z8 offers two on-chip counter/timers with a large number of user selectable modes.

Watch-Dog Timer and STOP-Mode Recovery features are software driven by setting specific bits in control registers.

Stop and Halt instructions support reduced power operation. The low power STOP mode allows parameter information to be stored in the register file if power fails. An external capacitor or battery retains power to the device.

DSP Coprocessor

The DSP coprocessor is a second generation, 16-bit two's complement CMOS Digital Signal Processor (DSP). Four external DSP registers are mapped into the expanded register file of the Z8. Communication between the Z8 and the DSP occurs through those common registers which form the mailbox registers.

The analog signal is generated by a 10-bit resolution Pulse Width Modulator. The PWM output is a digital signal with CMOS output levels. The output signal has a resolution of 1 in 1024 with a sampling rate of 16 kHz (XTAL = 20.48 MHz). The sampling rate can be changed under software control and can be set at 4, 10, 16, and 64 kHz. The dynamic range of the PWM is from 0 to 4 volts.

Two additional timers (Timer2 and Timer3) have been added to support different sampling rates for the Codec interface and Pulse Width Modulator. These timers are free-running counters that divide the crystal frequency.

PIN DESCRIPTION (Continued)

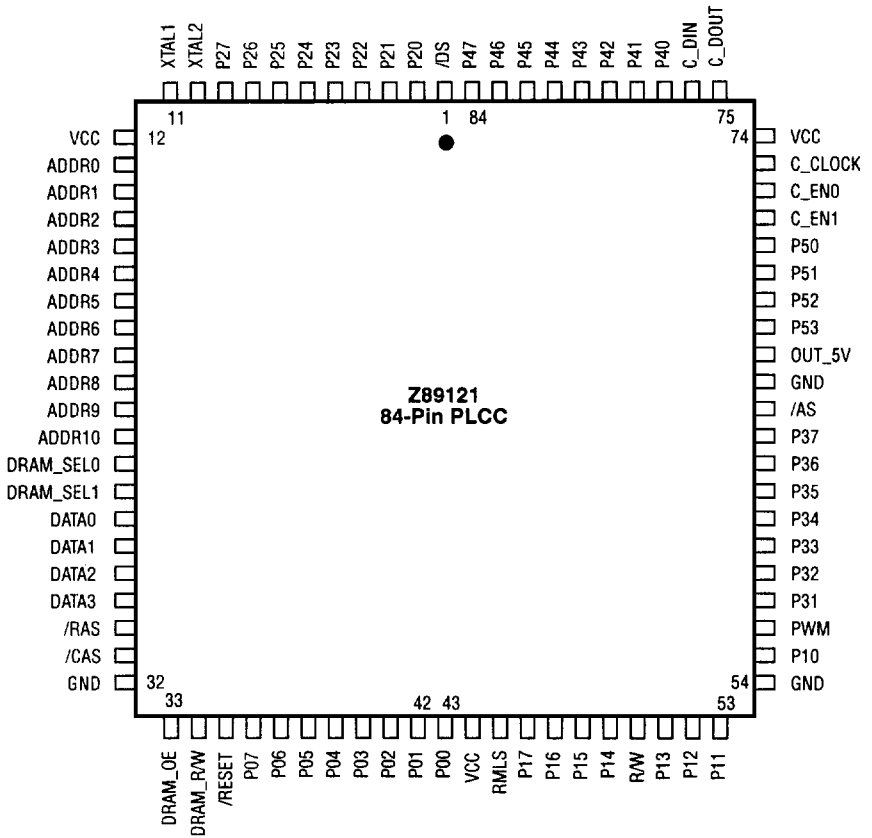

Figure 2. Z89121 84-Pin PLCC Pin Assignments

Table 1. Z89121 84-Pin PLCC Pin Identification

I/O Port Functions	Pin Number	I/O	Function
V_{SS}	32, 54, 65		Digital Ground
V_{CC}	12, 44, 74		Digital V_{CC} = +5V
P07-P00	43-36	Input/Output	P07-P00 (General purpose nibble programmable I/O port.)
P17-P10	55, 53-51, 49-46	Input/Output	P17-P10 (General purpose byte programmable I/O port.)
P27-P20	2-9	Input/Output	P27-P20 (General purpose bit programmable I/O.)
P37-P31	57-63	Input/Output	P37-P31 (General purpose I/O port. Bits P31-P33 are inputs, while bits P37-P34 are outputs.)
P47-P40	77-84	Input/Output	P47-P40 (General purpose bit programmable I/O.)
P53-P50	70-67	Input/Output	P53-P50 (General purpose bit programmable I/O.)
C_DIN	76	Input	Data input from Codec.
C_DOUT	75	Output	Data output to Codec.
C_CLOCK	73	Output	Codec clock (2.048 MHz)
C_ENA0	72	Output	Codec0 enable (8 kHz)
C_ENA1	71	Output	Codec1 enable (8 kHz)
PWM	56	Output	Pulse Width Modulator output
DATA0	26	Input/Output	Data 0 I/O of the DRAM Interface
DATA1	27	Input/Output	Data 1 I/O of the DRAM Interface
DATA2	28	Input/Output	Data 2 I/O of the DRAM Interface
DATA3	29	Input/Output	Data 3 I/O of the DRAM Interface
ADDR0	13	Output	Address 0 line of the DRAM Interface
ADDR1	14	Output	Address 1 line of the DRAM Interface
ADDR2	15	Output	Address 2 line of the DRAM Interface
ADDR3	16	Output	Address 3 line of the DRAM Interface
ADDR4	17	Output	Address 4 line of the DRAM Interface
ADDR5	18	Output	Address 5 line of the DRAM Interface
ADDR6	19	Output	Address 6 line of the DRAM Interface
ADDR7	20	Output	Address 7 line of the DRAM Interface
ADDR8	21	Output	Address 8 line of the DRAM Interface
ADDR9	22	Output	Address 9 line of the DRAM Interface
ADDR10	23	Output	Address 10 line of the RAM Interface for 4 Meg ARAMs. Select 2 output of DRAM Interface for 1 Meg ARAMs support. The latter mode is used to switch between different pages of ARAM.
DRAM_SEL0	24	Output	Select0 output of DRAM Interface. Used to switch between different pages of DRAM.
DRAM_SEL1	25	Output	Select1 output of DRAM Interface. Used to switch between different pages of DRAM.
/RAS	30	Output	Row Address Strobe of DRAM Interface.
/CAS	31	Output	Column Address Strobe of DRAM Interface.
DRAM_R/W	34	Output	Read/Write Strobe of DRAM Interface.
DRAM_/OE	33	Output	Output Enable Strobe of DRAM Interface.
XTAL1	11	Input	20.48 MHz crystal input
XTAL2	10	Output	20.48 MHz crystal output
ROMless	45	Input	Z8 ROMless mode input (P0 and P1 are switched to D/A mode if this pin is connected to V_{CC}). Internally this pin is tied to GND.
/Reset	35	Input	/RESET input
R/W	50	Output	Z8 external memory interface R/W output
/AS	64	Output	Z8 external memory interface /AS output
/DS	1	Output	Z8 external memory interface /DS
OUT_5V	66	Output	-5V charge pump

PIN DESCRIPTION (Continued)

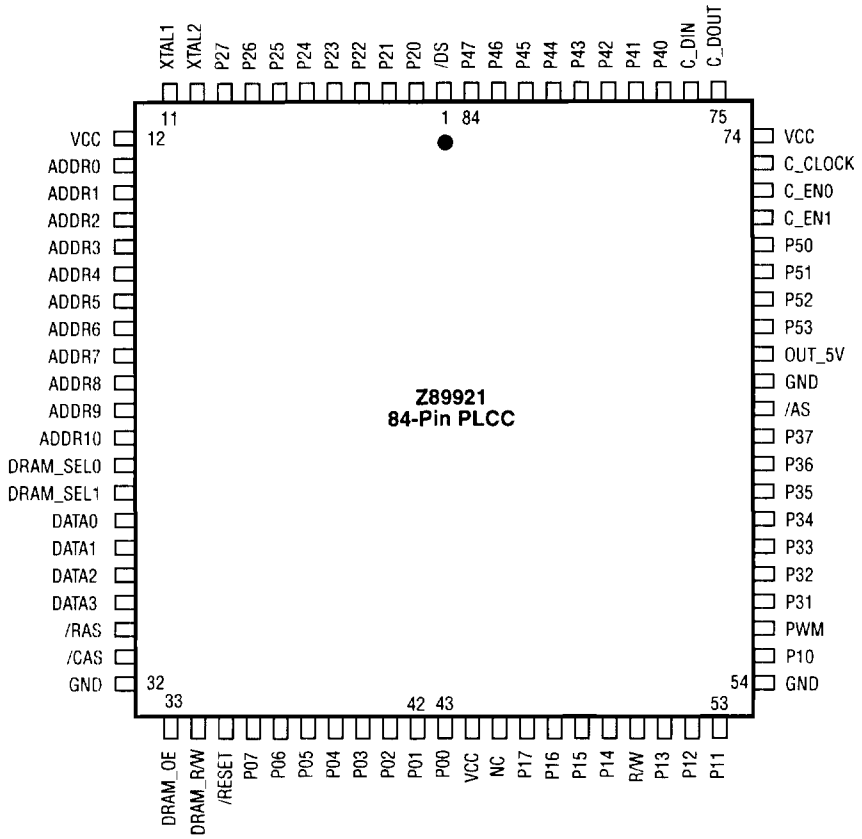

Figure 3. Z89921 84-Pin PLCC Pin Assignments

Table 2. Z89921 84-Pin PLCC Pin Identification

I/O Port Functions	Pin Number	I/O	Function
V_{SS}	32, 54, 65		Digital Ground
V_{CC}	12, 44, 74		Digital V_{CC} = +5 V
P07-P00	43-36	Input/Output	P07-P00 (General purpose nibble programmable I/O port.)
P17-P10	55, 53-51, 49-46	Input/Output	P17-P10 (General purpose byte programmable I/O port.)
P27-P20	2-9	Input/Output	P27-P20 (General purpose bit programmable I/O.)
P37-P31	57-63	Input/Output	P37-P31 (General purpose I/O port. Bits P31-P33 are inputs, while bits P37-P34 are outputs.)
P47-P40	77-84	Input/Output	P47-P40 (General purpose bit programmable I/O.)
P53-P50	70-67	Input/Output	P53-P50 (General purpose bit programmable I/O.)
C_DIN	76	Input	Data input from Codec.
C_DOUT	75	Output	Data output to Codec.
C_CLOCK	73	Output	Codec clock (2.048 MHz)
C_ENA0	72	Output	Codec0 enable (8 kHz)
C_ENA1	71	Output	Codec1 enable (8 kHz)
PWM	56	Output	Pulse Width Modulator output
DATA0	26	Input/Output	Data 0 I/O of the DRAM Interface
DATA1	27	Input/Output	Data 1 I/O of the DRAM Interface
DATA2	28	Input/Output	Data 2 I/O of the DRAM Interface
DATA3	29	Input/Output	Data 3 I/O of the DRAM Interface
ADDR0	13	Output	Address 0 line of the DRAM Interface
ADDR1	14	Output	Address 1 line of the DRAM Interface
ADDR2	15	Output	Address 2 line of the DRAM Interface
ADDR3	16	Output	Address 3 line of the DRAM Interface
ADDR4	17	Output	Address 4 line of the DRAM Interface
ADDR5	18	Output	Address 5 line of the DRAM Interface
ADDR6	19	Output	Address 6 line of the DRAM Interface
ADDR7	20	Output	Address 7 line of the DRAM Interface
ADDR8	21	Output	Address 8 line of the DRAM Interface
ADDR9	22	Output	Address 9 line of the DRAM Interface
ADDR10	23	Output	Address 10 line of the DRAM Interface for 4 Meg ARAMs. Select 2 output of DRAM Interface for 1 Meg ARAMs support. The latter mode is used to switch between different pages of ARAM.
DRAM_SEL0	24	Output	Select0 output of DRAM Interface. Used to switch between different pages of DRAM.
DRAM_SEL1	25	Output	Select1 output of DRAM Interface. Used to switch between different pages of DRAM.
/RAS	30	Output	Row Address Strobe of DRAM Interface.
/CAS	31	Output	Column Address Strobe of DRAM Interface.
DRAM_R/W	34	Output	Read/Write Strobe of DRAM Interface.
DRAM_/OE	33	Output	Output Enable Strobe of DRAM Interface.
XTAL1	11	Input	20.48 MHz crystal input
XTAL2	10	Output	20.48 MHz crystal output
NC	45	Not Connected	
/Reset	35	Input	/RESET input
R/W	50	Output	Z8 external memory interface R/W output
/AS	64	Output	Z8 external memory interface /AS output
/DS	1	Output	Z8 external memory interface /DS output
OUT_5V	66	Output	–5V Charge Pump

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PIN FUNCTIONS

/RESET (input, active Low). Initializes the MCU. Reset is accomplished either through Power-On Reset (POR), Watch-Dog Timer reset, STOP-Mode Recovery, or external reset. During POR and WDT Reset, the internally generated reset signal is driving the reset pin Low for the POR time. Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions. A /RESET will reset both the Z8 and the DSP.

For the Z8:
After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. Program execution begins at location 000CH (hexadecimal), 5-10 TpC cycles after the /RESET is released. The Z8 does not reset WDT, SMR, P2M, and P3M registers on a STOP-Mode Recovery operation.

For the DSP:
A low level on the /RESET pin generates an internal reset signal. The /RESET signal must be kept Low for at least one clock cycle. The CPU will fetch a new Program Counter (PC) value from program memory address 0FFCH after the reset signal is released.

ROMless (input, active High). This pin, when connected to V_{DD}, disables the internal Z8 ROM. (Note, when pulled Low to GND the part functions normally as the ROM version.) The DSP can not be configured as ROMless. This pin is available only on the Z89121.

R/W *Read/Write* (output, write Low). The R/W signal defines the signal flow when the Z8 is reading or writing to external program or data memory. The Z8 is reading when this pin is High and writing when this pin is Low.

/AS *Address Strobe* (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

/DS *Data Strobe* (output, active Low). Data Strobe is activated once for each external memory transfer. For read operations, data must be available prior to the trailing edge of /DS. For write operations, the falling edge of /DS indicates that output data is valid.

XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, or LC network to the on-chip oscillator output.

PWM *Pulse Width Modulator* (output). The PWM is a 10-bit resolution D/A converter. This output is a digital signal with CMOS output levels.

V_{DD}. Digital power supply for the Z89121/921.

GND. Digital ground for the Z89121/921.

C_DIN (input). Data input from Codec.

C_DOUT (output). Data output to Codec.

C_CLOCK (output). 2.048 MHz data rate clock signal output to Codec.

C_ENA0 (output). Enable signal to Codec0

C_ENA1 (output). Enable signal to Codec1.

DRAM_SEL0 (output). Select0 of DRAM.

DRAM_SEL1 (output). Select1 of DRAM.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and the output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction to Port 0 of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble.

The Auto Latch on Port 0 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they are configured by writing to the Port 0 mode register.

In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. (In ROM mode, Port 0 is defined as input after reset.)

Port 0 is set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals /AS, /DS and R/W (Figure 4).

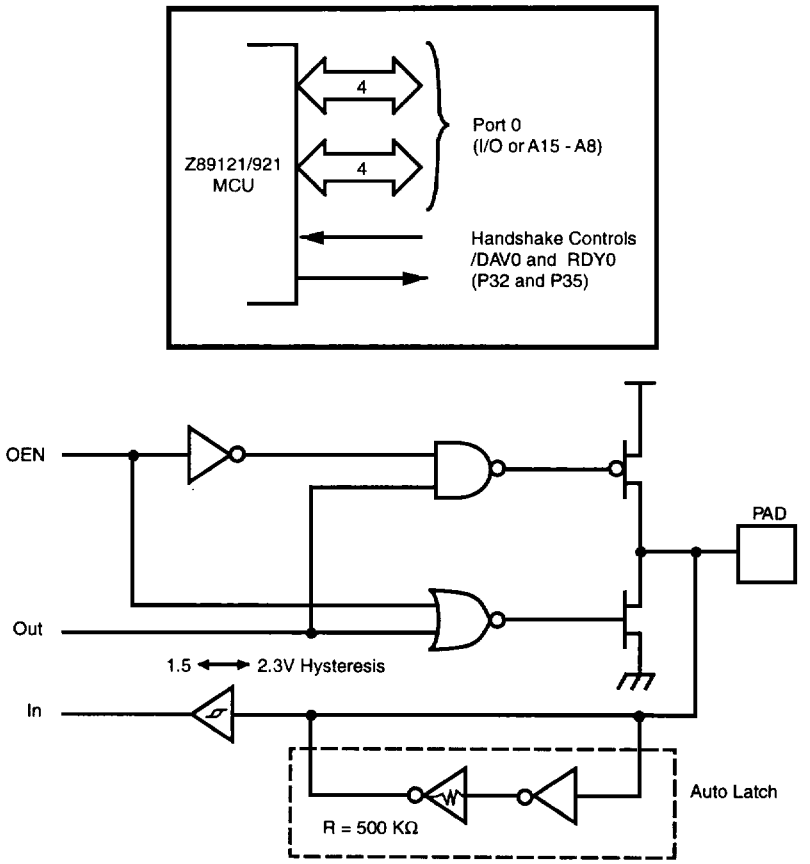


Figure 4. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS compatible port (Figure 5). It has multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines are programmed as inputs or outputs, or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt-triggered and the output drivers are push-pull.

Port 1 may be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake controls RDY1 and /DAV1 (Ready and Data Available). Memory locations greater than 24575 (in ROM mode) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS and R/W, allowing the Z89121/68 to share common resources in multiprocessor and DMA applications.

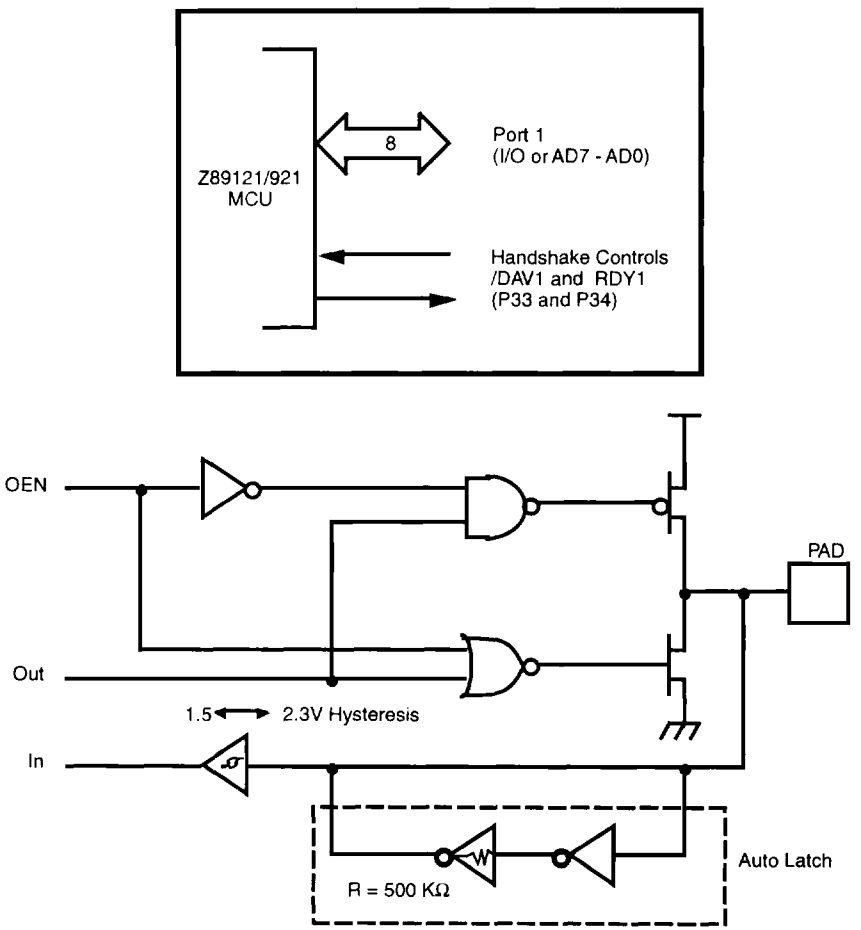


Figure 5. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines are configured under software control independently as inputs or outputs. Port 2 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain.

Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 6).

The Auto Latch on Port 2 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

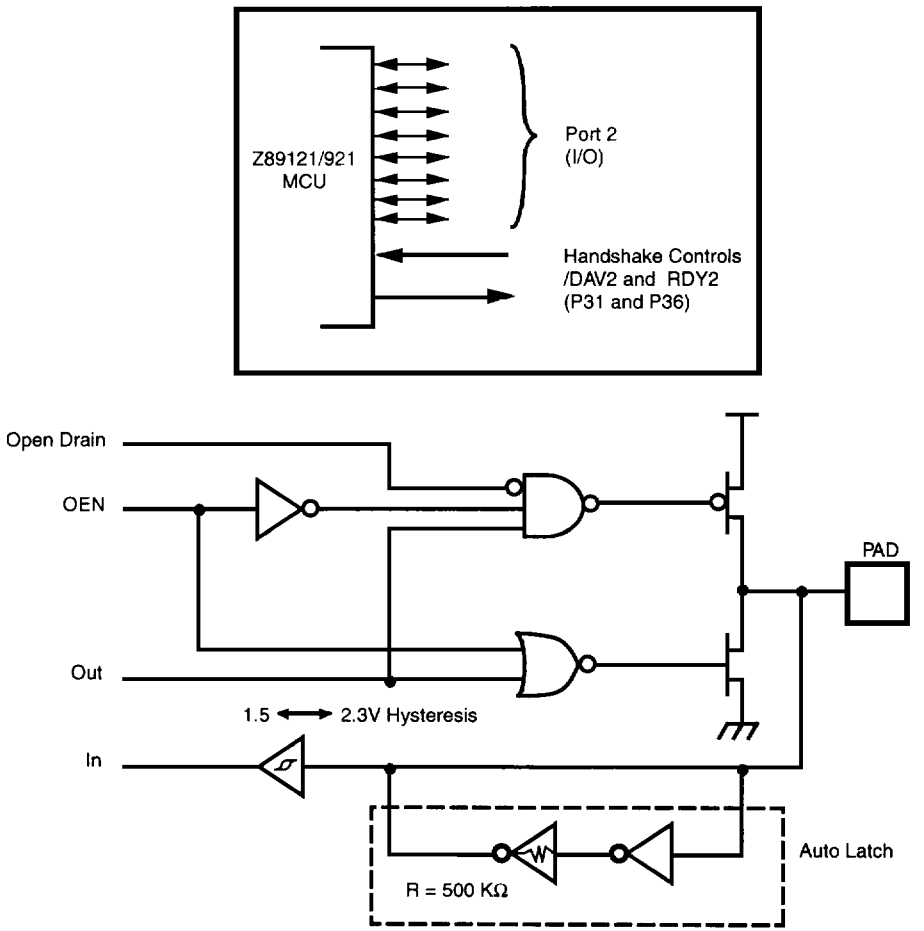


Figure 6. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P31). Port 3 is a 7-bit, CMOS compatible port with three fixed inputs (P33-P31) and four fixed outputs (P37-P34). It is configured under software control for input/output, counter/timers, interrupt, and port handshakes. Pins P33, P32, and P31 are standard CMOS inputs; outputs are push-pull.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). Port 3, pin 3 is a falling edge interrupt input. P31 and P32 are programmable as rising, falling or both edge-triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input. Access to Counter/Timer1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for ports 0, 1, and 2 are available on P31 through P36.

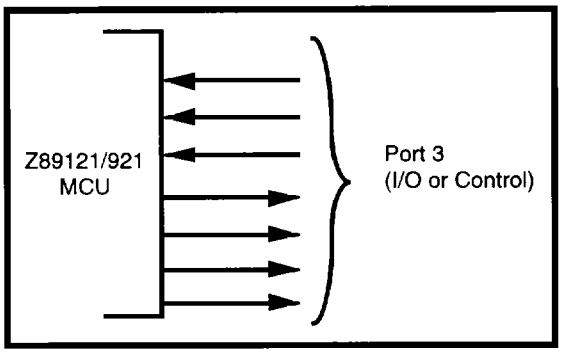
Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); three external interrupt request signals (IRQ3-IRQ1); timer input and output signals (T_{IN} and T_{OUT}); (Figure 7).

Comparator Inputs. Port 3, pins P31 and P32 both have a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In analog mode, P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source.

Table 3. Port 3 Pin Assignments

Pin	I/O	CTC1	AN IN	Int.	P0 HS	P1HS	P2 HS	EXT
P31	IN	T_{IN}	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT					R/D		DM
P35	OUT				R/D			
P36	OUT	T_{OUT}					R/D	
P37	OUT							

Notes:
HS = Handshake Signals
D = DAV
R = RDY



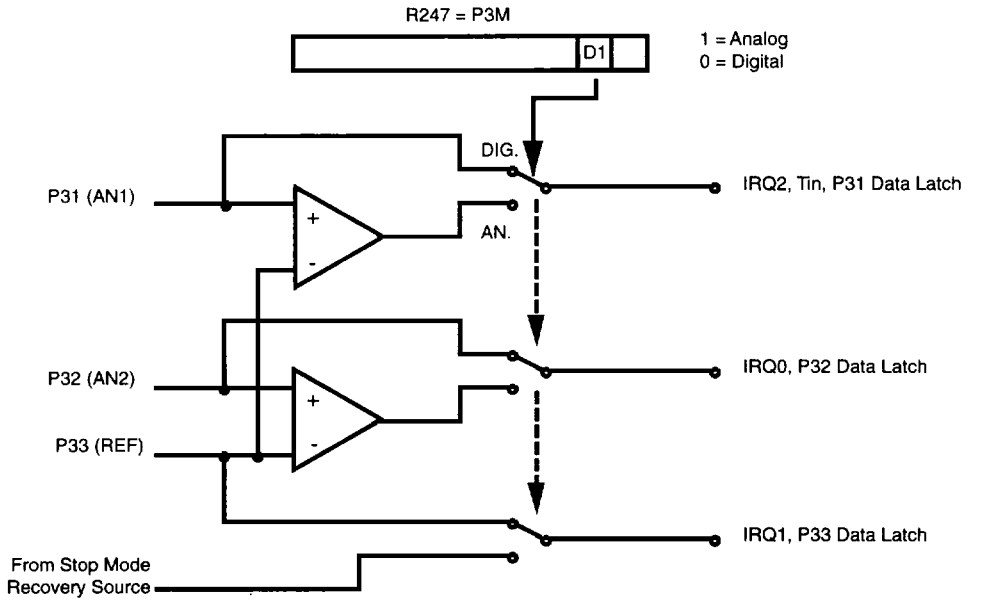


Figure 7. Port 3 Configuration

PIN FUNCTIONS (Continued)

Port 4 (P47-P40). Port 4 is an 8-bit, bidirectional, CMOS compatible I/O port (Figure 8). These eight I/O lines are configured under software control independently as inputs or outputs. Port 4 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain.

Port 4 is a bit programmable general purpose I/O port. The control registers for Port 4 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 4 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

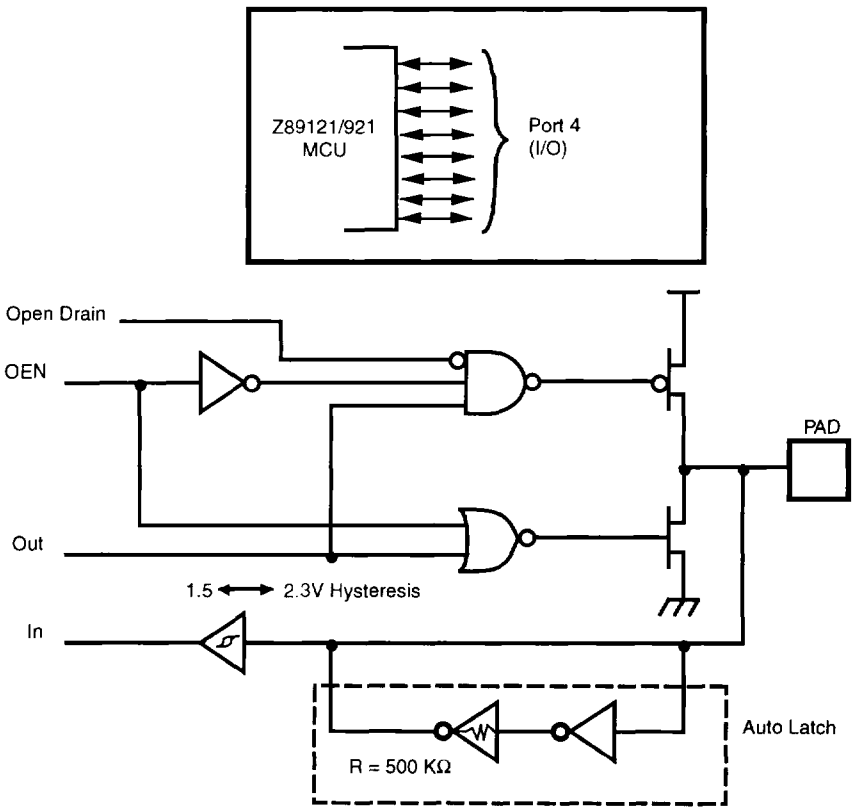


Figure 8. Port 4 Configuration

Port 5 (P53-P50). Port 5 is an 4-bit, bidirectional, CMOS compatible I/O port (Figure 9). These four I/O lines are configured under software control independently as inputs or outputs. Port 5 is always available for I/O operation. The input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain.

Port 5 is a bit programmable general purpose I/O port. The control registers for Port 5 are mapped into the expanded register file (Bank F) of the Z8.

Auto Latch. The Auto Latch on Port 5 puts valid CMOS levels on all CMOS inputs which are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

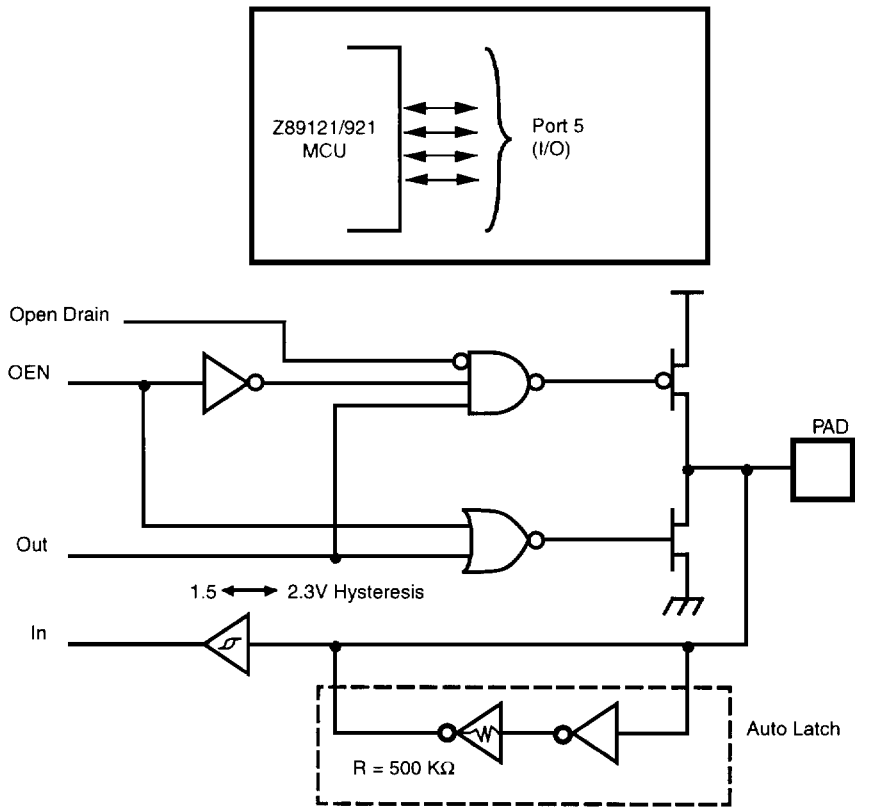


Figure 9. Port 5 Configuration

Z8® FUNCTIONAL DESCRIPTION

The Z8 CCP core incorporates special functions to enhance the Z8's performance in control applications.

Pipelined Instructions. The Z8 instructions (see page 5-66) are comprised of two parts, an instruction fetch and execute part. The instructions typically take between six and ten cycles to fetch and five cycles to execute. Five cycles of the next instruction fetch may be overlapped with five cycles of the current instruction execution. This improves performance over sequential methods. Additionally, the register-based architecture allows any registers to be picked as the source and destination in an instruction saving intermediate move.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP-Mode Recovery Source
- External Reset

Program Memory. The Z8 addresses up to 24 Kbytes of internal program memory and 40 Kbytes external memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors which correspond to the five user interrupts and one DSP interrupt. Byte 12 to byte 24575 consists of on-chip mask-programmed ROM. At addresses 24576 and greater, the Z8 executes external program memory. In ROMless mode, the Z8 will execute from external program memory beginning at byte 12 and continuing through byte 65535.

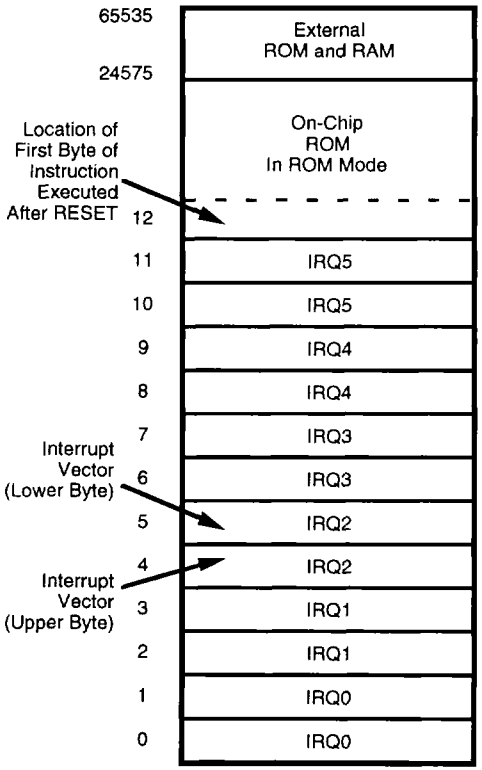


Figure 10. Program Memory Map

ROM Protect. The 24 Kbyte of internal program memory for the Z8 is mask programmable. A ROM protect feature prevents "dumping" of the ROM contents of Program Memory by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions. The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

Data Memory (/DM). In ROM mode, the Z8 can address up to 40 Kbytes of external data memory beginning at location 24576 (Figure 11). In ROMless mode, the Z8 can address the full 64 Kbytes of external data memory beginning at location 12. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on Port 34, is used to distinguish between data and program memory space (Table 3). The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references program (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory.

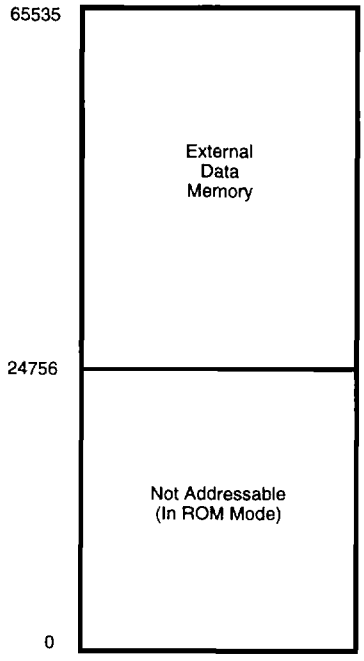


Figure 11. Data Memory Map

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Z8 FUNCTIONAL DESCRIPTION (Continued)

Register File. The standard Z8® register file consists of four I/O port registers, 236 general-purpose registers, and 15 control and status registers (R3-R0, R239-R4, and R255-R241, respectively). The instructions access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 12). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group (Figure 13).

Note: Register Group E (Registers E0-EF) is only accessed through a working register and indirect addressing modes.

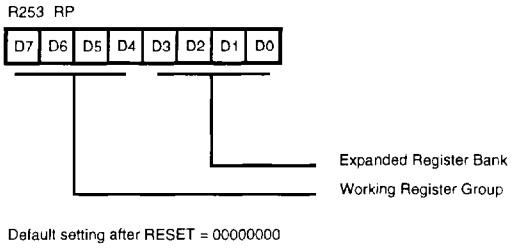

Figure 12. Register Pointer Register

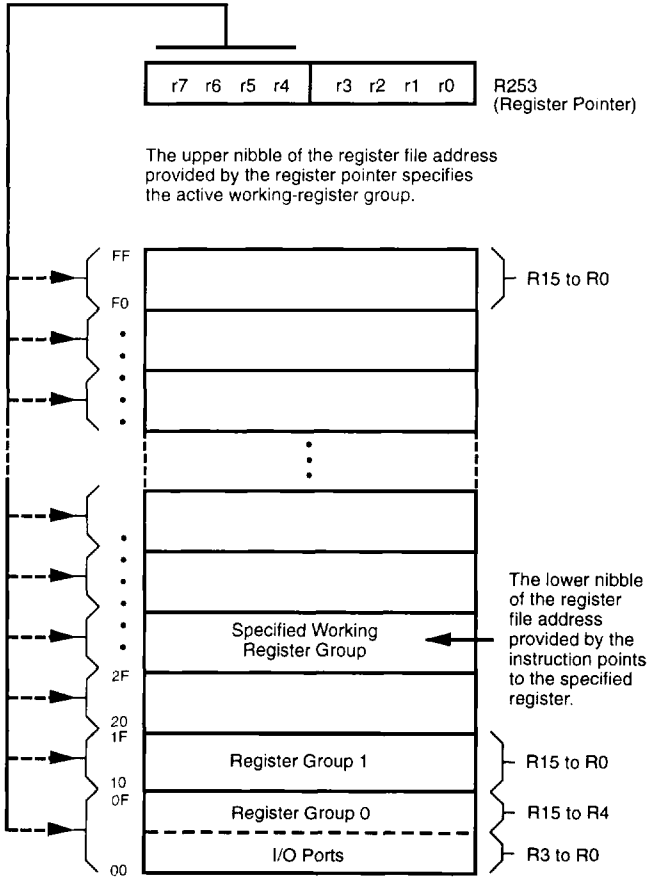

Figure 13. Register Pointer

RAM Protect. The upper portion of the Z8's RAM address spaces 90H to EFH (excluding the control registers) is protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user activates the RAM Protect from the internal ROM code by loading bit D6 in the IMR register to either a 0 (off) or a 1 (on). A 1 in D6 indicates RAM Protect enabled.

Stack. The Z8's external data memory or the internal register file is used for the stack. The 16-bit Stack Pointer (R255-R254) is used for the external stack which can reside only from 24576 to 65535 in ROM mode or 0 to 65535 in ROMless mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). SPH can be used as a general-purpose register when using internal stack only.

Expanded Register File. The register file on the Z8 has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices, along with I/O ports, into the register address area. The Z8 register address space has now been implemented as 16 banks of 16 register groups per bank (Figure 14). These register banks are known as the ERF (Expanded Register File). Bits 7-4 of register RP (Register Pointer) select the working register group. Bits 3-0 of register RP select the expanded register bank (Figure 14).

The SMR register, WDT Register, control and data registers for Port 4 and Port 5, and the DSP control register are located in Bank F of the Expanded Register File. Bank B of the Expanded Register File consists of the Mailbox Interface in which the Z8 and the DSP communicate. The rest of the Expanded Register is not physically implemented and is open for future expansion.

Z8 FUNCTIONAL DESCRIPTION (Continued)

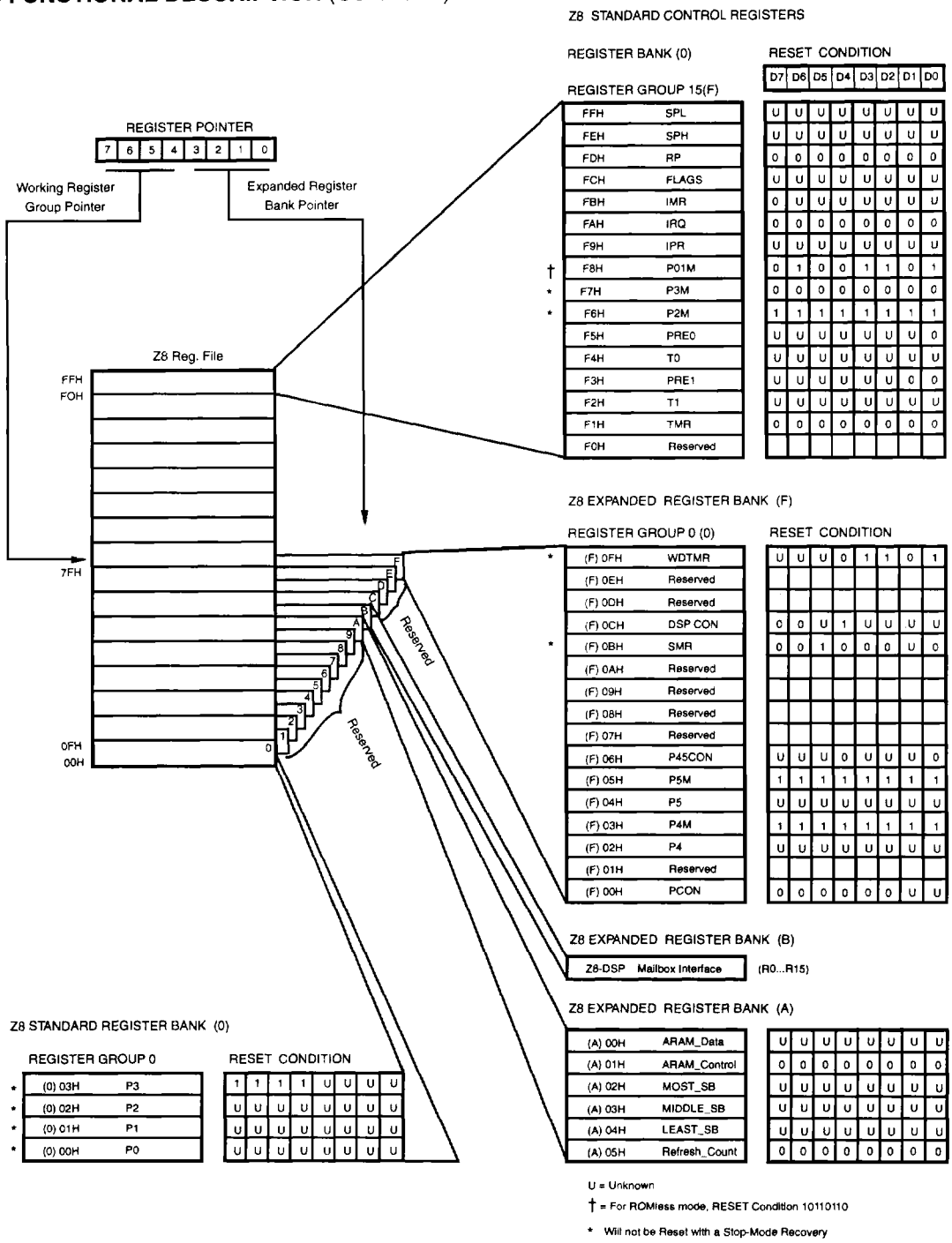

Figure 14. Expanded Register File Architecture

Interrupts. The Z8 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 15). The six sources are divided as follows; three sources are claimed by Port 3 lines P33-P31, two by counter/timers, and one by the DSP (Table 4). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

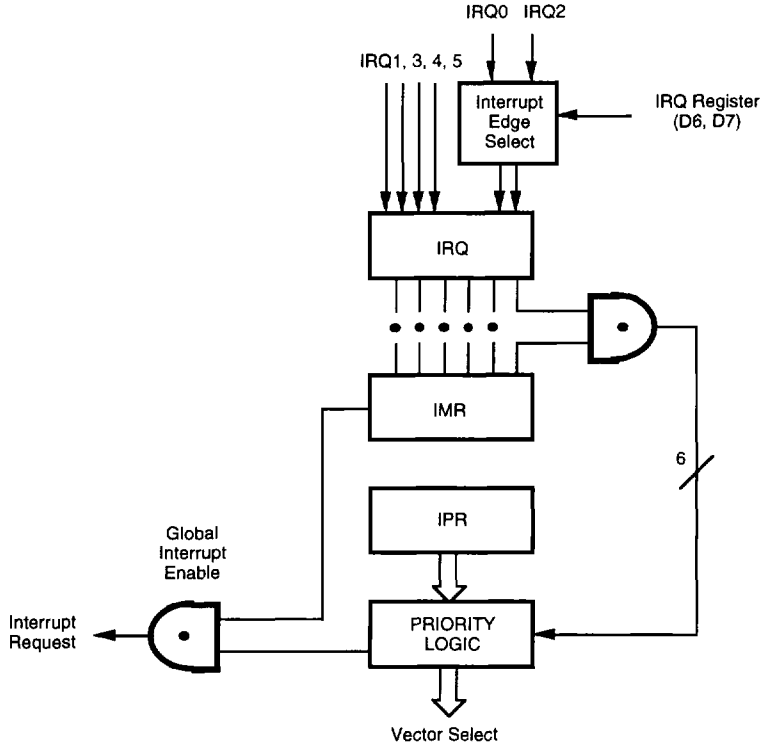

Figure 15. Interrupt Block Diagram

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, P32	0, 1	External (P32), Programmable Rise or Fall Edge Triggered
IRQ1	/DAV1, P33	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, P31, T_{IN}	4, 5	External (P31), Programmable Rise or Fall Edge Triggered
IRQ3	IRQ3	6, 7	Internal (DSP activated), Fall Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	TI	10, 11	Internal

Z8 FUNCTIONAL DESCRIPTION (Continued)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, pushes the Program Counter and Status Flags to the stack, and then branches to the program memory vector location reserved for that interrupt.

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests needs service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 5.

Table 5. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z89121/921 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 20.48 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The system clock (SCLK) is one half the crystal frequency (Figure 16).

The crystal is connected across XTAL1 and XTAL2 using capacitors from each pin to ground.

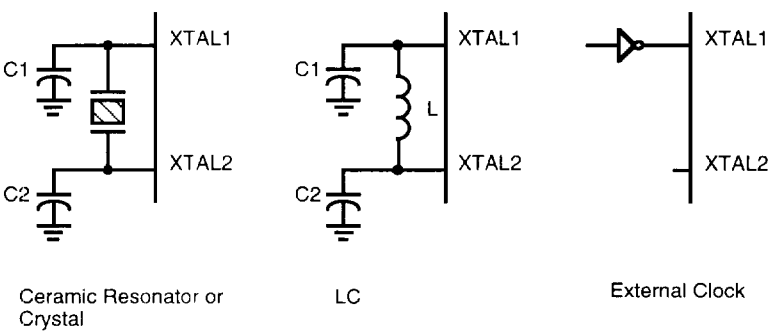

Figure 16. Oscillator Configuration

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 17).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 31. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

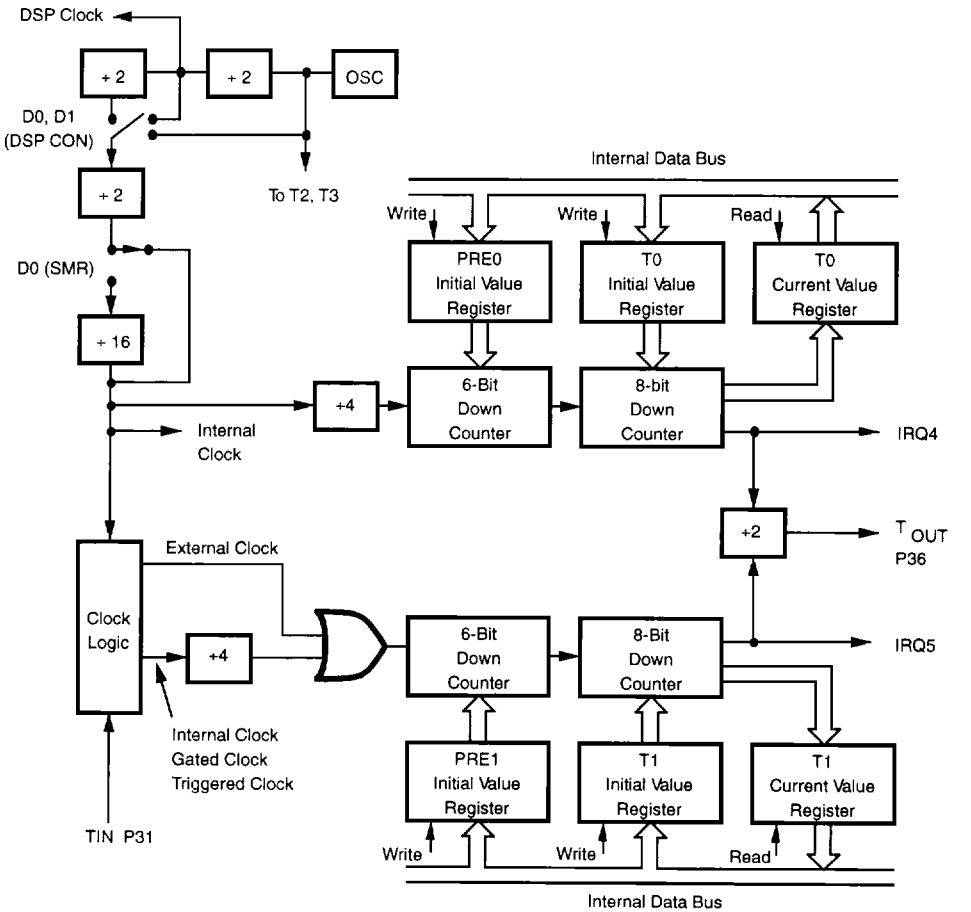

Figure 17. Counter/Timer Block Diagram

Z8 FUNCTIONAL DESCRIPTION (Continued)

Port Configuration Register (PCON). The PCON register configures each port individually; comparator output on Port 3, and open-drain on Port 0 and Port 1. The PCON register is located in the Expanded Register File at bank F, location 00H (Table 6).

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35, and a 0 releases the Port to its standard I/O configuration.

Port 0 Open-Drain (D1). Port 0 can be configured as an open-drain by resetting this bit (D1 = 0) or configured as push-pull active by setting this bit (D1 = 1). The default value is 1.

Port 1 Open-Drain (D2). Port 1 can be configured as an open-drain by resetting this bit (D2 = 0) or configured as push-pull active by setting this bit (D2 = 1). The default value is 1.

Table 6. Port Configuration Register (PCON) (F) 00H

Register PCON (F)%00	Position	Attrib.	Value	Description
	76543---			Reserved
	-----2--	R	0	Port 1 Open-drain
			1	Port 1 Push-pull Active*
	------1-	R	0	Port 0 Open-drain
			1	Port 0 Push-pull Active*
	-------0	R	0	P34, P35 Standard Output*
			1	P34, P35 Comparator Output

Note:
* Default setting after Reset

Port 4 and 5 Configuration Register (P45CON). The P45CON register configures Port 4 and Port 5, individually, to open-drain or push-pull active. This register is located in the Expanded Register File at Bank F, location 06H (Table 7).

Port 4 Open-Drain (D0). Port 4 can be configured as an open-drain by resetting this bit (D0 = 0) or configured as push-pull active by setting this bit (D0 = 1). The default value is 1.

Port 5 Open-Drain (D4). Port 5 can be configured as an open-drain by resetting this bit (D4 = 0) or configured as push-pull active by setting this bit (D4 = 1). The default value is 1.

Table 7. Port 4 and 5 Configuration Register (F) 06H [Write Only]

Register P45CON (F)%06	Position	Attrib.	Value	Description
	765-321-			Reserved
	---4----	W	0	Port 5 Open-drain
			1	Port 5 Push-pull Active*
	-------0	W	0	Port 4 Open-drain
			1	Port 4 Push-pull Active*

Note:
* Default setting after Reset

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status.
2. STOP-Mode Recovery (if D5 of SMR = 1).
3. WDT time-out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for external clock, RC/LC oscillators).

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation. It reduces the standby current to 10 µA (typical) or less. The STOP mode is terminated by a reset only, either by WDT time-out, POR, SMR recovery or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate Sleep instruction, i.e.;

```
FF  NOP    ; clear the pipeline
6F  STOP   ; enter STOP mode
           or
FF  NOP    ; clear the pipeline
7F  HALT   ; enter HALT mode
```

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Table 8). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a Low level or a High level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the STOP-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

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Table 8. Stop-Mode Recovery Register (SMR) (F) 0BH

Register SMR (F)%0B	Position	Attrib.	Value	Description
	7-------	R	0	POR*
			1	Stop Recovery
	-6------	W	0	Low Stop Recovery Level*
			1	High Stop Recovery Level
	--5-----	W	0	Stop Delay On*
			1	Stop Delay Off
	---432--	W		STOP-Mode Recovery Source
			000	POR Only*
			001	Reserved
			010	P31
			011	P32
			100	P33
			101	P27
			110	P2 NOR 0-3
			111	P2 NOR 0-7
	------1-			Reserved
	-------0	W	0	SCLK/TCLK Not Divide-by-16†
			1	SCLK/TCLK Divide-by-16

Notes:
* Default setting after Reset
† Reset after STOP-Mode Recovery

SCLK/TCLK divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 18 and Table 9).

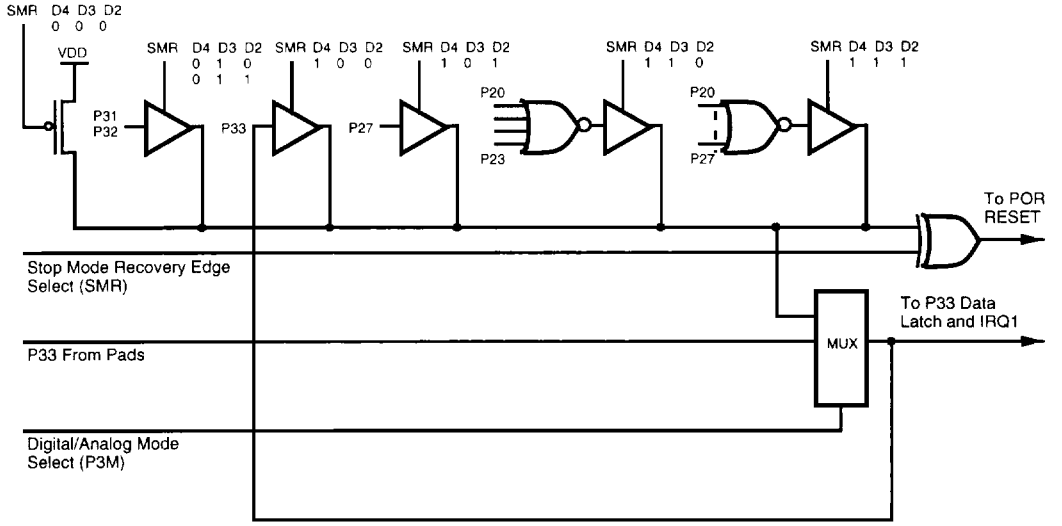

Figure 18. STOP-Mode Recovery Source

Table 9. STOP-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

STOP-Mode Recovery Delay Select (D5). This bit, if High, disables the 5 ms /RESET delay after STOP-Mode Recovery. The default configuration of this bit is one. If the "fast" wake up is selected, the Stop-Mode Recovery source is kept active for at least five TpC.

STOP-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z89121/921 from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR (Table 9).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. It is active High, and is 0 (cold) on POR/WDT /RESET. This bit is read only. It is used to distinguish between cold or warm start.

DSP Control Register (DSPCON). The DSPCON register controls various aspects of the Z8 and the DSP. It can configure the internal system clock (SCLK) or the Z8, RESET, and HALT of the DSP, and control the interrupt interface between the Z8 and the DSP (Table 10).

Z8 IRQ3 (D0). This bit, which causes the Z8 interrupt, can be set by the DSP by writing bit 9 of ICR. Z8 has to set this bit after serving the IRQ3 interrupt. The DSP can poll the status of IRQ3 by reading ICR bit 9.

DSP INT2 (D1). This bit is linked to DSP interrupt (INT2). It can be set by the Z8. After serving INT2, the DSP has to write a 1 to an appropriate bit in ICR (EXT4) to clear the IRQ. Reading this bit reflects the status of INT2 of the DSP.

Table 10. DSP Control Register
(F) 0CH [Read/Write]

Field DSPCON (F)0CH	Position	Attrib.	Value	Label
Z8_SCLK	76------	R/W	00	2.5 MHz (OSC/8)
			01	5 MHz (OSC/4)
			1x	10 MHz (OSC/2)
DSP_Reset	--5-----	R		Return '0'
		W	0	No effect
			1	Reset DSP
DSP_Run	---4----	R/W	0	Halt_DSP
			1	Run_DSP
Reserved	----32--		xx	
				Return '0'
				No effect
IntFeedback	------1-	R		FB_DSP_INT2
		W	1	Set DSP_INT2
			0	No effect
	-------0	R		FB_Z8_IRQ3
		W	1	Clear IRQ3
			0	No effect

DSP RUN (D4). This bit defines the HALT mode of the DSP. If this bit is set to 0, then the DSP clock is turned off to minimize power consumption. After this bit is set to 1, then the DSP will continue code execution from where it was halted. After a hardware reset, this bit is reset to 1.

DSP RESET (D5). Setting this bit to 1 will reset the DSP. If the DSP was in HALT mode, this bit is automatically preset to 1. Writing a 0 has no effect.

Z8 SLCK (D6-D7). These bits define the SCLK frequency of the Z8. The oscillator can be either divided-by-8, 4, or 2. After a reset, both of these are defaulted to 00.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Table 11). The WDT affects the Z (Zero), S (Sign), and V (Overflow) flags.

Table 11. Watch-Dog Timer Mode Register (F) 0F

Register WDTMR (F)%0F	Position	Attrib	Value	Description
	765-----			Reserved
	---4----	R/W	0	On-Board RC for WDT*
			1	XTAL for WDT
	----3---	R/W	0	WDT Off During STOP
			1	WDT On During STOP*
	-----2--	R/W	0	WDT Off During HALT
			1	WDT On During HALT*
	------10	R/W		Int RC Osc Ext. Clock
			00	5 ms 256 TpC
			01	15 ms 512 TpC*
			10	25 ms 1024 TpC
			11	100 ms 4096 TpC

Note:
* Default setting after Reset

Z8 FUNCTIONAL DESCRIPTION (Continued)

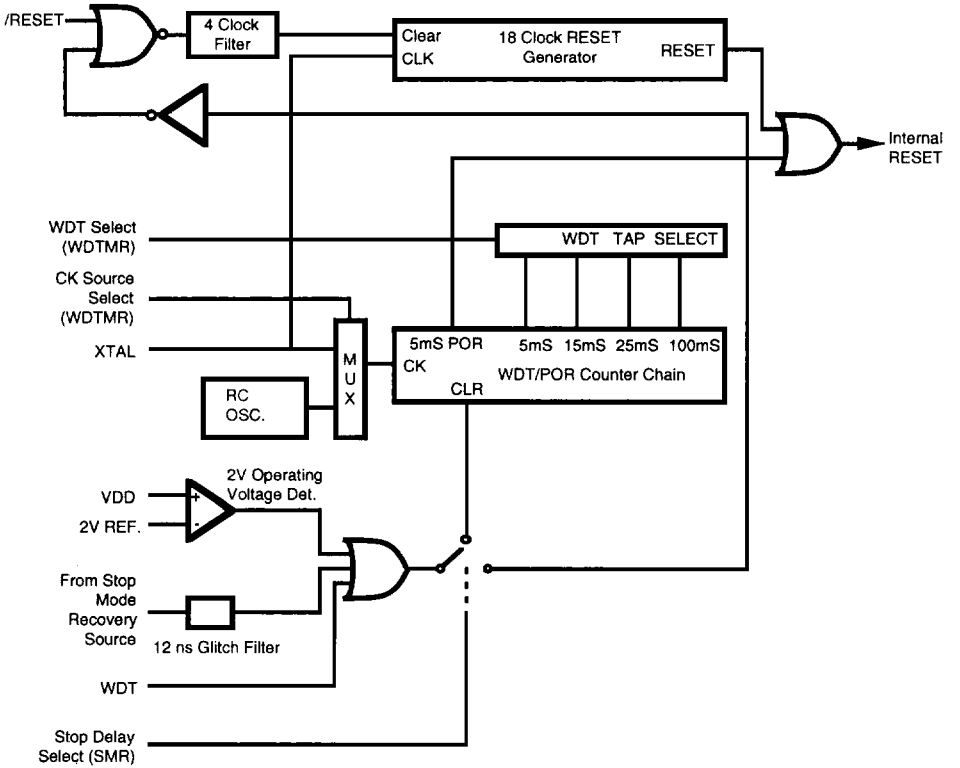

Figure 19. Resets and WDT

WDT Time Select (D0, D1). Selects the WDT time period. It is configured as shown in Table 12.

Table 12. WDT Time Select

D1	D0	Time-out of Internal RC OSC	Time-out of XTAL clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP mode, the on-board RC has to be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0 which selects the RC oscillator.

DSP FUNCTIONAL DESCRIPTION

The DSP coprocessor is characterized by an efficient hardware architecture that allows fast arithmetic operations such as multiplication, addition, subtraction and multiply accumulate of two 16-bit operands. Most instructions are executed in one clock cycle.

Four DSP registers (EXT3-EXT0) are shared through a quasi dual port mapping with the expanded register file of the Z8. Communication between the Z8 and the DSP occurs through these mailbox registers and interprocessor interrupt mechanism.

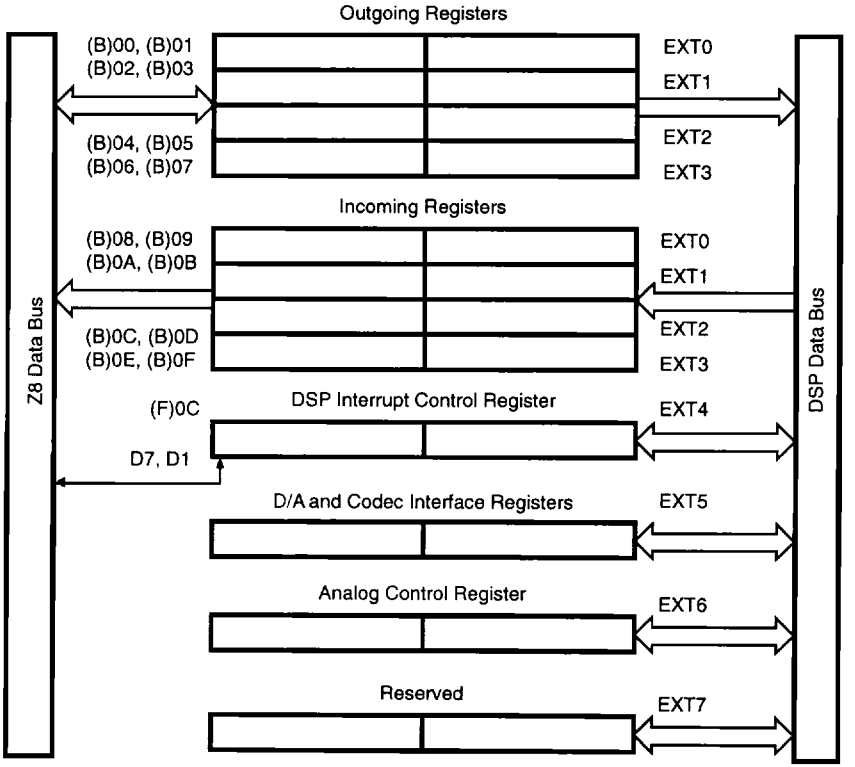

Figure 20. Z8-DSP Interface

DSP-Z8 Mail Box

To receive information from the DSP, the Z8 uses eight incoming registers which are mapped in the Z8 extended Register File (Bank B, 08 to 0F). The DSP treats these as four 16-bit registers that correspond to the eight incoming Z8 registers (Figure 20).

The Z8 can supply the DSP with data through eight outgoing registers mapped into both the Z8 Expanded Register File (Bank B, Registers 00 to 07) and the external register interface of the DSP. These registers are R/W and can be used as general purpose registers of the Z8. The DSP can only read information from these registers. Since the DSP uses a 16-bit data format and the Z8 an 8-bit data format, eight outgoing registers of the Z8 correspond to four DSP registers. The DSP can only read information from the outgoing registers.

Both the outgoing registers and the incoming registers share the same DSP address (EXT3-EXT0).

Note: The Z8 can read and write to ERF Bank B R00-R07, Registers 08-0F are read only from the Z8.

Table 13. Z8 Outgoing Registers (Read Only from DSP)

Field	Position	Attrib.	Value	Label
Outgoing [0] (B)00	76543210	R/W	%NN	(B)00/DSP_ext0_hi
Outgoing [1] (B)01	76543210	R/W	%NN	(B)01/DSP_ext0_lo
Outgoing [2] (B)02	76543210	R/W	%NN	(B)02/DSP_ext1_hi
Outgoing [3] (B)03	76543210	R/W	%NN	(B)03/DSP_ext1_lo
Outgoing [4] (B)04	76543210	R/W	%NN	(B)04/DSP_ext2_hi
Outgoing [5] (B)05	76543210	R/W	%NN	(B)05/DSP_ext2_lo
Outgoing [6] (B)06	76543210	R/W	%NN	(B)06/DSP_ext3_hi
Outgoing [7] (B)07	76543210	R/W	%NN	(B)07/DSP_ext3_lo

Table 14. Z8 Incoming Registers (Write Only from DSP)

Field	Position	Attrib.	Value	Label
Incoming [8] (B)08	76543210	R	%NN	DSP_ext0_hi
		W		No Effect
Incoming [9] (B)09	76543210	R	%NN	DSP_ext0_lo
		W		No Effect
Incoming [a] (B)0A	76543210	R	%NN	DSP_ext1_hi
		W		No Effect
Incoming [b] (B)0B	76543210	R	%NN	DSP_ext1_lo
		W		No Effect
Incoming [c] (B)0C	76543210	R	%NN	DSP_ext2_hi
		W		No Effect
Incoming [d] (B)0D	76543210	R	%NN	DSP_ext2_lo
		W		No Effect
Incoming [e] (B)0E	76543210	R	%NN	DSP_ext3_hi
		W		No Effect
Incoming [f] (B)0F	76543210	R	%NN	DSP_ext3_lo
		W		No Effect

Table 15. DSP Incoming Registers

Field	Position	Attrib.	Value	Label
DSP_ext0	fedcba9876543210	R	%NNNN	(B)00, (B)01
Mail Box		W		(B)08, (B)09
DSP_ext1	fedcba9876543210	R	%NNNN	(B)02, (B)03
Mail Box		W		(B)0A, (B)0B
DSP_ext2	fedcba9876543210	R	%NNNN	(B)04, (B)05
Mail Box		W		(B)0C, (B)0D
DSP_ext3	fedcba9876543210	R	%NNNN	(B)06, (B)07
Mail Box		W		(B)0E, (B)0F

DSP Interrupts

The DSP processor has three interrupt sources (INT2, INT1, INT0) (Figure 21). These sources have different priority levels (Figure 22). The highest priority, the next lower and the lowest priority level are assigned to INT2, INT1 and INT0, respectively. The DSP does not allow interrupt nesting (interrupting service routines that are currently being executed). When two interrupt requests occur simultaneously the DSP starts servicing the interrupt with the highest priority level.

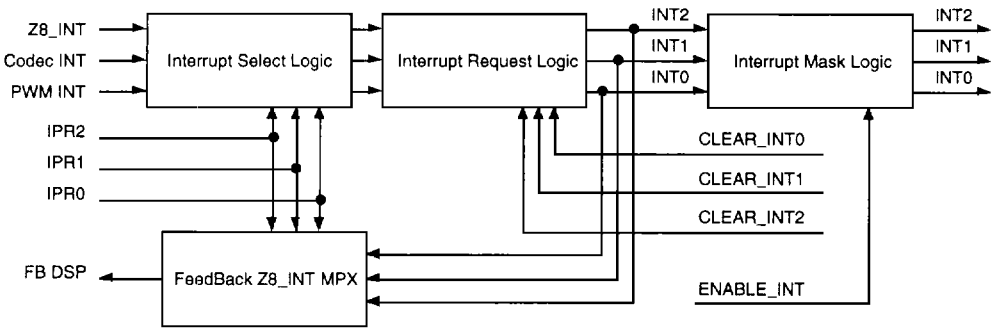

Figure 21. DSP Interrupts

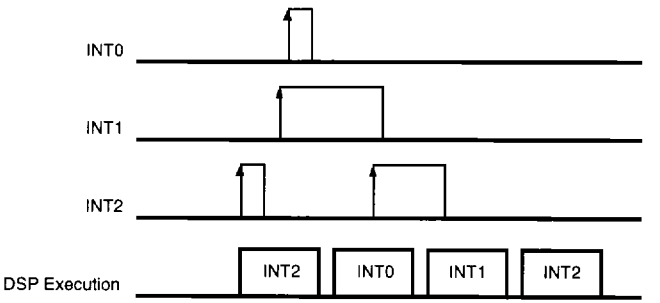

Figure 22. DSP Interrupt Priority Structure

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DSP Interrupts (Continued)

Table 16. EXT4 DSP Interrupt Control Register (ICR) Definition

Field	Position	Attrib	Value	Label
DSP_INT2	f---------------	R	1	INT2_is set
			0	INT2_is reset
	f---------------	W	1	Clear_DSP_INT2
			0	Has_no_effect
DSP_INT1	-e--------------	R	1	INT1_is set
			0	INT1_is reset
	-e--------------	W	1	Clear_DSP_INT1
			0	Has_no_effect
DSP_INT0	--d-------------	R	1	INT0_is set
			0	INT0_is reset
	--d-------------	W	1	Clear_DSP_INT0
			0	Has_no_effect
DSP_MaskINT2	---c------------	R/W	1	Enable_INT2
			0	Disable_INT2
DSP_MaskINT1	----b-----------	R/W	1	Enable_INT1
			0	Disable_INT1
DSP_MaskINT0	-----a----------	R/W	1	Enable_INT0
			0	Disable_INT0
Z8_IRQ3	------9---------	R	1	IRQ3_active
			0	IRQ3_inactive
	------9---------	W	1	Set_Z8_IRQ3
			0	Has_no_effect
Enable_INT	-------8--------	R/W	1	Enable_INT
			0	Disable_INT
DSP_INTSel2	--------7-------	R/W	Binary	INTSel2
DSP_INTSel1	---------6------	R/W	Binary	INTSel1
DSP_INTSel0	----------5-----	R/W	Binary	INTSel0
Reserved	----------43210		xxxxx	Reserved

Interrupt Control Register (ICR). The ICR is mapped into EXT4 of the DSP (Table 16). The bits are defined as follows.

DSP_IRQ2 (Z8 Interrupt). This bit can be read by both Z8 and DSP and can be set only by writing to the Z8 expanded Register File (Bank F, ROC, bit 0). This bit asserts IRQ2 of the DSP and can be cleared by writing to the Clear_IRQ2 bit.

DSP_IRQ1 (A/D Interrupt). This bit can be read by the DSP only and is set when valid data is present at the A/D output register (conversion done). This bit asserts IRQ1 of the DSP and can be cleared by writing to the Clear_IRQ1bit.

DSP_IRQ0 (D/A Interrupt). This bit can be read by DSP only and is set by Timer3. This bit assists IRQ0 of the DSP and can be cleared by writing to the Clear_IRQ0 bit.

DSP_MaskIntX. These bits can be accessed by the DSP only. Writing a 1 to these locations allows the INT to be serviced, while writing a 0 masks the corresponding INT off.

Z8_IRQ3. This bit can be read from both Z8 and DSP and can be set by DSP only. Addressing this location accesses bit D3 of the Z8 IRQ register; hence, this bit is not implemented in the ICR. During the interrupt service routine executed on the Z8 side, the User has to reset the Z8_IRQ3 bit by writing a 1 to bit D0 of the DSPCON. Three Z8 instructions after this operation, the hardware of the Z89121/921 automatically resets Z8_IRQ3. This delay provides the timing synchronization between the Z8 and the DSP sides during interrupts. In summary, the interrupt service routine of the Z8 for IRQ3 should be finished by:

```
PUSH  RP
LD    RP,#%0F
OR    r12,#%01
POP   RP
IRET
```

DSP Enable_INT. Writing a 1 to this location enables global interrupts of the DSP while writing 0 disables them. A system Reset globally disables all interrupts.

DSP_IPRX. This 3-bit group defines the Interrupt Select logic according to Table 17.

Clear_IRQX. These bits can be accessed by the DSP only. Writing a 1 to these locations rests the corresponding DSP_IRQX bits to 0. Clear_IRQX are virtual bits and are not implemented.

Table 17. DSP Interrupt Selection

DSP_IPR[2-0] 2 1 0	Z8_INT is Switched to	Codec_INT is Switched to	D/A_INT is Switched to
0 0 0	INT2	INT1	INT0
0 0 1	INT1	INT2	INT0
0 1 0	INT2	INT0	INT1
0 1 1	INT1	INT0	INT2
1 0 0	INT0	INT2	INT1
1 0 1	INT0	INT1	INT2
1 1 0	Reserved	Reserved	Reserved
1 1 1	Reserved	Reserved	Reserved

6

PULSE WIDTH MODULATOR (PWM)

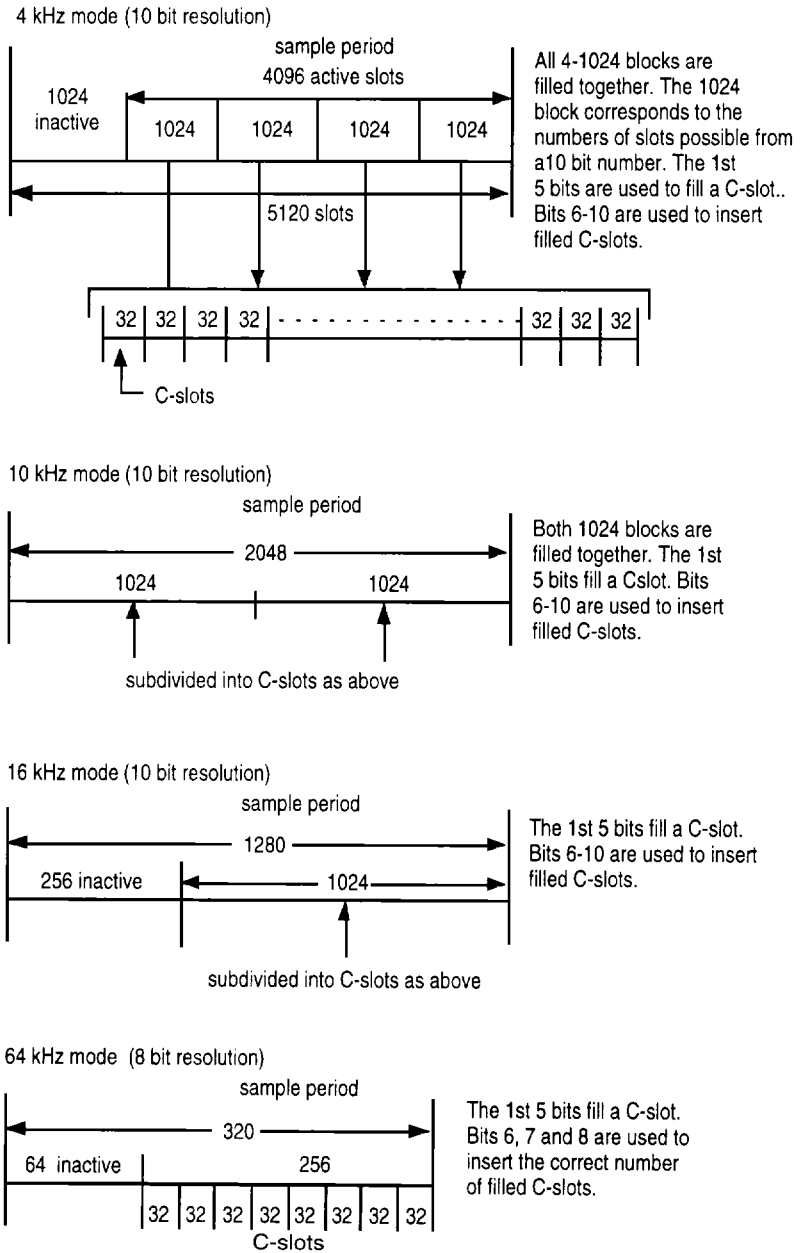

Figure 23. PWM Output

CODEC INTERFACE

Codec interface provides the user all the necessary signals to connect two independent codec chips. The supported sampling rate is 8K samples/sec. at a data rate of 2.048 MHz, or 6.66K samples/sec. at a 1.7066 MHz data rate. Figure 24 shows the connection of T2 (TCM29C18) and Motorola (MC145503) Codec to Z89121. The timing diagram is shown in Figure 25.

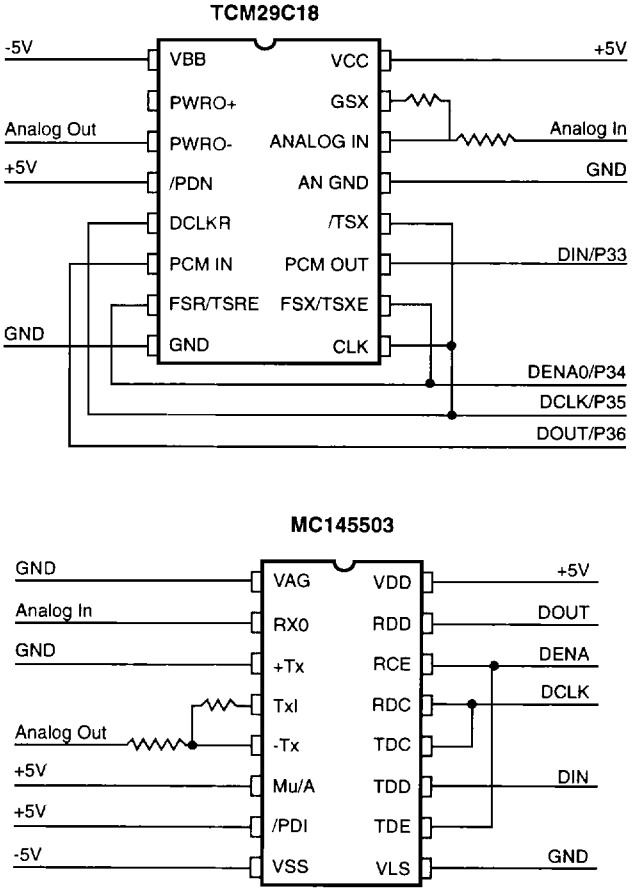

Figure 24. Connecting TCM29C18 and MC145503 to Z89121/921

CODEC INTERFACE (Continued)

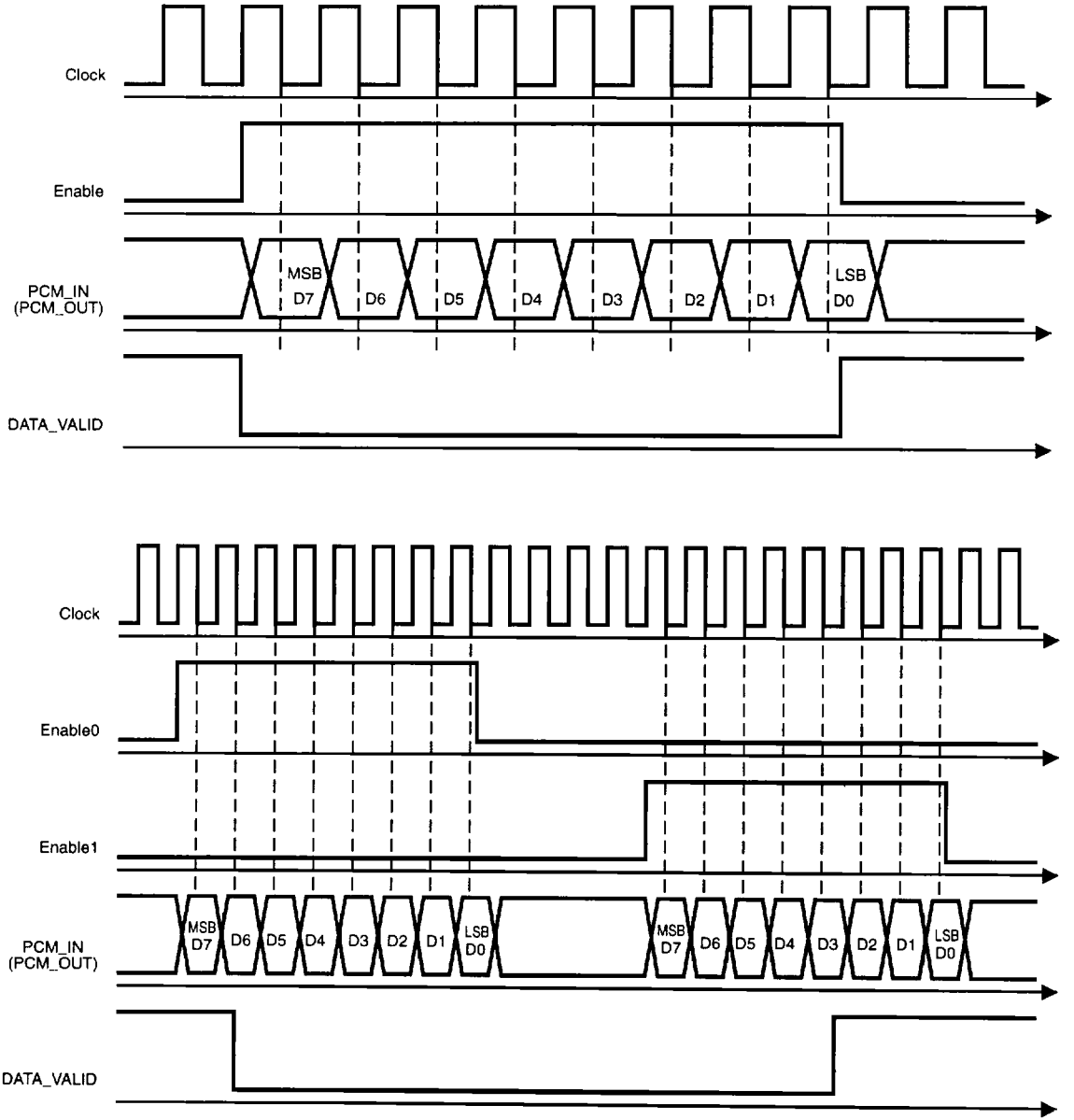

Figure 25. Timing Diagram of Codec Interface

D/A (PWM) Converter/Codec interface Register - EXT5

External DSP register EXT5 is used by the D/A converter and an External Codec Interface. The accessibility of all these devices is driven by the Analog Control register (EXT6).

The D/A converter (10-bit PWM) will be loaded by writing to register EXT5 of the DSP.

Two different Codecs can be addressed by the Analog Control register (EXT6). The data loaded to Codec0 and Codec1 is defined by writing to the EXT5 register of the DSP, while reading from this register gives the data received from Codecs.

Because the same logical register (EXT5) can be either the source or the destination for several physical devices (D/A and Codecs), the user must specify which one of all available devices is desirable to write (read) to (from). EXT5 bits 'e' and 'f' are used to distinguish between different devices upon writing data to D/A, Codec0 and Codec1, as shown below. Upon reading from EXT5, the DSP reads in sequence all active (enabled) devices according to the definition of the Select_Sequence field (bits 'c' and 'd') in ACR (EXT6). The sequence of reading data can be reset by writing a 1 to the Reset_Toggle field of EXT6.

Register EXT5 is accessible to the DSP only.

Digital to Analog Converter - EXT5 (when written)

The D/A conversion is DSP driven by sending 10-bit data to the external register EXT5 of the DSP. The six remaining bits of EXT5 are reserved, as shown in the following table.

Data will be loaded into the D/A latch during the clock cycle following the (ld EXT5,data) instruction.

Table 18. EXT5 (when written)

Field	Position	Attrib.	Value	Label
Data	f----------	W	0	Should be '0'
	-edcba----------			Reserved
	------98765-----	W	%NN	Data To PWM (High Val)
	----------43210	W	%NN	Data To PWM (Low Val)

Codec Interface Controller - EXT5 (when written)

The two Data registers of the External Codec interface are mapped into the external register EXT5 of the DSP. The eight remaining bits of EXT5 are reserved as shown in the Table 19. Data will be loaded into the corresponding Data register (defined by field 'e') during the clock cycle following the (ld EXT5,data) instruction.

Table 19. EXT5 (when written)

Field	Position	Attrib.	Value	Label
Data	f----------		1	Should be '1'
	-e----------		0	Codec0
			1	Codec1
	--dcba98--------			Reserved
	--------76543210		%NN	DataToCodec

Codec Interface Controller - EXT5 (when read)

8-Bit Data can be read from the Codec by the DSP through the external register, EXT5. Of the 16 bits of the EXT5, only eight bits, 0 through 7, return Data; the remaining bits are padded with zeroes.

Table 20. EXT5 (when read)

Field	Position	Attrib.	Value	Label
Data	fedcba98--------			Return '0'
	--------76543210		%NN	DataFromCodec

Analog Control Register (ACR)

The Analog Control register is mapped to register EXT6 of the DSP (Table 21). This read/write register is accessible by the DSP only.

The 16-bit field of EXT6 defines modes of both the A/D and the D/A. The High Byte configures the Codec.

Table 21. EXT6 Analog Control Register (ACR)

Field	Position	Attrib.	Value	Label
MPX_DSP_INT0	f------- --------	R/W	1	P26
			0	Timer3
Reset_Toggle	-e------ --------	R		Return '0'
	-e------ --------	W	1	Reset Toggle
			0	No Effect
Select_Sequence	--dc--- --------	R/W	XX	Selects Codec0/Codec1 upon Reading EXT5
Reserved	----b--- --------	R		Return '0'
		W		No Effect
D/A_SamplingRate	-----a98--------	R/W	11x	Reserved
			101	Reserved
			100	64 kHz
			010	16 kHz
			011	10 kHz
			001	4 kHz
			000	Reserved
Div10/12	-------- 7-------	R/W	1	Divided-by-10
			0	Divided-by-12
Reserved	-------- -6------	R/W		Should Be Set to '0'
Reserved	-------- --543210	R	%DD	Return '0'
		W		No Effect

DSP IRQ0. Defines the source of DSP IRQ0 interrupt.

Select_Sequence. Defines the Codec0 and Codec1 enabling/disabling and the sequence of reading data from these devices starting from the reset condition (Table 22).

A 1 should be written to bit 'e' in order to reset the sequence. Writing 1 to bit e ensures the next data read from EXT5 is the data of Codec0.

Table 22. Select_Sequence

Select Sequence d	Select Sequence c	Codec Enabled/Disabled Codec0	Codec Enabled/Disabled Codec1	Sequence of Access First	Sequence of Access Second
0	0	Disable	Disable	N/A	
0	1	Enable	Disable	Codec0	N/A
1	0	Enable	Enable	Codec0	Codec1
1	1	Disable	Disable	Reserved	Reserved

Div 10/12. This bit defines the speed of the Codecs. If the bit is set to 1, the Codec clock frequency is set to 2.048 MHz, and the sampling rate is 8 kHz. If the bit is reset to 0, Codec clock frequency is set to 1.7066 MHz and the sampling rate to 6.66 kHz.

Note: Bit 6 of ACR should be set to zero.

D/A_Sampling Rate. This field defines the sampling rate of the D/A output. It changes the period to Timer3 interrupt and the maximum possible accuracy of the D/A (Table 23).

Table 23. D/A Data Accuracy

D/A_Sampling Rate	Sampling Rate	D/A Accuracy
1 0 0	64 kHz	8 Bits
0 1 0	16 kHz	10 Bits
0 1 1	10 kHz	10 Bits
0 0 1	4 kHz	10 Bits

DSP Timers

Timer2 is a free-running counter that divides the XTAL frequency (20.48 MHz) to support different sampling rates for the A/D converter. The sampling rate is defined by the Analog Control Register. Upon reaching the end of a count, the timer generates an interrupt request to the DSP.

Analogous to Timer2, Timer3 generates the different sampling rates for the D/A converter. Timer3 also generates an interrupt request to the DSP upon reaching its final count value (Figure 26).

Note: The crystal speed in this example is 20.48 MHz, which is the maximum tested speed, but other lower speeds may be used.

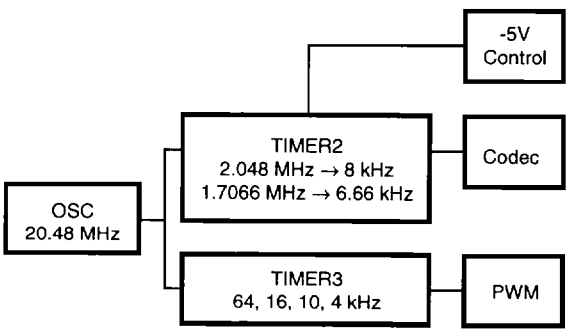

Figure 26. Timer2 and Timer3

Minus 5V DC Generation

Some Codecs require a ±5V power supply. The Z89121/921 provides a $-5V_{OUT}$ output to drive an external pump circuit. A complete circuit diagram for the –5V generation is shown in Figure 27. The reference voltage of 2.5V is generated by a resistor divider R5, R6 on the P33 input of Z86C67/921. This voltage is compared with the voltage of the voltage divider formed by R2, R4. If the latter voltage rises above the reference voltage, the comparator (inside Z86C67/921) will be switched and connect the internal 128 kHz output of Timer2 to the $-5V_{OUT}$ output pin of Z89121/921. On the contrary, the $-5V_{OUT}$ will be switched off if the voltage from voltage divider R2, R4 drops below the reference voltage. This regulates the voltage across C1 to be –5V.

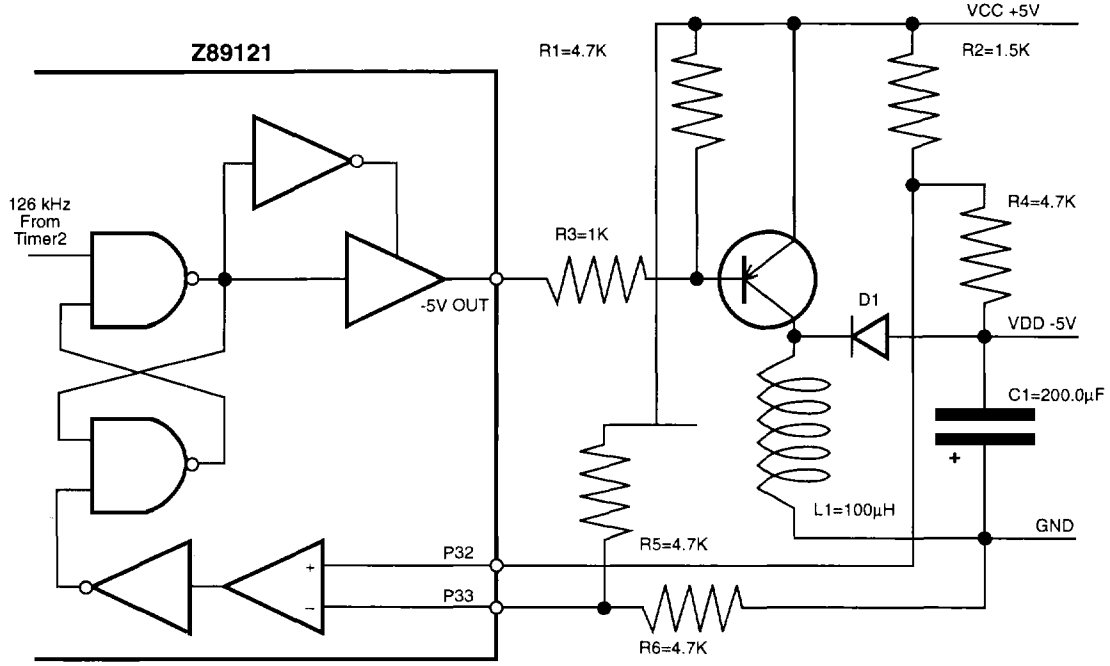

Figure 27. Circuit Diagram for –5V Generation

DRAM INTERFACE

The DRAM interface controller accepts a wide variety of external DRAM configurations (up to 48 Mbits) with 4-bit wide data buses. It can be reconfigured from the software to support: 1 Mbit x 1, 4 Mbit x 1, 1 Mbit x 4, 4 Mbit x 4 DRAM. DRAM interface registers are mapped to expanded register file (bank0A).

Table 24. Registers of DRAM Interface

Field	Position	Attrib.	Value	Label
Data (Register (A)00)	76543210	R/W	%FF	Data
Control (Register (A)01)	76543210	R/W	%FF	See Text
Most Significant Byte (Register (A)02)	76543210	R/W	%FF	Data
Middle Significant Byte (Register (A)03)	76543210	R/W	%FF	Data
Least Significant Byte (Register (A)04)	76543210	R/W	%FF	Data
Refresh Count (Register (A)05)	76543210	R/W	%FF	Data

Data Register. This register is used as a logical device for reading (writing) data from (to) the DRAM. After reading by the Z8 in Auto Increment mode, the logical DRAM address specified by register (AH)04H is increased by 1 and new DRAM data at this address will be read and stored into the data register. When data is written to this register, it will be stored into the last valid DRAM logical address. The hardware write-data-to-DRAM cycle is implemented as an early write cycle with Twcs > 40 ns. The user has to load a 23-bit address into the Least, Middle, and Most Significant Byte Registers and then write the 8-bit data to the Data Register. The data will be automatically separated into higher nibble and lower nibble and stored into two subsequent locations in the DRAM (2*Address for higher nibble and 2*Address+1 for lower nibble). Writing data to the Data Register with the Auto-incremental Bit (bit 0) of the DRAM Control Register equal to 0 increases the address in the Least Significant DRAM register (AH)04H by 1.

Most, Middle, and Least Significant Byte Registers. The 23-bit logical address of DRAM is stored in these three registers. Upon writing to these registers, the read cycle from DRAM is executed so that the new data is available in the data register.

Refresh Count Register. The /RAS-only refresh cycle is transparent to the user and is supported by hardware logic. This register specifies how many rows of memory matrix, starting from the beginning of the DRAM (logical address 000000H), should be refreshed. The number of the rows in DRAM to be refreshed is defined by the value in Refresh Count Register plus one and then multiplied by eight.

The basic timing diagram of the DRAM interface is shown in Figure 28.

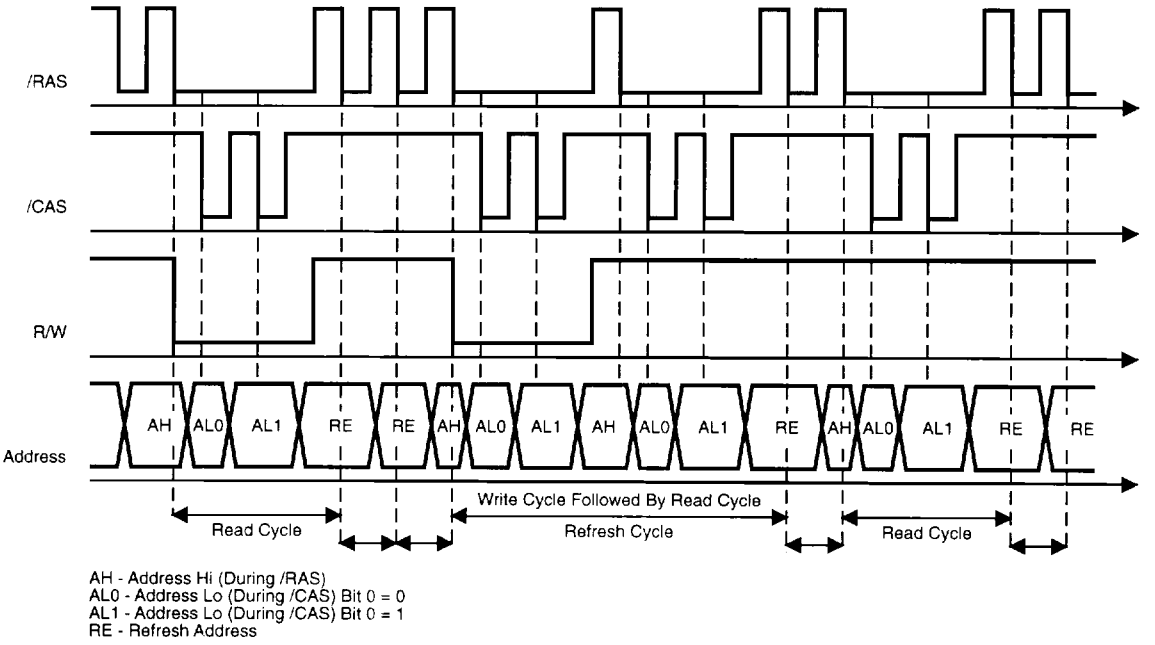

Figure 28. Timing Diagram for DRAM Interface

DRAM Control Register

The register defines DRAM access time, DRAM memory size, refresh operation, etc. (Figure 29). After Power-On Reset, the DRAM Control Register is set to %00, which defines 1 Mbit DRAM configuration with permanently active DRAM refreshing.

Table 25. DRAM Control Register

Register	Position	Attrib.	Value	Description
Access_Time	7-------	R/W	0	400 ns
			1	200 ns
ARAM_size	-6------	R/W	0	1 Mbit
			1	4 Mbit
Reserved	--54----	R/W	%DD	number
				These two bits can be used as User defined flags.
Refresh_start	----32--	R/W	00	Permanently
			01	Upon T0
			10	Upon T0
			11	Refresh off
Refresh_clear	------1-	R		Return '0'
		W	1	Refresh clear
			0	No effect
Autoincrement	-------0	R/W	0	Increment ON
			1	Increment OFF

Access_time. This bit defines the speed of DRAM Controller. The read/write cycle width can be changed to support slower DRAMs. When set to 1, the width of /CAS signal is set to 200 ns. Reset the Access_time bit to 0 set the width of /CAS signal to 400 ns.

DRAM_size. DRAM interface supports four different sizes of ARAM: 1 Mbit x 1, 1 Mbit x 4, 4 Mbit x 1 and 4 Mbit x 4. These require either 11- or 10-bit address bus. For 1 Mbit x 1 or 1 Mbit x 4 DRAM, the ADDR10 is used to generate select (/CAS) signal.

Bit 6	/CAS	ARAM_SEL1	ARAM_SEL0	Addr10
0	1st /CAS	3rd /CAS	2nd /CAS	Addr10
1	1st /CAS	3rd /CAS	2nd /CAS	4th /CAS

Auto Increment. This bit specifies the Auto Increment of the LBS byte of the DRAM address. The Auto Increment function does not affect any flag of Z8.

6

DRAM Interface

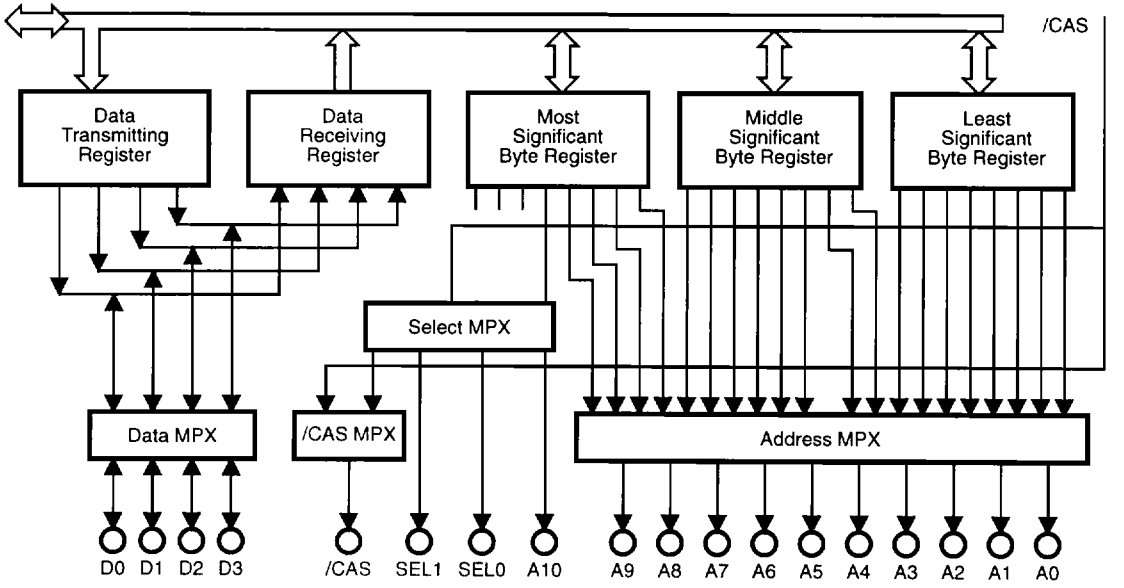

Figure 29. Block Diagram of the DRAM Interface

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min.	Max.	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp		†	C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 30).

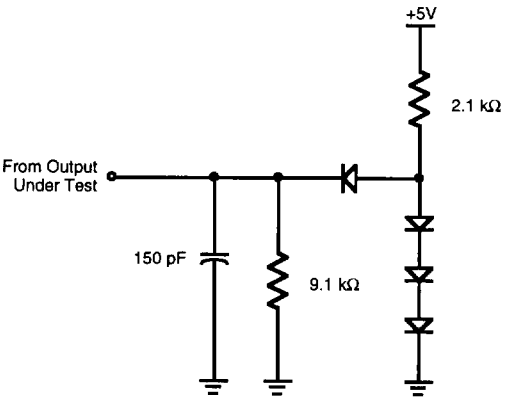

Figure 30. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} Note [1]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units
I_{CC}	Supply Current	5.0V		65	40	mA
I_{CC1}	HALT Mode Current	5.0V		10	6	mA
I_{CC2}	STOP Mode Current	5.0V		20	6	µA
I_{-5V}	Output Current, –5V Supply		–15		–20	mA

Note:
[1] 5.0V ±0.5V

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C Min	Max	T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage	3.3V		7		7		V	I_{IN} 250 uA
		5.0V		7		7		V	I_{IN} 250 uA
V_{CH}	Clock Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.3V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator
		5.0V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V	
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	
V_{IL}	Input Low Voltage	3.3V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	0.7	V	
		5.0V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.5	V	
V_{OH}	Output High Voltage	3.3V	V_{CC} –0.4		V_{CC} –0.4		3.1	V	I_{OH} = –2.0 mA
		5.0V	V_{CC} –0.4		V_{CC} –0.4		4.8	V	I_{OH} = –2.0 mA
V_{OL1}	Output Low Voltage	3.3V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA
		5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA
V_{OL2}	Output Low Voltage	3.3V		1.2		1.2	0.3	V	I_{OL} = +6 mA, 3 Pin Max
		5.0V		1.2		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max
V_{RH}	Reset Input High Voltage	3.3V	0.8 V_{CC}	V_{CC}	0.8 V_{CC}	V_{CC}	1.5	V	
		5.0V	0.8 V_{CC}	V_{CC}	0.8 V_{CC}	V_{CC}	2.1	V	
V_{RI}	Reset Input Low Voltage	3.3V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.1		
		5.0V	GND–0.3	0.2 V_{CC}	GND–0.3	0.2 V_{CC}	1.7		
V_{OFFSET}	Comparator Input Offset	3.3V		25		25	10	mV	
	Voltage	5.0V		25		25	10	mV	
I_{IL}	Input Leakage	3.3V	-1	1	–1	2	<1	µA	V_{IN} = 0V, V_{CC}
		5.0V	-1	1	–1	2	<1	µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	3.3V	-1	1	–1	2	<1	µA	V_{IN} = 0V, V_{CC}
		5.0V	-1	1	–1	2	<1	µA	V_{IN} = 0V, V_{CC}
I_{IR}	Reset Input Current	3.3V		–45		–60	–20	µA	
		5.0V		–55		–70	–30	µA	

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

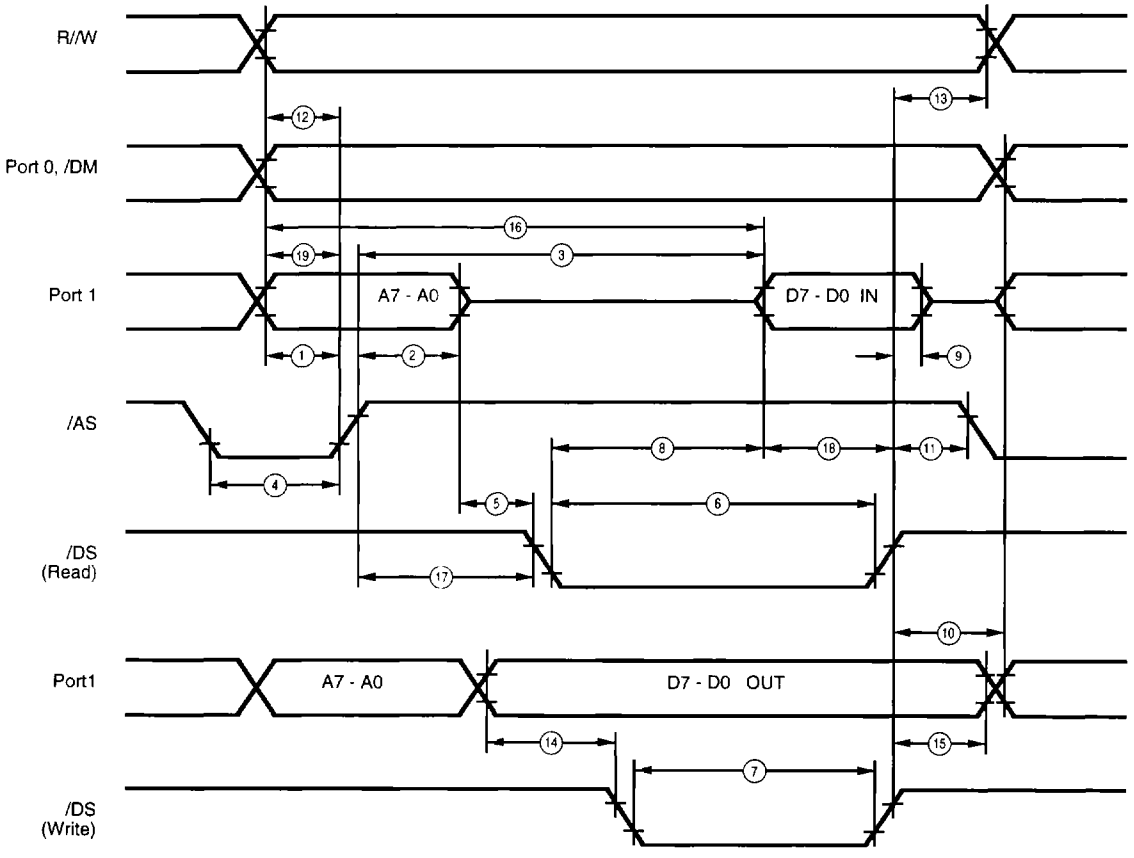

Figure 31. External I/O or Memory Read/Write Timing

6

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

No	Symbol	Parameter	V_{CC} Note [4]	T_A = 0°C to +70°C Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	5.0	20		ns	[2, 3]
2	TdAS(A)	/AS Rise to Address Float Delay	5.0	25		ns	[2, 3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	5.0		150	ns	[1, 2, 3]
4	TwAS	/AS Low Width	5.0	30		ns	[2, 3]
5	TdAZ(DS)	Address Float to /DS Fall	5.0	0		ns	
6	TwDSR	/DS (Read) Low Width	5.0	105		ns	[1, 2, 3]
7	TwDSW	/DS (Write) Low Width	5.0	65		ns	[1, 2, 3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	5.0		55	ns	[1, 2, 3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	5.0	0		ns	[2, 3]
10	TdDS(A)	/DS Rise to Address Active Delay	5.0	40		ns	[2, 3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	5.0	25		ns	[2, 3]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	5.0	20		ns	[2, 3]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	5.0	25		ns	[2, 3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	5.0	20		ns	[2, 3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	5.0	25		ns	[2, 3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0		180	ns	[1, 2, 3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	5.0	35		ns	[2, 3]
18	TdDI(DS)	Data Input Setup to /DS Rise	5.0	50		ns	[1, 2, 3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	5.0	20		ns	[2, 3]

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] See clock cycle dependent characteristics table.
[4] 5.0V ±0.5V

Standard Test Load
All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Diagram

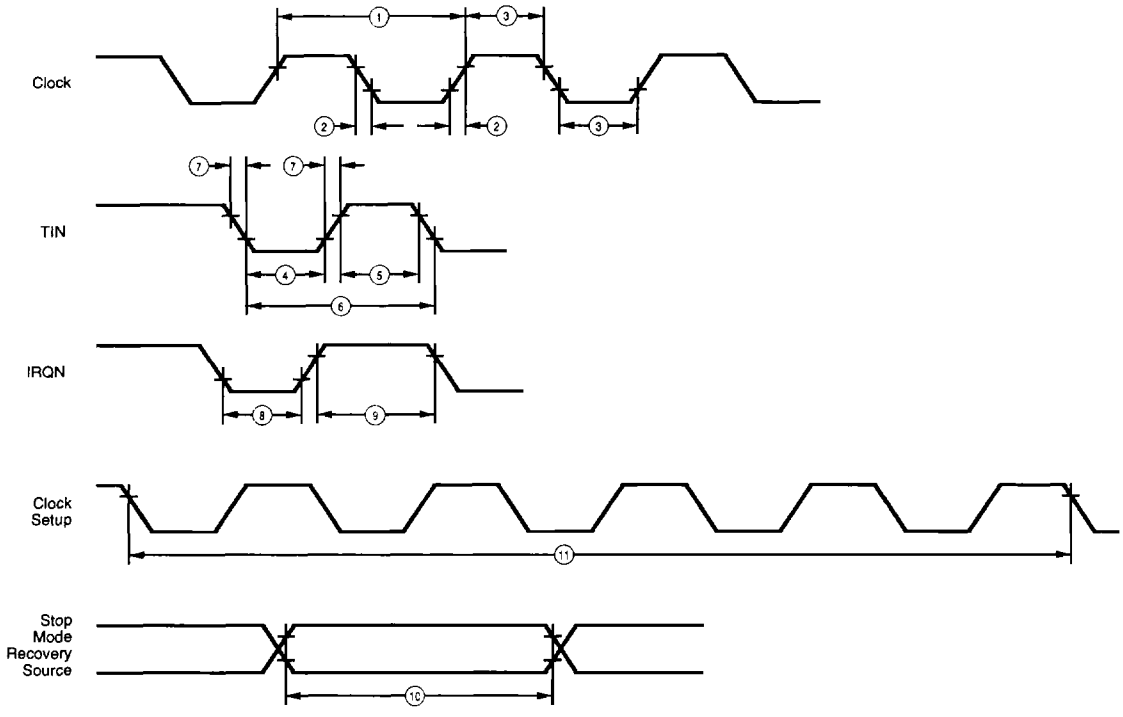

Figure 32. Additional Timing

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table

No	Symbol	Parameter	V_{CC} Note [5]	T_A = 0°C to +70°C Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0V	48.83		ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		6	ns	[1]
3	TwC	Input Clock Width	5.0V	16		ns	[1]
4	TwTinL	Timer Input Low Width	5.0V	70		ns	
5	TwTinH	Timer Input High Width	5.0V	3TpC			[1]
6	TpTin	Timer Input Period	5.0V	8TpC			[1]
7	TrTin, TfTin	Timer Input Rise & Fall Timer	5.0V		100	ns	[1]
8A	TwIL	Int. Request Low Time	5.0V	70		ns	[1, 2]
8B	TwIL	Int. Request Low Time	5.0V	3TpC			[1]
9	TwIH	Int. Request Input High Time	5.0V	3TpC			[1]
10	Twsm	STOP-Mode Recovery Width Spec	5.0V	12 5TpC		ns	[1]
11	Tost	Oscillator Startup Time	5.0V	5TpC			[3]
12	Twdt	Watch-Dog Timer	5.0V	5		ms	D1 = 0, D0 = 0 [4]
			5.0V	15		ms	D1 = 0, D0 = 1 [4]
			5.0V	25		ms	D1 = 1, D0 = 0 [4]
			5.0V	100		ms	D1 = 1, D0 = 1 [4]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] SMR-D5 = 0.
[4] Reg. WDT.
[5] 5.0V ±0.5V

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams

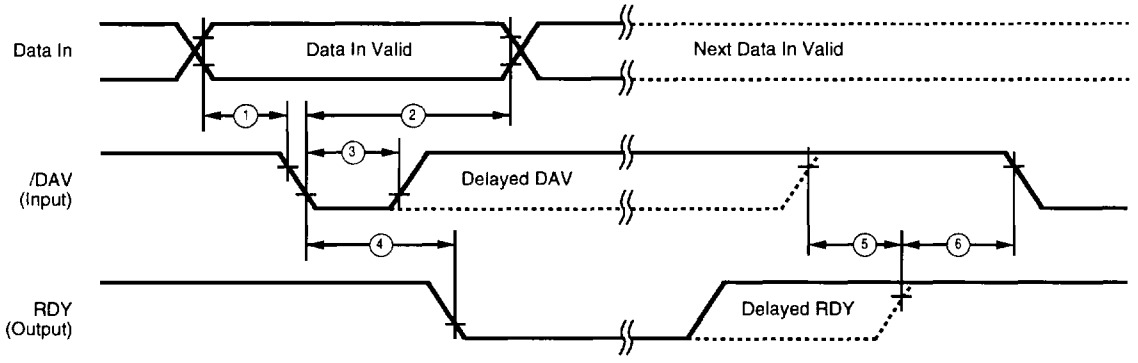

Figure 33. Input Handshake Timing

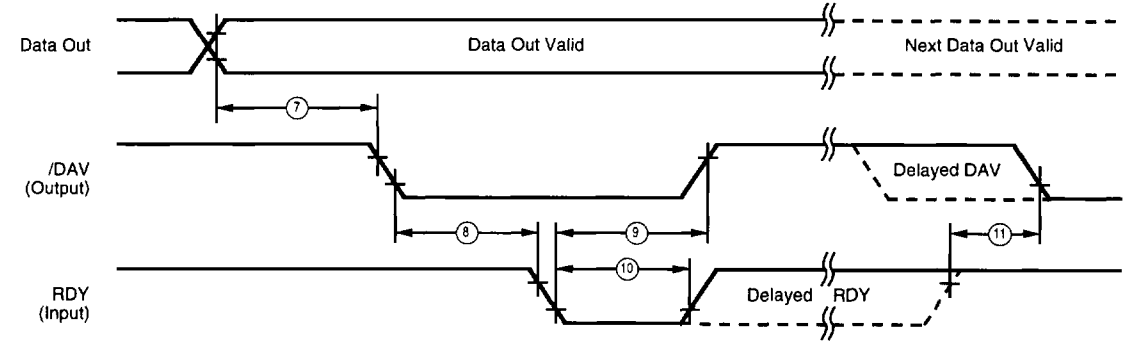

Figure 34. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note [1]	T_A = 0°C to +70°C Min	Max	Units	Data Direction
1	TsDI(DAV)	Data In Setup Time	5.0 V	0		ns	IN
2	ThDI(DAV)	Data In Hold Time	5.0 V	115		ns	IN
3	TwDAV	Data Available Width	5.0 V	110		ns	IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0 V		115	ns	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0 V		80	ns	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	5.0 V	0		ns	IN
7	TcLDAV0(RDY)	Data Out to DAV Fall Delay	5.0 V	25		ns	OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0 V	0		ns	OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0 V		115	ns	OUT
10	TwRDY	RDY Width	5.0 V	80		ns	OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0 V		80	ns	OUT

Note:
[1] 5.0V ±0.5V

Z8 EXPANDED REGISTER FILE REGISTERS

Expanded Register Bank B

Register	Position	Attrib.	Value	Description
Outgoing Reg. to DSP EXT0 (High Byte) (B)%00	76543210	R/W		DSP EXT0, Bits D15-D8
Outgoing Reg. to DSP EXT0 (Low Byte) (B)%01	76543210	R/W		DSP EXT0, Bits D7-D0
Outgoing Reg. to DSP EXT1 (High Byte) (B)%02	76543210	R/W		DSP EXT1, Bits D15-D8
Outgoing Reg. to DSP EXT1 (Low Byte) (B)%03	76543210	R/W		DSP EXT1, Bits D7-D0
Outgoing Reg. to DSP EXT2 (High Byte) (B)%04	76543210	R/W		DSP EXT2, Bits D15-D8
Outgoing Reg. to DSP EXT2 (Low Byte) (B)%05	76543210	R/W		DSP EXT2, Bits D7-D0
Outgoing Reg. to DSP EXT3 (High Byte) (B)%06	76543210	R/W		DSP EXT3, Bits D15-D8
Outgoing Reg. to DSP EXT3 (Low Byte) (B)%07	76543210	R/W		DSP EXT3, Bits D7-D0

Z8 EXPANDED REGISTER FILE REGISTERS

Expanded Register Bank B (Continued)

Register	Position	Attrib.	Value	Description
Incoming Reg. to DSP EXT0 (High Byte) (B)%08	76543210	R		DSP EXT0, Bits D15-D8
Incoming Reg. to DSP EXT0 (Low Byte) (B)%09	76543210	R		DSP EXT0, Bits D7-D0
Incoming Reg. to DSP EXT1 (High Byte) (B)%0A	76543210	R		DSP EXT1, Bits D15-D8
Incoming Reg. to DSP EXT1 (Low Byte) (B)%0B	76543210	R		DSP EXT1, Bits D7-D0
Incoming Reg. to DSP EXT2 (High Byte) (B)%0C	76543210	R		DSP EXT2, Bits D15-D8
Incoming Reg. to DSP EXT2 (Low Byte) (B)%0D	76543210	R		DSP EXT2, Bits D7-D0
Incoming Reg. to DSP EXT3 (High Byte) (B)%0E	76543210	R		DSP EXT3, Bits D15-D8
Incoming Reg. to DSP EXT3 (Low Byte) (B)%0F	76543210	R		DSP EXT3, Bits D7-D0

Expanded Register Bank F

Register	Position	Attrib.	Value	Description
PCON (F)%00				
	76543---			Reserved
	-----2--	R	0	Port 1 Open-drain
			1	Port 1 Push-pull Active*
	------1-	R	0	Port 0 Open-drain
			1	Port 0 Push-pull Active*
	-------0	R	0	P34, P35 Standard Output*
			1	P34, P35 Comparator Output
DSPCON (F)0CH				
Z8_SCLK	76------	R/W	00	2.5 MHz (OSC/8)
			01	5 MHz (OSC/4)
			1x	10 MHZ (OSC/2)
DSP_Reset	--5-----	R		Return '0'
		W	0	No effect
			1	Reset DSP
DSP_Run	---4----	R/W	0	Halt_DSP
			1	Run_DSP
Reserved	----32--		xx	
				Return '0'
				No effect
IntFeedback	------1-	R		FB_DSP_INT2
		W	1	Set DSP_INT2
			0	No effect
	-------0	R		FB_Z8_IRQ3
		W	1	Clear IRQ3
			0	No effect
P4 (F)%02	76543210	R/W	%NN	Port 4 Data Register
P4M (F)%03	76543210	R	%FF	Returns %FF
		W	0	Defines P4X as Output
			1	Defines P4X as Input
P5 (F)%04	76543210	R/W	%NN	Port 5 Data Register
P5M (F)%05	76543210	R	%FF	Returns %FF
		W	0	Defines P5X pin as Output
			1	Defines P5X pin as Input
P45CON (F)%06				
	765-321-			Reserved
	---4----	W	0	Port 5 Open-drain
			1	Port 5 Push-pull Active*
	-------0	W	0	Port 4 Open-drain
			1	Port 4 Push-pull Active*

Note:
* Default setting after Reset

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Z8 EXPANDED REGISTER FILE REGISTERS

Expanded Register Bank F (Continued)

Register	Position	Attrib.	Value	Description
SMR (F)%0B				
	7-------	R	0	POR*
			1	Stop Recovery
	-6------	W	0	Low Stop Recovery Level*
			1	High Stop Recovery Level
	--5-----	W	0	Stop Delay On*
			1	Stop Delay Off
	---432--	W		STOP-Mode Recovery Source
			000	POR Only*
			001	Reserved
			010	P31
			011	P32
			100	P33
			101	P27
			110	P2 NOR 0-3
			111	P2 NOR 0-7
	------1-			Reserved
	-------0	W	0	SCLK/TCLK Not Divide-by-16†
			1	SCLK/TCLK Divide-by-16
WDTMR (F)%0F				
	765-----			Reserved
	---4----	R/W	0	On-Board RC for WDT*
			1	XTAL for WDT
	----3---	R/W	0	WDT Off During STOP
			1	WDT On During STOP*
	-----2--	R/W	0	WDT Off During HALT
			1	WDT On During HALT*
	------10	R/W		Int RC Osc Ext Clock
			00	5 ms 256 TpC
			01*	15 ms 512 TpC
			10	25 ms 1024 TpC
			11	100 ms 4096 TpC

Notes:
* Default setting after Reset
† Reset after STOP-Mode Recovery

Z8 CONTROL REGISTERS

Register	Position	Attrib.	Value	Description
%F0	76543210			Reserved
TMR %F1				T_{OUT} Modes
	76------	RW	00	Not Used
			01	T0 Out
			10	T1 Out
			11	Internal Clock Out P36
				T_{IN} Modes
	--54----	RW	00	External Clock Input
			01	Gate Input
			10	Trigger Input (Non-Retriggerable)
			11	Trigger Input (Retriggerable)
	----3---	R/W	0	Disable T1 Count
			1	Enable T1 Count
	-----2--	R/W	0	No Effect
			1	Load T1
	------1-	R/W	0	Disable T0 Count
			1	Enable T0 Count
	-------0	R/W	0	No Effect
			1	Load T0
T1 %F2	76543210	R	%NN	T1 Current Value
		W	%NN	T1 Initial Value
PRE1 %F3	765432--	W		Prescaler Modulo (1-64 Dec)
	------1-			T1 Clock Source
		W	0	External Timing Input (T_{IN}) Mode
			1	Internal Clock
	-------0			T1 Count Mode
		W	0	Single Pass
			1	Modulo-n
T0 %F4	76543210	R	%NN	T0 Current Value
		W	%NN	T0 Initial Value
PRE0 %F5	765432--	W		Prescaler Modulo (1-64 Dec)
	------1-			Reserved
	-------0			T0 Count Mode
		W	0	Single Pass
			1	Modulo-n
P2M %F6	76543210	W	0	Defines P2X pin as Output
			1	Defines P2X pin as Input

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Z8 CONTROL REGISTERS (Continued)

Register	Position	Attrib.	Value	Description
P3M %F7				
	7-------			Reserved
	-6------	W	0	P30 = Input; P37 = Output
	--5-----	W	0	P31 = Input (T_{IN}); P36 = Output (T_{OUT})*
			1	P31 = /DAV2/RDY2; P36 = RDY2//DAV2
	---43---	W	00	P33 = Input; P34 = Output*
			01	P33 = Input; P34 = /DM
			10	P33 = Input; P34 = /DM
			11	P33 = /DAV1/RDY1; P34 = RDY1//DAV1
	-----2--	W	0	P32 = Input; P35 = Output*
			1	P32 = /DAV0/RDY0; P35 = RDY0//DAV0
	------1-	W	0	P31, P32 Digital Mode
			1	P31, P32 Analog Mode
	-------0	R/W	0	Port 2 Open-drain*
			1	Port 2 Push-pull Active
P01M %F8				T_{OUT} Modes
	76------	W		P04-P07 Mode
			00	Output
			01	Input*
			1x	A15-A12
	--5-----	W		External Memory Timing
			0	Normal*
			1	Extended
	---43---	W		P10-P17 Mode
			00	Byte Output
			01	Byte Input*
			10	AD7-AD0
			11	High-Z AD7-AD0, /AS, /DS/ R/W, A11-A8 A15-A12, If selected
	-----2--	W		Stack Selection
			0	External
			1	Internal*
	------10	W		P00-P03 Mode
			00	Output
			01	Input*
			1x	A11-A8

Note:
* Default setting after Reset.

Register	Position	Attrib.	Value	Description
IPR %F9	76------			Reserved
	--5-----	W		IRQ3, IRQ5 Priority (Group A)
			0	IRQ5 > IRQ3
			1	IRQ3 > IRQ5
	-----1--	W		IRQ0, IRQ2 Priority (Group B)
			0	IRQ2 > IRQ0
			1	IRQ0 > IRQ2
	-----2--	W		IRQ1, IRQ4 Priority (Group C)
			0	IRQ1 > IRQ4
			1	IRQ4 > IRQ1
	---43--0	W		Interrupt Group Priority
			000	Reserved
			001	C>A>B
			010	A>B>C
			011	A>C>B
			100	B>C>A
			101	C>B>A
			110	B>A>C
			111	Reserved
IRQ %FA	76------	R/W		Inter Edge (R = Rising edge; F = Falling edge)
			00	P31 = F; P32 = F
			01	P31 = F; P32 = R
			10	P31 = R; P32 = F
			11	P31 = RF; P32 = RF
	--543210	R/W		IRQ5 = T1
				IRQ4 = T0
				IRQ3 = DSP
				IRQ2 = P31 Input
				IRQ1 = P33 Input
				IRQ0 = P32 Input
IMR %FB	7-------	R/W	0	Disables Interrupts
			1	Enables Interrupts
	-6------	RW	0	Disables RAM Protect
			1	Enables RAM Protect
	--543210	R/W	0	Disables IRQ5-IRQ0 (D0 = IRQ0)
			1	Enables IRQ5-IRQ0
Flags %FC	7-------	R/W		Carry Flag
	-6------	R/W		Zero Flag
	--5-----	R/W		Sign Flag
	---4----	R/W		Overflow Flag
	----3---	R/W		Decimal Adjust Flag
	-----2--	R/W		Half Carry Flag
	------1-	R/W		User Flag F2
	-------0	R/W		User Flag F1
RP %FD	7654----	R/W	%N0	Working Register Group
	----3210	R/W	%0N	Expanded Register File Bank
SPH %FE	76543210	R/W	%NN	Stack Pointer Upper Byte
SPL %FF	76543210	R/W	%NN	Stack Pointer Lower Byte

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Z8 INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

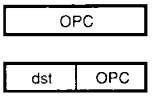
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

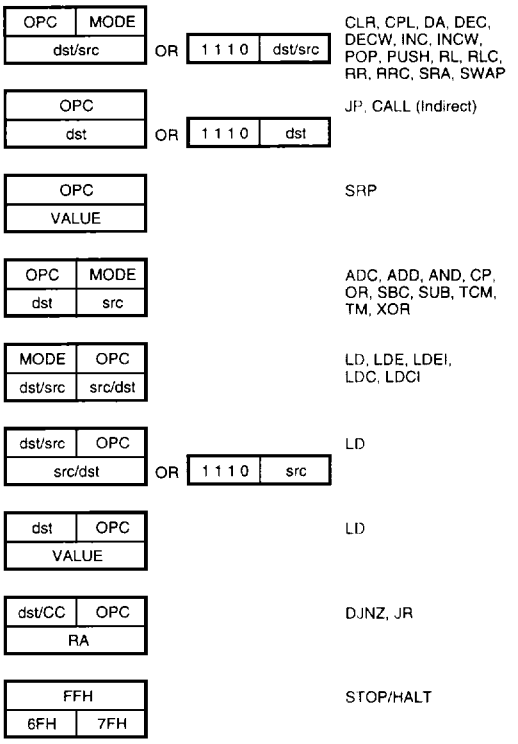
Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS

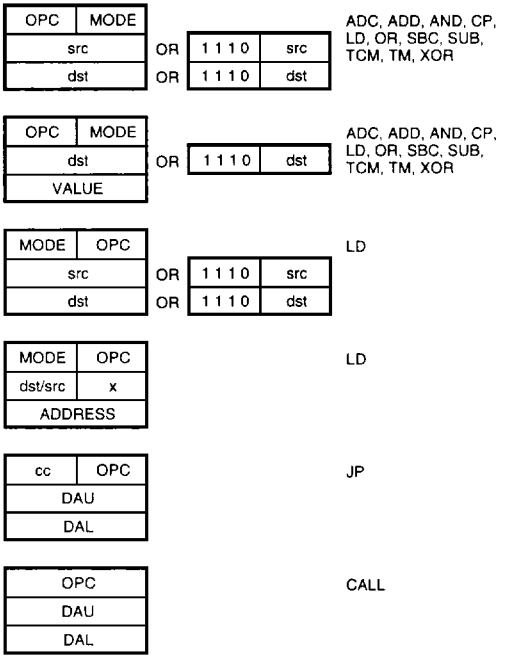


CCF, DI, EI, IRET, NOP, RCF, RET, SCF

One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZ dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r		rE r = 0 – F	-	*	*	*	-	-
	R		20						
	IR		21						
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r	Im	rC	-	-	-	-	-	-
	r	R	r8						
	R	r	r9						
			r = 0 – F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

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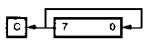
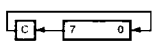
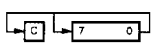
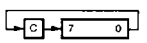
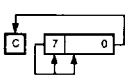
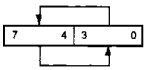
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5[ ]	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

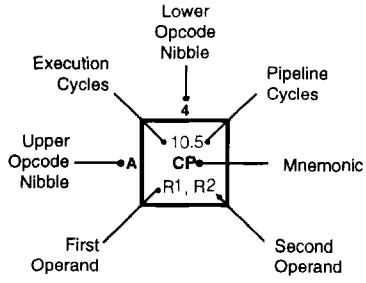
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1 x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2				3		1	



Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

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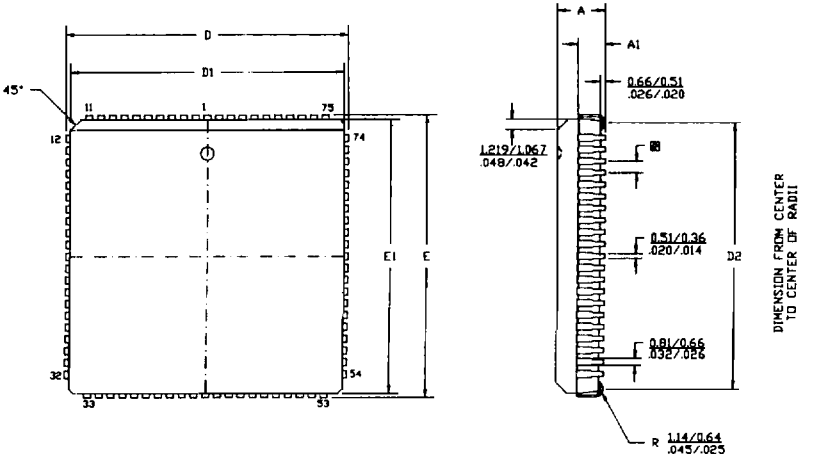
PACKAGE INFORMATION



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.67	2.92	.105	.115
D/E	30.10	30.35	1.185	1.195
D1/E1	29.21	29.41	1.150	1.158
D2	27.94	28.58	1.100	1.125
B	1.27 TYP		.050 TYP	

84-Lead PLCC Package Diagram

ORDERING INFORMATION

Z89121	Z89921
20 MHz	**20 MHz**
84-Pin PLCC	84-Pin PLCC
Z8912120VSC	Z8992120VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Speed
20 = 20.48MHz

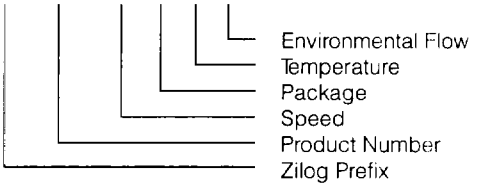
Package
V = Plastic Leaded Chip Carrier (PLCC)

Temperature
S = 0°C to + 70°C

Environment
C = Plastic Standard

Example:

Z 89121 20 V S C is a Z89121, 20.48 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow



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