Synertek.

SY6591/SY6591A

Floppy Disk Controller (FDC)

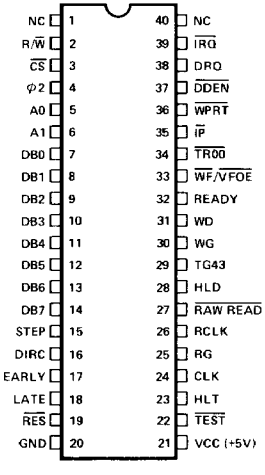
Features

- Functionally compatible with SY1791-02/SY1793-02
- MPU bus interface directly compatible with SY6500 and MC6800 microprocessors.
- Single 5 volt power supply
- Accommodates both single-density (FM) and double-density (MFM) formats
- IBM format compatibility:
  - IBM 3740 Single-Density
  - IBM System-34 Double-Density

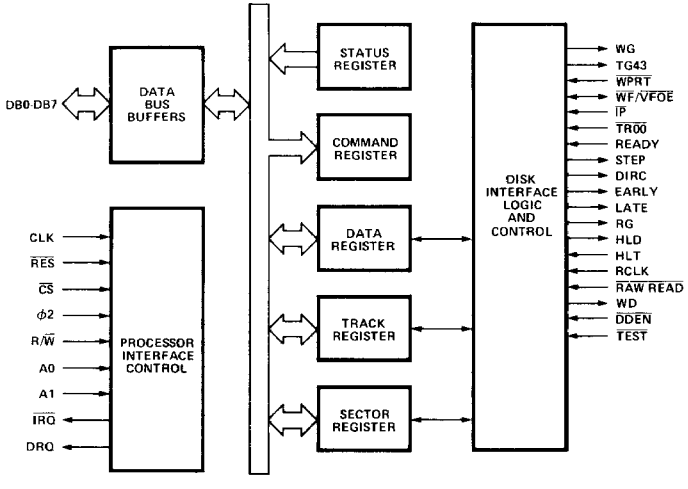
Description

The SY6591 Floppy Disk Controller is a fully programmable device intended for SY6500 or MC6800 microprocessor-based systems. The CPU bus interface is the only distinguishing difference between the 17XX series FDC and the 6591.

Pin Configuration



Block Diagram



MICRO PROCESSORS

Detailed List of Features

- Single 5 volt (±5%) power supply
- 40-pin package
- Automatic track seek with verification
- Accommodates single-density (FM) and double-density (MFM) formats
- Soft-sector format compatibility
- IBM 3740 (single-density) and System-34 (double-density) compatible
- Single or multiple record read with automatic sector search or entire track read
- Selectable record length (128, 256, 512 or 1024 bytes)
- Single or multiple record write with automatic sector search
- Entire track write for initialization
- Programmable controls:
  - Selectable track-to-track stepping time
  - Selectable head settling and engage times
  - Head position verification
  - Side verification
- Double-buffered read and write data flow
- DMA or programmed data transfers
- TTL-compatible inputs and outputs
- Write precompensation (FM and MFM)
- Comprehensive status register

Processor Interface Signals

- $\phi 2$ ($\phi 2$) — The $\phi 2$ signal is combined with $\overline{CS}$ to gate the processor interface signals A0, A1 and R/$\overline{W}$ into the floppy disk controller (FDC).
- DATA BUS (DB0-DB7) — This 8-bit non-inverting bidirectional data bus is used for transferring data, control, and status words. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.
- READ/WRITE (R/$\overline{W}$) — This input signal is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read data supplied by the FDC. A low on the R/$\overline{W}$ pin allows data to be written to the FDC.
- INTERRUPT REQUEST ($\overline{IRQ}$) — The $\overline{IRQ}$ is an open drain output. This signal goes low at the completion or termination of any operation and is reset when a new command is loaded into the command register or when the status register is read. An external pull-up resistor to V_{CC} is required when using the SY6591 with a SY6500 or a MC6800 MPU.
- RESET ($\overline{RES}$) — This signal is identical to $\overline{MR}$ on the SY1791-02/SY1793-02. A low on this input resets the device and loads hex 03 into the command register. The Not Ready status bit (status bit 7) is reset during $\overline{RES}$ low. When $\overline{RES}$ is driven high, a Restore command is executed regardless of the state of the Ready signal, and hex 01 is loaded into the Sector Register.
- REGISTER ADDRESS LINES (A0-A1) — These inputs address the internal registers for access by the Data Bus lines under R/$\overline{W}$ and $\phi 2$ control.

REGISTER ADDRESS CODES

A1	A0	READ	WRITE
0	0	STATUS	COMMAND
0	1	TRACK	
1	0	SECTOR	
1	1	DATA	

- READ/WRITE (R/$\overline{W}$) — If $\overline{CS}$ is low, a high on this input enables the addressed internal register to output data onto the data bus when $\phi 2$ is high. If $\overline{CS}$ is low, then a low on this input gates data from the data bus into the addressed register when $\phi 2$ is high.
- CHIP SELECT ($\overline{CS}$) — A low level on this input selects the FDC and enables processor communications with the FDC.
- DATA REQUEST (DRQ) — DRQ is an open drain output. DRQ high during read operations indicates that the Data Register (DR) contains data. When high during write operations, DRQ indicates that the DR is empty and ready to be loaded. DRQ is reset by reading or loading the DR during read or write operations, respectively. Use 10K pull-up resistor to V_{CC}.
- CLOCK (CLK) — This input requires a square wave clock for internal timing reference (2 MHz for 8-inch drives, 1 MHz for 5-inch drives).

1.3 Floppy Disk Interface Pin Functions

- READ GATE (RG) — A high on this output indicates that a field of zeroes (zeroes or ones) has been detected in FM (MFM) encoded information. This can be used to indicate to a data separator that a sync field has been found.
- WRITE DATA (WD) — This output to the disk drive electronics supplies one pulse per required flux transition.
- READ CLOCK (RCLK) — The RCLK input is a nominal square-wave clock signal derived from the data stream. Phasing (RCLK relative to $\overline{\text{RAW READ}}$) is important, but polarity (RCLK high or low) is not.
- RAW READ ($\overline{\text{RAW READ}}$) — This is the data input to the FDC from the drive. This input must be a negative pulse for each recorded flux transition.
- HEAD LOAD (HLD) — The HLD output notifies the drive to engage the Read/Write head against the medium.
- HEAD LOAD TIMING (HLT) — The HLT input, which is generated by external logic, indicates that a sufficient time has elapsed for the head to have engaged.
- STEP — The step output provides a pulse to the disk drive electronics to cause each incremental head movement.
- DIRECTION (DIRC) — The DIRC output defines the direction of the step. It is high for stepping the head in towards track 76, and low for stepping the head out towards track 0.
- EARLY — A high EARLY output indicates to external circuitry that the WD pulse should be shifted early for write precompensation.
- LATE — A high LATE output indicates to external circuitry that the WD pulse should be shifted late for write precompensation.
- TRACK GREATER THAN 43 (TG43) — This output informs the drive that the Read/Write head is positioned between tracks 44-255 inclusive. This output is valid during Read and Write commands.
- WRITE GATE (WG) — The WG output is set high when writing to the disk if all the Write prerequisites have been met. WG is used to enable the drive's write circuitry.
- READY — This input indicates disk readiness to perform any Read or Write command. READY must he high for a Read or Write command to be accepted. If READY is low and the FDC receives any such command, the command is not executed and an interrupt is generated if the Not-Ready status bit is set.
- WRITE FAULT ($\overline{\text{WF}}$)/VFO ENABLE ($\overline{\text{VFOE}}$) — This pin is used as both an input and output. During Write operations after WG is high, this pin acts as an input to sense a negative transition indicating a Write Fault. If a Write Fault is detected, the Write command is terminated, the Write Fault status bit is set, and INTRQ goes high.

  During Read operations, $\overline{\text{WF}}$/$\overline{\text{VFOE}}$ is an output used to synchronously control external RCLK circuitry. $\overline{\text{VFOE}}$ will go true (low) when the following are all true:

  1. HLD and HLT are true;
  2. settling time, if programmed, has expired;
  3. the SY6591 is inspecting data from the disk.

- TRACK 00 ($\overline{\text{TR00}}$) — This input, when low, indicates to the FDC that the Read/Write head is positioned over track Ø.
- INDEX PULSE ($\overline{\text{IP}}$) — This input is generated by the drive electronics to indicate the start of a track.
- WRITE PROTECT ($\overline{\text{WPRT}}$) — This input is sampled whenever a Write command is received. A low terminates the command and sets the Write Protect status bit.
- DOUBLE DENSITY ($\overline{\text{DDEN}}$) — This input selects either single or double density operation. When $\overline{\text{DDEN}}$ is low, double density is selected. When $\overline{\text{DDEN}}$ is high, single density is selected.
- TEST ($\overline{\text{TEST}}$) — This input is used for testing purposes and should be tied to +5V, or left open, by the user unless interfacing to voice coil motors. When low, the motor stepping rate is increased (see Figure 3b).

2.0 FUNCTIONAL OPERATION

2.1 Single/Double Density Selection

The SY6591 has two selectable data densities, determined by input $\overline{\text{DDEN}}$.

2.2 Clock Selection

In addition to $\overline{\text{DDEN}}$, the CLK input determines overall circuit timings, and must be properly selected. A 1MHz CLK input is normally used for 5" mini-diskette drives and 2MHz for standard 8" drives.

2.3 DRQ Operation

The DRQ output indicates that a data transfer operation is required. For disk read operations, DRQ signifies that the Data Register needs to be read so that the next data byte can be received. For disk write operations, DRQ signifies that a data byte has been transmitted and another must be entered. DRQ may be used as a "handshake" control signal in a DMA based system.

2.4 DMA Sequences

In disk read operations, DRQ goes high when a serial data byte is assembled in the Data Register. DRQ is reset when the byte is read by the DMA controller (or system processor). If a newly assembled byte is transferred into the DR (from the DSR) before the DR has been read, then the overwritten byte in the DR is lost. Furthermore, the Lost Data status bit in the Status Register is set, to indicate this condition. Read operations continue until the end of sector is encountered.

Disk write operations are similar. DRQ is activated when the data byte is transferred from the Data Register to the Data Shift Register, indicating that the DR is ready to be loaded with another byte. It is cleared when the new byte is loaded by the DMA controller (or system processor). However, if the new byte is not loaded by the time the prior byte is shifted out, then a byte of all zeroes is written on the diskette and the Lost Data status bit in the Status Register is set.

2.5 Disk Read Operations

For disk read operations, the FDC requires $\overline{\text{RAW READ}}$ and RCLK inputs. $\overline{\text{RAW READ}}$ is a low going pulse for each flux transition. The FDC detects the rising and falling edges of RCLK and uses these edges to frame $\overline{\text{RAW READ}}$ data/clock inputs. RCLK is provided by some drives, but if not it must be provided externally (phase-lock-loops, one-shots, counters, etc.) To assist in generating RCLK, the FDC has a RG (Read Gate) output, which may be used to acquire synchronization. Whenever two bytes of zeroes are detected in read operations (in single-density mode), RG is activated (high) and the FDC must find a valid AM (Address Mark) within the next 10 bytes. If the AM is not found, RG is deactivated (low) and the search for two bytes of zeroes is re-started. If the AM is found, RG remains active as long as the FDC is deriving data from the diskette. For double-density mode, RG is activated when 4 bytes of hex ØØ or hex FF are detected and the FDC must find the AM within 16 bytes.

2.6 Disk Write Operations

The fundamental signals in write operations are: WD (Write Data) output, WG (Write Gate) output, $\overline{\text{WPRT}}$ (Write Protect) input, and $\overline{\text{WF}}$ (Write Fault) input. When writing to the diskette, WG goes high enabling the disk drive write electronics. However, WG will not be activated until the first data byte has been loaded in the Data Register. This ensures that false writing will not occur. Writing is inhibited when $\overline{\text{WPRT}}$ is low. This sets the Write Protect status bit and an interrupt (INTRQ) is generated.

The $\overline{\text{WF}}$ input signifies a fault condition at the disk drive. When low, it causes the current command to terminate, sets the Write Fault bit in the Status Register, and generates the INTRQ interrupt.

2.7 Write Precompensation

EARLY and LATE are two additional signals which are generated by the SY6591 during write operations. They are used for write precompensation functions. Both signals are active-high. The EARLY signal is active when the WD pulse is to be written early; the LATE signal is active when WD is to be written late. If neither signal is active, then WD is to be written at its normal time. EARLY and LATE are valid for both single and double density modes.

3.0 Command Words

The FDC accepts eleven commands. Command words should be loaded in the Command Register only when the Busy status bit (status bit Ø) is low. The sole exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Figure 2.

		BIT							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	RESTORE	0	0	0	0	h	V	r_1	r_0
	SEEK	0	0	0	1	h	V	r_1	r_0
	STEP	0	0	1	u	h	V	r_1	r_0
	STEP IN	0	1	0	u	h	V	r_1	r_0
	STEP OUT	0	1	1	u	h	V	r_1	r_0
II	READ SECTOR	1	0	0	m	S	E	C	0
	WRITE SECTOR	1	0	1	m	S	E	C	a_0
III	READ ADDRESS	1	1	0	0	0	E	0	0
	READ TRACK	1	1	1	0	0	E	0	0
	WRITE TRACK	1	1	1	1	0	E	0	0
IV	FORCE INTERRUPT	1	1	0	1	I_3	I_2	I_1	I_0

1 = HIGH LEVEL 0 = LOW LEVEL

Figure 2. Command Summary

3.1 Type I Commands

The Type I commands are Restore, Seek, Step, Step-In, and Step-Out.

- RESTORE — The RESTORE command is used to position the Read/Write head to track Ø of the diskette. Upon the receipt of this command, the $\overline{\text{TR00}}$ input is sampled. If $\overline{\text{TR00}}$ is low, indicating the Read/Write head is positioned over track Ø, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TR00}}$ is not low, step pulses at a rate specified by the r_1r_0 field are issued until the $\overline{\text{TR00}}$ input is asserted. At this time, the TR is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TR00}}$ input does not go low after 255 stepping pulses, the FDC terminates operation, interrupts and sets the Seek Error status bit. A verification operation takes place if the V bit is set. The h bit allows the head to be loaded at the start of the command. Note that the Restore command is executed when $\overline{\text{MR}}$ goes from low (true) to high (false).

- SEEK — This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The FDC will update the Track Register and issue stepping pulses until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V bit is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.
- STEP — Upon receipt of this command, the FDC issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V bit is on. If the u bit is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.
- STEP-IN — Upon receipt of this command, the FDC sets DIRC high and issues one stepping pulse. If the u bit is on, the Track Register is incremented. After a delay determined by the r_1r_0 field, a verification takes place if the V bit is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.
- STEP-OUT — This command is identical to the Step-In command, except that DIRC is set low and the Track Register is decremented for each step pulse if the u bit is high.

3.1.1 Type I Command Option Bits

The operation of the option determining bits for Type I commands is summarized in Figures 3a and 3b.

The detailed descriptions of the Type I option bits follow.

- r_1r_0 (Step Rate) — These bits select the rate at which step pulses are issued. Note that the stepping rates are independent of $\overline{DDEN}$ select. Both single and double-density modes step at the same rate.
- V (VERIFY) — This bit is used to select track verification at the end of the stepping sequence. During verification, the head is loaded and after an internal head settling time delay* ($\overline{TEST}$ = 1), the HLT input is sampled. When HLT is true, the first encountered ID field is read from the disk. The track address of the ID field is then compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match, but there is a valid ID CRC, an interrupt is generated, the Seek Error status bit (status bit 4) is set, and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC Error status bit (status bit 3) is set, and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FDC terminates the operation and generates an interrupt.
- h (Head Load) — This bit determines if the head is to be loaded at the beginning of the command. If so, the HLD output goes high (active) and remains in this state until the FDC receives a command to disengage the head. If the FDC is idle (not Busy) for 15 disk revolutions, then the head is automatically disengaged (HLD goes low). If track verification is selected (V = "1"), then the head loading is affected, as follows:
  - h = 0, V = 1
    HLD is activated near the end of the sequence, an internal head settling time delay* occurs, and the FDC waits for the HLT input to go active (high) before verifying track identification.
  - h = 1, V = 1
    HLD is activated at the start of the sequence. At the end, an internal head settling time delay* occurs and the FDC waits for HLT to go active before verification.

  *Head settling time delay is 15 msec for 2 MHz clock, 30 msec for 1 MHz clock.
- u (Update) — With Update selected (u = "1"), the Track Register is updated at each step pulse. The update operation increments the Track Register for stepping in toward track 76 and decrements it for stepping out toward track 0.

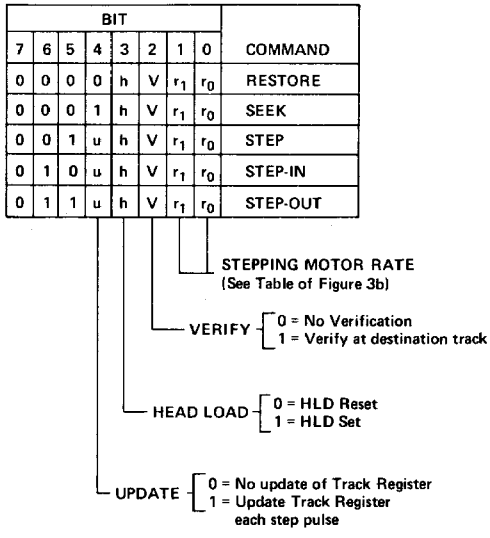


Figure 3a. Type I Command Option Bit

$\overline{TEST}$	r_1	r_0	STEPPING RATE	
			CLK = 1MHz	CLK = 2MHz
H	0	0	6 ms	3 ms
H	0	1	12 ms	6 ms
H	1	0	20 ms	10 ms
H	1	1	30 ms	15 ms
L	—	—	~400μs	~200μs

Figure 3b. Stepping Motor Rates

3.2.1 Type I Command Signals

Type I commands control the operation of the STEP and DIRC (Direction) output signals of the FDC.

- STEP — A 2 μs (MFM) or 4 μs (FM) positive-true output pulse is generated at a rate determined by the r_1r_0 field of the command (see Figure 3b). Each step pulse moves the Read/Write head one track location in a direction controlled by the DIRC output.
- DIRC — The DIRC output determines the direction of the track stepping. A high level indicates step direction IN towards track 76, a low level indicating direction OUT towards track Ø.

In addition, the Type I commands use the following signals:

- HLD (Head Load) — This output is used to control movement of the Read/Write head against the recording medium. HLD is set at the beginning of a Type I command if h = "1", near the end of a Type I command if V = "1" and h = "0", or immediately when a TYPE II or TYPE III command is executed. Once HLD is set it remains high until a subsequent Type I command with h = "0" and V = "0" is loaded, or until the FDC goes into its non-busy state after 15 index pulses.
- HLT (Head Load Timing) — The low to high transition of this input indicates that a sufficient time has elapsed for the drive's head to become engaged. It typically follows HLD going high, by a time delay which is dependent on the particular drive's characteristics. If not available from the drive electronics, this input must be generated by the user (typically by means of one-shot timers). Figure 4 illustrates an example of HLD and HLT timing.

  The logical AND of HLD and HLT is status bit 5 for Type I commands, and it controls the operation of the disk read and write functions.

3.2 Type II Commands

The Type II commands, Read Sector and Write Sector, permit actual data to be read from or written onto the diskette. Before the command is entered, it is necessary for the processor to have loaded the Sector Register with the number of the desired sector. Figure 5 is useful for understanding the operation of Type II commands.

3.2.1 Type II Command Basic Operation Sequence

The basic operation of Type II commands is outlined as the following sequence:

— The ID field is located by the detection of the ID AM (ID Address Mark).

— The Track Number in the ID field is compared to the contents of the Track Register. If it does not match, then the ID AM search begins again.

— As a selectable option, the Side Number is checked for a match. If selected, a failure to match again causes the ID AM search to re-start.

— The Sector Number is compared to the contents of the Sector Register. If there is not a match, the ID AM search is again begun.

— The Sector Length field is entered into the FDC and stored internally for use in Read or Write operations. The value of the Sector Length byte is determined when the diskette is formatted (initialized) and must have one of the values in the table of Figure 6.

— The ID field CRC1 and CRC2 bytes are checked with internally generated CRC. If they match, then the command (Read or Write) is permitted; if not, the CRC Error status bit is set and the search for the ID AM is begun again.

If the Track Number, Side Number, Sector Number, and CRC all check properly within 4 disk revolutions (5 index pulses), then the command continues; otherwise the Record-Not-Found status bit is set and the command is terminated with an interrupt (INTRQ).

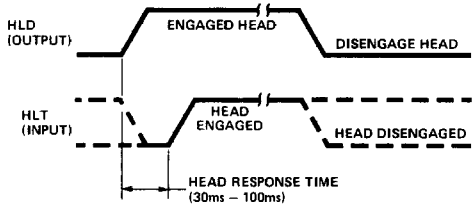


Figure 4. HLD/HLT Timing Example

SECTOR LENGTH FIELD (hex)	NUMBER OF BYTES IN SECTOR
00	128
01	256
02	512
03	1024

Figure 6. Sector Length Field Codes

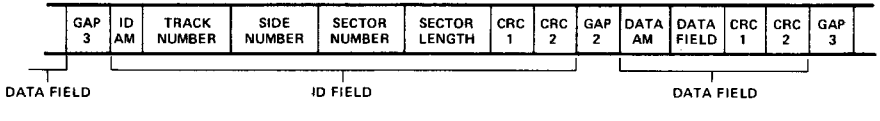


Figure 5. General Track Format

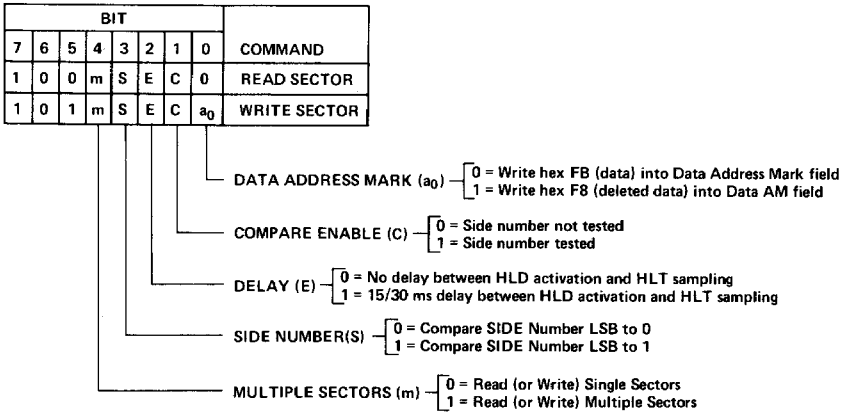


Figure 7. Type II Command Option Bits

3.2.2 Type II Command Option Bits

Several bits in the Type II command words are used to select various options. Figure 7 summarizes the special control bits which are outlined, as follows:

- a_0 (Data AM) — The a_0 bit is used to select which of two Data Address Mark bytes is to be stored in the Data AM field for Write Sector operations. A "1" in a_0 causes hex F8 to be stored, indicating that the data field is actually deleted data. A "0" in a_0 causes hex FB to be stored, indicating undeleted data.
- S (Side) — The S bit is compared with the LSB of the Side Number (in the ID field), if the side number compare option has been enabled by the C bit.
- C (Compare) — This bit enables the comparison of the Side Number (in the ID field) with the S bit of the Type II command.
- E (Delay) — The E bit causes the internally generated head settling delay to be inserted between the time the HLD (Head Load) output is activated and the time the HLT (Head Load Timing) input is strobed and checked.
- m (multiple Records) — This bit is used to select whether one sector (m = "0") or more than one sector (m = "1") is to be read or written. For single sector operation, the interrupt is generated and the command is terminated immediately after the sector operation is complete. Multiple sector operation, however, is somewhat different. After the first sector operation is complete, the FDC Sector Register is incremented and the sequence is re-started. In this way, the next sequential sector number is read or written. Likewise, after it is complete, the Sector Register is again updated and the sequence re-started. This continues until the Sector Register has incremented to a number higher than any sector on the current track. At this point, the sequence terminates.

3.2.3 Type II Command Operation

The specific operation of the Read Sector and Write Sector commands, once the ID field is properly encountered, is outlined below:

- READ SECTOR — When the correct Track Number, Side Number (if selected), Sector Number, and CRC have been identified, the Data Field check commences. The Data AM must be found within 30 bytes for single-density (or 43 bytes for double-density) from the time the last CRC byte for the ID field was encountered. If not, the Record-Not-Found bit in the Status Register is set and the command is terminated. After the Data AM is found, the data bytes are entered through the internal Data Shift Register and transferred to the Data Register. Each byte transferred results in a DRQ. The Data Register must be unloaded (read) by the MPU or DMA controller before the next byte is fully received. If not, then the new byte is written over the previous byte in the Data Register, the previous byte is lost, and the Lost Data status bit is set. At the end of the Data Field, the CRC bytes are compared to the internal CRC generated by the FDC. If they do not match, the CRC Error status bit is set and the command is terminated, even if it is a multiple-record command (m = "1"). At the end of the sequence, the Data AM encountered in the Data Field determines bit 5 of the Status Register. If the Data AM was hex FB (undeleted), then bit 5 is set to "0"; hex F8 (deleted data) causes bit 5 to be set to "1".
- WRITE SECTOR — The Write Sector command operates in a fashion very similar to Read Sector. When the correct Track Number, Side Number (if selected), Sector Number, and CRC have been identified, a DRQ is generated, requesting the first data byte which is to be written on the diskette. The FDC then counts 11 bytes for single-density (or 22 bytes for double-density) to account for part of the gap between the ID

and DATA fields (Gap 2 in Figure 5). At this point, if the DRQ has been serviced and a data byte stored in the Data Register, the WG output goes true (high) and 6 bytes of zeroes for single-density (12 bytes for double-density) are written on the diskette. This accounts for the remainder of Gap 2. (If the DRQ had not been serviced, the Lost Data status bit would have been set and the command terminated). Following Gap 2, the Data AM is written. This byte is either hex FB (undeleted data) or hex F8 (deleted data) and is determined by the state of the a_0 bit in the command byte, (see Figure 7). Finally, the data is written on the diskette, starting with the byte already loaded in the Data Register. As each byte is transferred from the Data Register to the Data Shift Register to be stored on the diskette, a DRQ is generated to the MPU or DMA control unit requesting the next data. If any DRQ is not serviced in time, the Lost Data status bit is set and a byte of zeroes is stored on the diskette, but the command is not terminated. After the last data byte is stored on the diskette, the two-byte CRC (generated in the FDC) is then stored on the diskette. Finally, after the CRC bytes, the FDC stores one more byte (hex FF), the WG output goes low (false), and the command is terminated.

3.3 Type III Commands

There are three Type III Commands:

- READ ADDRESS — Read the next ID field (6 bytes) into the FDC.
- READ TRACK — Read all bytes of the entire track, including gaps.
- WRITE TRACK — Write all bytes to the entire track, including gaps.

3.3.1 Type III Command Option Bit

There is one option bit for Type III commands.

- E (DELAY) — This option bit acts the same for Type III commands as it does for Type II commands. See section 3.2.2 for further information.

3.3.2 Type III Command Operation

- READ ADDRESS — When this command is issued, the head is loaded (HLD high) and the Busy status bit is set. The next ID field encountered on the diskette is then read a byte at a time, using DRQ initiated data transfers to the MPU or DMA controller. Six bytes are entered, comprising the entire ID field. They are: Track Number (1 byte); Side Number (1 byte); Sector Number (1 byte); Sector Length (1 byte); and CRC (2 bytes). Although the CRC bytes are passed unaltered, the FDC checks their validity and sets the CRC Error status bit accordingly. Part of the operation of this command causes the Track Number to be stored in the Sector Register of the FDC. The command ends with the generation of an interrupt (INTRQ) and the clearing of the Busy status bit.
- READ TRACK — The initiation of this command causes the head to be loaded (HLD active) and the Busy status bit to be set. Reading of the track starts with the next encountered Index pulse and continues until the following Index Pulse. Each byte is assembled and transferred to the Data Register. As in any normal read operation, a DRQ output is generated with each byte, signalling to the MPU or DMA control unit that the byte is ready. CRC and Gap bytes are treated as any other byte. No CRC checking is performed. When all bytes are transferred, the Busy status bit is cleared, and INTRQ goes high.
- WRITE TRACK — The start of this command causes the head to be loaded (HLD active) and the Busy status bit to be set. Data is written onto the track when the first Index pulse is encountered, and terminated at the subsequent Index Pulse. DRQ is activated immediately after the command is issued to permit adequate time for the first byte to be made available before the Index is found. If this time is not enough and the Index Pulse occurs before the Data Register is loaded, then the command is terminated. Once the data transfers begin, the DRQ is generated for each byte as needed. Any byte which is not transferred into the FDC in time causes a byte of all zeroes to be stored on the diskette instead. Address Marks and CRC bytes are generated by the FDC in response to format control bytes supplied by the system MPU or DMA control unit. When all bytes are transferred, the command is terminated, the Busy status bit is cleared, and INTRQ is set high.

3.4 Type IV Command

Force Interrupt is the only Type IV command. This command permits the MPU to terminate (abort) any command in progress. Figure 8 tabulates the Type IV command option bits.

The four bits, I_0-I_3, are used to select the condition of the interrupt occurrence. Regardless of which bit is set, any command currently being executed is immediately terminated and the Busy status bit is cleared, indicating "Not Busy". Then, when the condition is met, INTRQ goes high, causing the required interrupt.

If I_0-I_3 are all "0", no interrupt occurs, but any currently executing command is immediately terminated. If more than one condition is selected, then the interrupt occurs when any of the conditions is met.

To clear the interrupt, it is necessary to read the Status Register or to write the Command Register. An exception, however, is for $I_3 = 1$ (Immediate Interrupt). For this case, the interrupt is cleared with another Force Interrupt command with I_0-I_3 all 0.

3.5 Status Register

The Status Register permits the MPU to monitor a variety of conditions in the FDC. For each command, the individual status bits have their own meaning. When a command is initiated (except for the Force Interrupt command), the Busy status bit is set and the others are cleared or updated. If the Force Interrupt command is entered when another command is in progress, the Busy status bit is cleared, but the others remain unaffected. However, if the Force Interrupt command is initiated

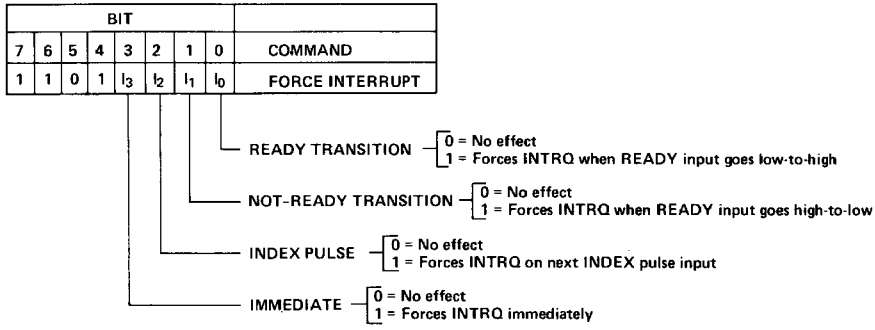


Figure 8. Force Interrupt Command Flags

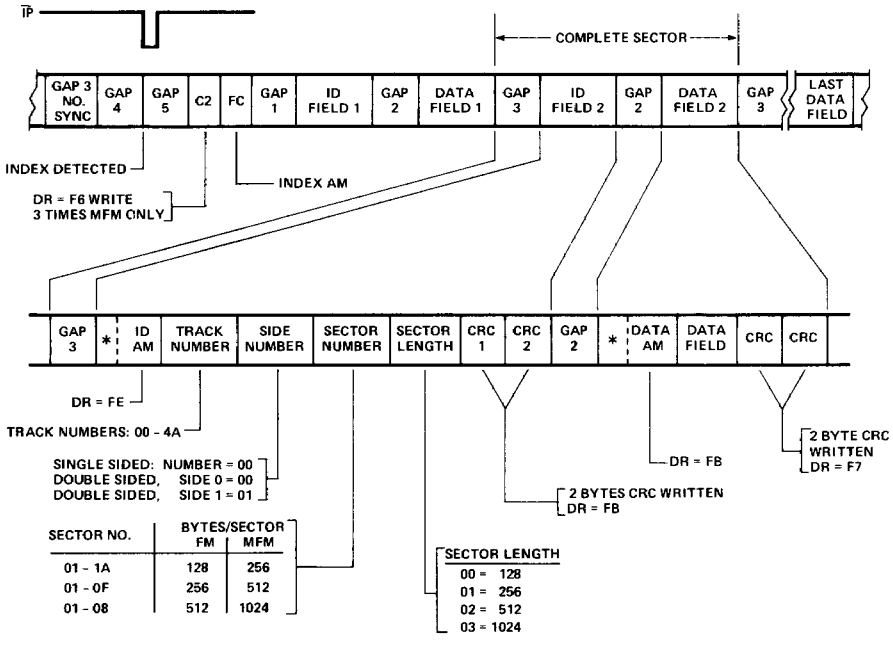
COMMAND	STATUS BIT							
	7	6	5	4	3	2	1	0
ALL TYPE I	Not Ready	Write Protect	Head Loaded	Seek Error	CRC Error	Track 0	Index	Busy
READ SECTOR	Not Ready	0	Record Type	Rec not Found	CRC Error	Lost Data	DRQ	Busy
WRITE SECTOR	Not Ready	Write Protect	Write Fault	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ ADDRESS	Not Ready	0	0	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ TRACK	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
WRITE TRACK	Not Ready	Write Protect	Write Fault	0	0	Lost Data	DRQ	Busy

Figure 9. Status Register Summary

when there is not another command in progress, the other status bits are cleared or updated and represent the Type I Command status. Figure 9 illustrates the meaning of the status bits for each command.

Detailed descriptions of each status bit function follow:

- NOT READY
  0 = Drive is Ready
  1 = Drive is Not Ready
- WRITE PROTECT
  0 = $\overline{\text{WPRT}}$ input is high (unprotected)
  1 = $\overline{\text{WPRT}}$ input is low (protected)
- HEAD LOADED
  0 = Head is not currently loaded
  1 = Head is loaded and engaged (both HLD and HLT are active)
- SEEK ERROR
  0 = Desired track was found. Updating clears this bit
  1 = Desired track was not found
- TRACK 0
  0 = $\overline{\text{TR00}}$ input is high
  1 = $\overline{\text{TR00}}$ input is low (Read/Write head is on Track Ø)
- INDEX
  0 = $\overline{\text{IP}}$ input is high (no index mark)
  1 = $\overline{\text{IP}}$ input is low (index mark)
- BUSY
  0 = Not Busy
  1 = Busy (Command sequence in progress)
- RECORD TYPE
  0 = Non-deleted data mark
  1 = Deleted data mark
- WRITE FAULT
  0 = No write fault
  1 = Write fault has occurred
- RECORD NOT FOUND
  0 = Desired track and sector properly found. Updating clears this bit
  1 = Desired track and sector not found
- CRC ERROR
  0 = No CRC error. Updating clears this bit
  1 = CRC check error encountered
- LOST DATA
  0 = No data lost. Updating clears this bit
  1 = MPU did not respond to DRQ. Data was lost
- DATA REQUEST (DRQ)
  0 = DRQ not in progress. Updating clears this bit.
  1 = DRQ currently in progress



*3 bytes of A1 for MFM synchronization.

Figure 10. IBM Compatible Sector/Track Format

4.0 Disk Formatting

Disk formatting (initialization) is accomplished by the Write Track command. Each byte for the entire track must be provided for proper formatting. This includes gap as well as data bytes.

The sequence required to format a diskette begins with positioning the Read/Write head at the desired track. Once this has been done, it is necessary to perform a Write Track command to store all the information on a track. The Write Track command uses DRQ to request each byte from the system MPU, starting with the byte at the beginning of the physical Index Pulse and ending with the last gap bytes at the end of the track. Figure 10 illustrates the IBM standard for track formatting.

Normally, each data byte stored on the diskette must be generated by the system MPU and passed into the FDC Data Register. However, there are exceptions to this rule. If a data byte of hex F5 through FE is entered into the Data Register, then the FDC recognizes this as Data AM with missing clocks or CRC generation code. Consequently, F5 through FE must not be used in gaps, data fields, or ID fields, as this will disrupt normal operation of the FDC during formatting.

4.1 IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 11.

4.2 IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 12.

4.3 Non-IBM Formats

Unique (non-IBM) formats are permissible providing the following restrictions are understood.

- Sector length may only be 128, 256, 512, or 1024 bytes.
- Gap sizes must conform to Figure 13.

	DATA BYTE (hex)	NO. OF BYTES	COMMENTS
	FF	40	Gap 5 (Post Index)
	00	6	
	FC	1	Index AM
	FF	26	Gap 1
	00	6	
	FE	1	ID AM
	XX	1	Track Number (00-4A)
	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	00	1	Sector Length (128 bytes)
ONE SECTOR (1)	F7	1	Causes 2-Byte CRC to be Written
	FF	11	Gap 2 (ID Gap)
	00	6	
	FB	1	Data AM
	E5	128	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	FF	27	Part of Gap 3 (Data Gap)
	FF	247 (2)	Gap 4 (Pre Index)

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX FF UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT

Figure 11. Byte Sequence for IBM 3740 Formatting

	DATA BYTE (hex)	NO. OF BYTES	COMMENTS
	4E	80	Gap 5 (Post Index)
	00	12	
	F6	3	Writes C2
	FC	1	Index AM
	4E	50	
	00	12	Gap 1
	F5	3	Writes ID AM Sync Bytes
	FE	1	ID AM
	XX	1	Track Number (00-4C)
	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	01	1	Sector Length (256 Bytes)
ONE SECTOR (1)	F7	1	Causes 2-Byte CRC to be Written
	4E	22	Gap 2 (ID Gap)
	00	12	
	F5	3	Writes ID AM Sync Bytes
	FB	1	Data AM
	40	256	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	4E	54	Part of Gap 3 (Data Gap)
	4E	598 (2)	Gap 4 (Pre Index)

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX 4E UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT.

Figure 12. Byte Sequence for IBM System-34 Formatting

GAP	SINGLE DENSITY (FM)	DOUBLE DENSITY (MFM)	NOTE
Gap 1	16 bytes FF	16 bytes 4E	2
Gap 2	11 bytes FF 6 bytes 00	22 bytes 4F 12 bytes 00 3 bytes A1	1
Gap 3	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1	2
Gap 4	16 bytes FF	16 bytes 4E	2

NOTES: 1. THESE BYTES COUNTS ARE EXACT.
2. THESE BYTES COUNTS ARE MINIMUM EXCEPT FOR 3 BYTES A1, WHICH IS EXACT.

Figure 13. Gap Size Limitations

Electrical Specifications

Absolute Maximum Ratings*

Rating	Symbol	Allowable Range
Supply Voltage	V_{CC}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to +7.0V
Operating Temp.	T_{OP}	0°C to 70°C
Storage Temp.	T_{STG}	-55°C to 150°C

Comment*

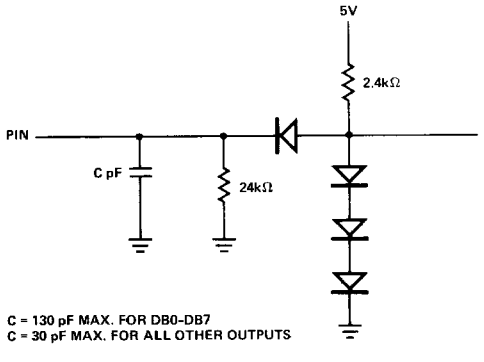
All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics (V_{CC} = 5V ± 5%, T_A = 0-70°C)

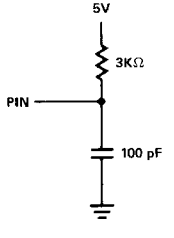
CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage	V_{IH}	2.0	–	V
Input Low Voltage	V_{IL}	–	0.8	V
Input Leakage Current, V_{IN} = 0V to V_{CC}	I_{IL}	–	± 10	μA
Output High Voltage, I_{LOAD} = -100 μA	V_{OH}	2.4	–	V
Output Low Voltage, I_{LOAD} = 1.6 mA	V_{OL}	–	0.4	V
Output Leakage Current, V_{OUT} = V_{CC}	I_{OL}	–	10	μA
Power Dissipation (V_{CC} = 5.25 V)	P_D	–	525	mW
Input Capacitance	C_{IN}	–	15	pF

Test Load



C = 130 pF MAX. FOR DB0-DB7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS

OPEN COLLECTOR OUTPUT TEST LOAD

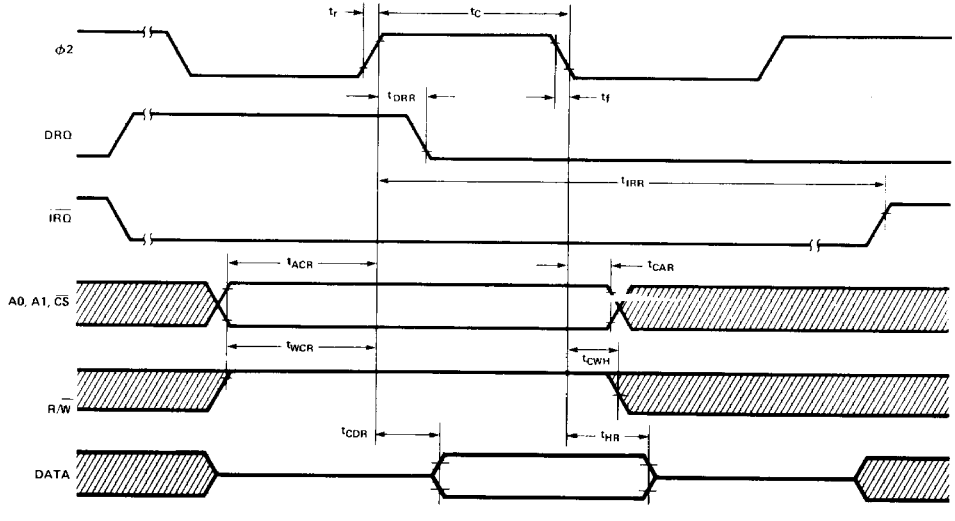


Read Cycle (V_{CC} = 5.0V ±5%, T_A = 0 to70°C, unless otherwise noted)

Characteristic	Symbol	6591		6591A		Units
		Min.	Max.	Min.	Max.	
$\phi 2$ Pulse Width	t_C	470	–	235	–	ns
DRQ Reset From $\phi 2$	t_{DRR}	–	500	–	500	ns
$\overline{IRQ}$ Reset From $\phi 2$	t_{IRR}	–	3	–	3	μs
Address Setup Time	t_{ACR}	180	–	90	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Setup Time	t_{WCR}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Access Time	t_{CDR}	–	395	–	200	ns
Data Bus Hold Time	t_{HR}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

Read Timing

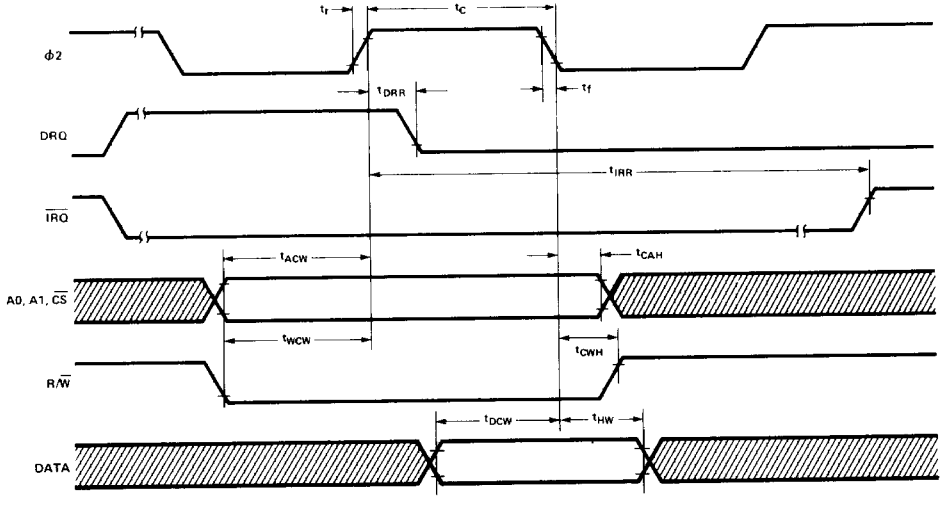


Write Cycle (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	6591		6591A		Units
		Min.	Max.	Min.	Max.	
$\phi 2$ Pulse Width	t_C	470	–	235	–	ns
DRQ Reset From $\phi 2$	t_{DRR}	–	500	–	500	ns
$\overline{IRQ}$ Reset From $\phi 2$	t_{IRR}	–	3	–	3	µs
Address Setup Time	t_{ACW}	180	–	90	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Setup Time	t_{WCW}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Setup Time	t_{DCW}	300	–	150	–	ns
Data Bus Hold Time	t_{HW}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

Write Timing



Package Availability

40 Pin Ceramic
40 Pin Cerdip
40 Pin Plastic

Ordering Information

Part Number	Package	MPU Clock Rate
SYC6591	Ceramic	1MHz
SYD6591	Cerdip	1MHz
SYP6591	Plastic	1MHz
SYC6591A	Ceramic	2MHz
SYD6591A	Cerdip	2MHz
SYP6591A	Plastic	2MHz