MN379

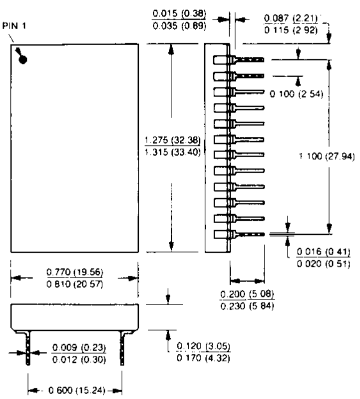
FLASH-CONVERTER COMPATIBLE T/H AMPLIFIER

MICRO NETWORKS

FEATURES

- **Designed to Directly Drive Flash Converters**
- **2psec Maximum Aperture Jitter**
- **Capacitive Loads to 500pF**
- **30nsec Max Acquisition Time (1V Step to ±0.1%)**
- **15nsec Max Settling Time**
- **±300V/μsec Min Slew Rate**
- **100MHz Bandwidth**
- **TTL or ECL Compatible**
- **24-Pin DIP**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD 1772 Qualified Facility**

24 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN379 is an extremely high-speed track-hold (T/H) amplifier designed to overcome the bandwidth and loading problems associated with many 6-9 bit, high-throughput, flash-type A/D converters. The relatively high aperture uncertainty (jitter) of many higher-resolution flash converters results in correspondingly large accuracy and linearity errors when digitizing high-slew-rate (wide-bandwidth) signals. The result is a reduction in effective-bit resolution. MN379 overcomes this problem with its outstanding 2psec maximum aperture jitter. In such aperture-reducing applications, MN379 can result in a 10 times improvement in the ability to digitize rapidly slewing signals while its 25MHz throughput causes no reduction in overall sampling rate.

An additional problem associated with higher-resolution flash converters is the high capacitive input impedance that often characterizes these devices. MN379 is designed to be unconditionally stable with capacitive loads up to 500pF, and its ability to supply instantaneous output currents up to ±100mA makes its acquisition, settling and bandwidth characteristics relatively unaffected by load.

MN379 has an input/output voltage range of ±2.5V. Its compensated open-loop design architecture gives it a minimum gain of +0.92 and a pedestal guaranteed not to exceed ±20mV. The outstanding 2psec aperture jitter is achieved using a high-speed diode-bridge switching scheme. The track-hold digital input controlling the bridge can be referenced to an external voltage for CMOS or ECL compatibility. An internal reference is supplied for TTL compatibility.

MN379 is packaged in a standard, 24-pin ceramic dual-in-line. Power supply requirements are ±15V and maximum power consumption is 2 Watts. Standard product is fully specified for 0°C to +70°C (case) operation and for military/aerospace applications, is available fully screened to MIL-H-38534 (MN379H/B CH).

MICRO NETWORKS
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MN379 FLASH-CONVERTER COMPATIBLE T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C (case)
Specified Temperature Range:	
MN379	0°C to +70°C (case)
MN379H, MN379H/B (Note 1)	−55°C to +125°C (case)
Storage Temperature Range	−65°C to +150°C
+15V Supply(+Vcc, Pin 23)	−0.5 to +18 Volts
−15V Supply (−Vcc, Pin 12)	+0.5 to −18 Volts
Analog Input Voltage (Pin 5)	±5 Volts
Digital Input Voltage (Pins 2 or 3 to ground)	±15 Volts
Differential Digital Input Voltage (Pin 2 to Pin 3)	±5 Volts
Output Current (Note 2)	±35mA

ORDERING INFORMATION

PART NUMBER ——— **MN379H/B CH**

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

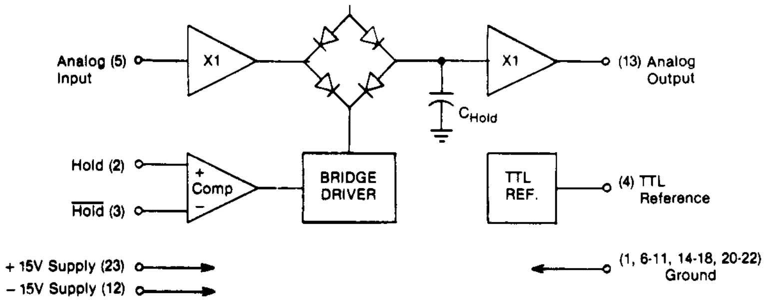
SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V, Z_{Load} = 500Ω // 15pF unless otherwise indicated)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	±2.5			Volts
Input Impedance		10 // 5		kΩ // pF
Output Current (Note 2)	±25			mA
Output Impedance		10		Ω
Maximum Capacitive Load	500			pF
DIGITAL INPUTS (Note 3)				
Digital Input Threshold (Pin 2 to Pin 3)	−100		+100	mV
Digital Input Operating Range (Pins 2 and 3 to Ground)	−5.5		+5.5	Volts
Logic Levels (Pin 2 or 3 tied to Pin 4): Logic "1" Logic "0"	+2		+5.5 +0.8	Volts Volts
Logic Currents: Logic "1" Logic "0"			+10 −0.25	μA mA
TTL Reference (Pin 4) Output Voltage	+1.1	+1.25	+1.4	Volts
TTL Reference (Pin 4) Output Impedance		560		Ω
TRANSFER CHARACTERISTICS				
Gain Error: Initial (+25°C) Drift (Note 4)	+0.92	+0.96 ±20	 ±50	V/V ppm/°C
Linearity Error (Full Temperature Range) (Notes 4, 5)		±0.05	±0.1	%FSR
Offset Voltage (Track Mode): Initial (+25°C) Drift (Note 4)		±5 ±100	±10 ±200	mV μV/°C
Pedestal (Note 6): Initial (+25°C, V_{in} = 0V) Drift (Note 4) Variation with V_{in}		±10 ±100 −8	±20 ±200	mV μV/°C mV/V
DYNAMIC CHARACTERISTICS				
Acquisition Time: 5V Step to ±1% (±50mV) 5V Step to ±0.1% (±5mV) 1V Step to ±1% (±10mV) 1V Step to ±0.1% (±1mV)		25 35 15 25	30 40 20 30	nsec nsec nsec nsec
Track-to-Hold Transient: Height (Peak-to-Peak) Settling Time (to ±5mV)		60 10	 15	mV nsec
Aperture Delay Time		5	8	nsec
Aperture Jitter		1	2	psec (rms)
Slew Rate	±300	±400		V/μsec
Small Signal Bandwidth (1Vp-p)		100		MHz
Large Signal Bandwidth (5Vp-p)		25		MHz
Feedthrough Attenuation (@10MHz)	60			dB
Droop Rate: +25°C Over Temperature (Note 4)		±0.5 Doubles Every 10°C	±5	mV/μsec
POWER SUPPLIES REQUIREMENTS				
Power Supply Range	±14.25	±15	±15.75	Volts
Power Supply Rejection		±12	±25	μV/V
Current Drain: +15V Supply −15V Supply		+55 −50	+70 −65	mA mA
Power Consumption		1575	2025	mW

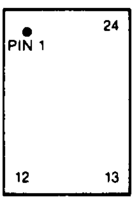
SPECIFICATION NOTES:

1. The MN379 has an approximate 50°C rise of case temperature over still, ambient air temperature.
2. Under normal operating conditions, continuous output current should not exceed ±35mA. The MN379 can withstand a continuous short to ground for approximately 10 seconds. Shorts to either supply will result in destruction.
3. The MN379's Hold and $\overline{\text{Hold}}$ inputs are essentially the direct inputs of a comparator, and the Digital Input Threshold Voltage is effectively the comparator offset. Tying either Pin 2 or Pin 3 to Pin 4 (TTL Reference) will make the other pin TTL compatible. For Pin 2: "0" = Track, "1" = Hold. For Pin 3: "1" = Track, "0" = Hold. Tying either Pin 2 or Pin 3 to other reference voltages can make the MN379 compatible with any logic family.
4. Listed specifications apply over the 0°C to +70°C (case) temperature range for the MN379 and over the −55°C to +125°C (case) temperature range for the MN379H and MN379H/B.
5. Linearity Error is expressed as a percentage of the Full Scale Range (peak-to-peak) of the input/output signal. In an 8-bit system, ½LSB is equivalent to 0.19%FSR. In a 9-bit system, ½LSB is equivalent to ±0.1% FSR.
6. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For the MN379, pedestal amplitude varies linearly with input signal amplitude. The pedestal becomes more negative as the input signal becomes more positive.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Ground	24	Ground
2	Hold Command (Note)	23	+15V Supply (+V_{CC})
3	$\overline{\text{Hold}}$ Command (Note)	22	Ground
4	TTL Reference	21	Ground
5	Analog Input	20	Ground
6	Ground	19	N/C
7	Ground	18	Ground
8	Ground	17	Ground
9	Ground	16	Ground
10	Ground	15	Ground
11	Ground	14	Ground
12	−15V Supply (−V_{CC})	13	Analog Output

Note: Pin 2: "0" = Track, "1" = Hold
Pin 3: "1" = Track, "0" = Hold

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—The large switching currents produced by MN379's diode-bridge switching circuitry make it mandatory to provide a good ground and clean supplies to the device in order to achieve specified speed and accuracy performance. The unit has 16 ground pins (pins 1, 6-11, 14-18, 20-22 and 24). They should all be tied together as close to the unit as possible and all connected to system analog ground, preferably through a large low-impedance, analog ground plane beneath the package.

If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01µF ceramic capacitors interconnecting them as close to the package as possible.

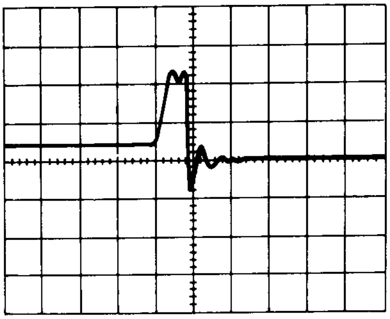
Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1µF tantalum capacitors in parallel with 0.01µF ceramic capacitors are the most effective combination.

Coupling between analog inputs and digital control signals should be minimized to avoid noise pickup. Care should be taken to avoid long analog runs or analog runs in parallel with digital lines.

TRACK-HOLD COMMAND—A logic "0" applied to pin 2 (or a logic "1" applied to pin 3) drives MN379 into the track (sample) mode. In this mode, the device performs as a unity-gain amplifier (follower), and its output follows (tracks) its input. A logic "1" applied to pin 2 (or a logic "0" applied to pin 3) drives MN379 into the hold mode, holding the output constant at the level present when the hold command was given.

MN379's Hold and $\overline{\text{Hold}}$ inputs are essentially the direct inputs of a comparator, and the specification for Digital Input Threshold Voltage is effectively the comparator offset. Tying either pin 2 or pin 3 to pin 4 (TTL Reference) will make the other pin TTL compatible. If, for example, pin 3 ($\overline{\text{Hold}}$) is tied to pin 4 (TTL Reference), a TTL logic "1" (+2.0V minimum) applied to pin 2 will drive MN379 into the hold mode.

Tying either pin 2 or pin 3 to other reference voltages can make MN379 compatible with any logic family. Tying either to −1.3 volts, for example, will make the other ECL compatible.



Scale: Vertical 20mV/div
Horizontal 10nsec/div
Glitch Amplitude: 40mV
Glitch Area: 240mV-nsec

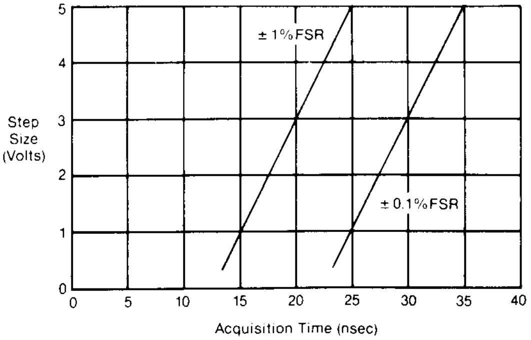
MN379 Typical Track-to-Hold Transient

MN379 ACQUISITION TIME—MN379 acquisition time for any step size settling to ±1%FSR (±50mV) or ±0.1%FSR (±5mV) can be read from the plot below or calculated using the following guidelines. Acquisition time basically consists of the following 4 components:

1) 5nsec gate delay
2) 3nsec output amplifier delay
3) 2.5nsec/volt slew rate
4) 4nsec for settling to ±1%FSR or 14nsec for settling to ±0.1%FSR

The 8nsec total delay for the gate and output amplifier circuits is constant. The total time required for slewing obviously varies as a function of step size, and the settling times are constant independent of step size. Therefore, as demonstrated below, the acquisition time is easily calculated for any step size.

		Typ	Max
5V step to ±1%	(8 + 12.5 + 4)nsec =	25nsec	30nsec
5V step to ±0.1%	(8 + 12.5 + 14)nsec =	35nsec	40nsec
1V step to ±1%	(8 + 2.5 + 4)nsec =	15nsec	20nsec
1V step to ±0.1%	(8 + 2.5 + 14)nsec =	25nsec	30nsec



MN379 Acquisition Time vs. Step Size

DRIVING CAPACITIVE LOADS—As stated earlier, MN379 is designed to directly drive most 6-9 bit flash converters. Such converters often have highly capacitive input impedances, and certain precautions must be taken to optimize MN379 performance with capacitive loads at the megahertz frequencies the device is designed to handle. In particular, the series inductance of the wire or pc card run connecting the output of MN379 to its capacitive load is no longer insignificant. In order to obtain the quickest settling at the load in response to a driving function at the T/H output, it will be necessary to add a series resistor such that the resulting RLC circuit is critically damped. Actually, a slightly underdamped response will settle somewhat faster, but the improvement is not significant. The value of the damping resistor will depend upon the length of wire and the load capacitance.

Critical damping occurs in a series RLC circuit when the resonant radian frequency (ω_0) equals the exponential damping coefficient (α):

Since $\omega_0 = 1/\sqrt{LC}$
and $\alpha = R/2L$
it follows that $R = 2\sqrt{L/C}$

where R is the required value of series resistance, L is the wire inductance and C is the load capacitance. The 10Ω output resistance of the T/H should be subtracted from the calculated value of R since it is effectively in series with the load. In making calculations, an inductance of 23nHy/in. can be assumed for straight, solid wire of AWG 20 to 28, or P.C. runs of 100 to 600 mil² cross-sectional area. This value should also serve as a good starting point for experimentation if other shapes or wire sizes are used. Bear in mind that critical damping only guarantees best settling for a given combination of L and C. There will still be practical limits on the values these can assume if settling is to be accomplished in a reasonable time.

The voltage at the load capacitor will be of the form

$$v(t) = A\{1 - (\alpha t + 1)e^{-\alpha t}\}$$

in response to a step of amplitude A at the T/H output. For settling to ±0.1%, v(t) = 0.999A and, from the equation above, $\alpha t = 9.23$. Since $\alpha = \omega_0 = 1/\sqrt{LC}$, it follows that settling to ±0.1% of the step size occurs at $t = 9.23\sqrt{LC}$.

As an example, assume $C_{LOAD} = 200pF$ and that it is 2.2 inches from the T/H output. This corresponds to a wire inductance of L = 23nHy/in. x 2.2in. = 51nHy. For critical damping, $R = 2\sqrt{L/C} = 32\Omega$. Subtracting 10Ω for the T/H output yields a final value of 22Ω. This resistor should be a carbon or other non-inductive type, and its length will count as part of the inductance to be damped. With C and L as above, the settling time to ±0.1% will be $t = 9.23\sqrt{LC} = 30nsec$.

The actual settling time in any given situation will be somewhat longer than predicted above due to the effects of the settling time of the T/H itself. A very good approximation of the overall settling time can be obtained by assuming the two components add as the square root of the sum of their squares. In the above example, assuming 30nsec settling time for the T/H to ±0.1%, this would mean $\sqrt{30^2 + 30^2}$, or about 42nsec total settling from the time a step is applied to the input of the T/H to the time the voltage seen by the A/D settles to ±0.1% of its final value.

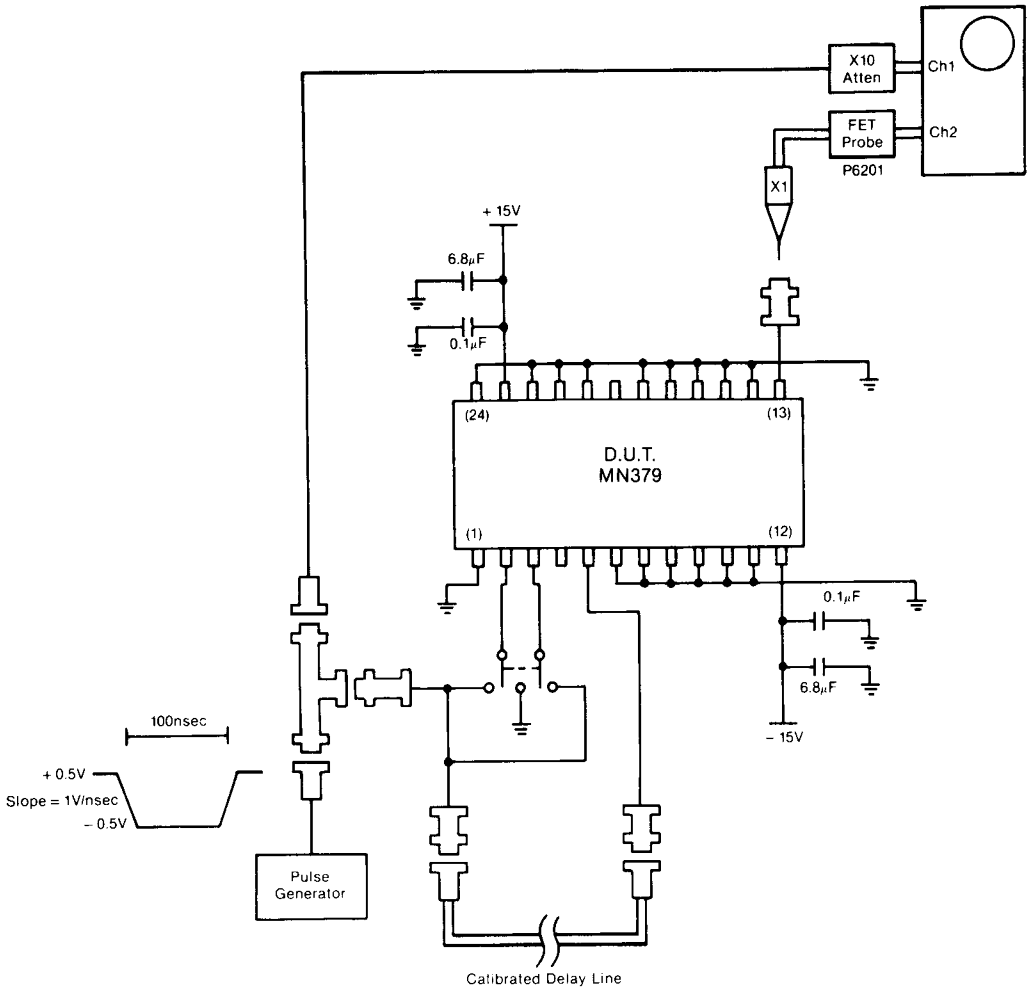
HEAT SINKING — "H" versions of MN379 are fully specified for −55°C to +125°C (case temperature) operation. Because of the device's high internal power dissipation, heatsinking precautions may be necessary to maintain junction temperatures below +150°C.

MN379 typically dissipates 1575mW (2025mW maximum). The device has a junction-to-ambient thermal resistance (θ_{JA}) of 34°C/watt. Therefore, with no heatsinking, MN379's junction-to-ambient temperature differential is typically 53.5°C. Following the +150°C maximum junction-temperature restriction, the calculated temperature differential dictates that one not operate MN379 in still, ambient air above +96.5°C. Note, however, that the unit has a relatively low 7.5°C/watt junction-to-case thermal resistance (θ_{JC}) that makes the device relatively easy to heatsink.

TESTING APERTURE JITTER—The following method is designed to measure the aperture jitter of the MN379 but, with appropriate modification of the D.U.T. socket pinout, may be used to measure any high-speed track-hold amplifier.

Please refer to the diagram labeled 'Aperture Jitter Test Set-up' for the following procedure. A pulse generator capable of generating pulses with rising and falling edges with slopes on the order of 1 Volt/ns is needed as is a sampling scope and FET probe. The pulse train is used initially to drive the Hold or $\overline{\text{Hold}}$ input of the MN379 (depending upon whether rising edge or falling edge jitter is to be measured). Since the control inputs to the MN379 are fully differential, the unused input is simply connected to ground for a reference and a symmetrical-around-ground input signal is used. The indicated signal levels were chosen so as not to overload the FET probe when used in the X1 mode. Probe noise is too high to get meaningful readings if a X10 attenuator is used. The drive signal is sent to both the sampling scope, to set levels and for triggering, and to a "calibrated delay line". The delay line compensates for aperture delay time and consists of a length of coax selected so that the aperture time (switch opening) of the track and hold occurs at the fastest rising (zero crossing) point of the input waveform. Use of this form of delay ensures no added jitter. The length of the delay line may vary from a few inches to several feet.

Once the delay line has been adjusted properly (this may be confirmed by noting that the "held' voltage is near zero volts), the FET probe is used to measure the input-signal slew rate directly at the D.U.T. input pin (pin 5). This slew rate will most likely be different for the rising vs falling edge so both should be measured. The FET probe is then returned to the Analog Output (pin 13), and the sampling scope is set to view a portion of the held waveform well past the track-to-hold settling transient. A tangential noise measurement is made by observing the width of the noise band on the scope (mVp-p). This reading is then divided by six to get the approximate rms value of the noise. This number, when divided by the slope of the input signal, will give the aperture jitter. If the units used are mV and volts/ns the calculated jitter will be in picoseconds (rms). A slightly more accurate measurement may be obtained by subtracting the contribution of system noise to overall output noise. This may be measured by observing the output on the oscilloscope while the D.U.T. is in the track mode.



Aperture Jitter Test Setup