TDC1049

High-Speed A/D Converter

9-Bit, 30Msps

The TDC1049 is a flash (full-parallel) analog-to-digital converter capable of converting analog signals with full-power frequency components up to 15MHz into 9-bit words at rates up to 30Msps (Megasamples Per Second). A sample-and-hold circuit is not required. All digital inputs and outputs are differential ECL.

The TDC1049 consists of 512 latching comparators, encoding logic and an output register. A differential convert signal controls the conversion operation. The outputs can be connected to give either true or inverted binary or offset two's complement formats.

Features

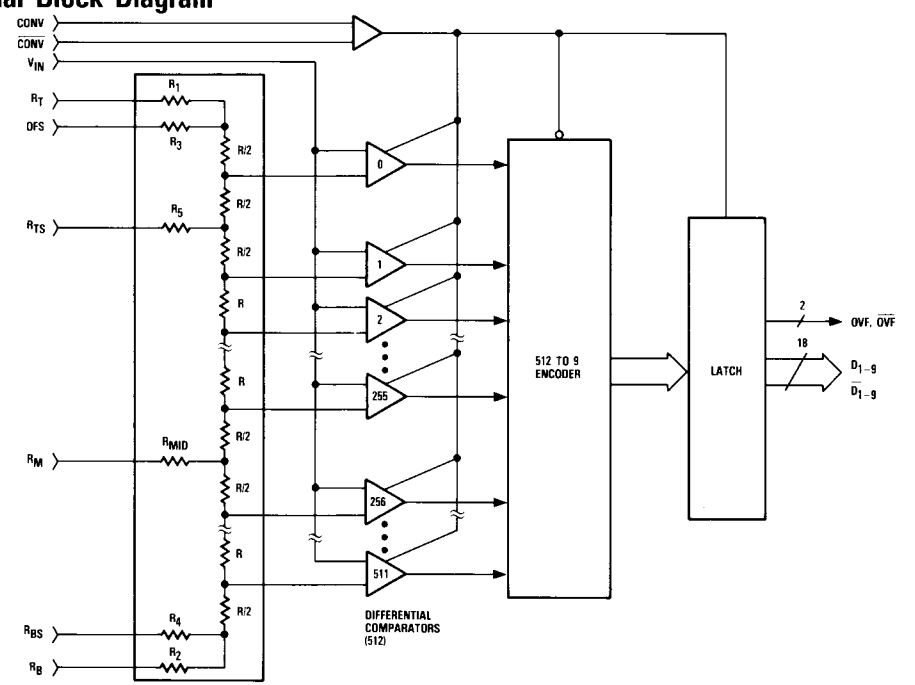
- 30Msps Conversion Rate, 15MHz Analog Bandwidth
- 9-Bit Resolution And Linearity
- Sample-And-Hold Circuit Not Required
- Differential Phase 0.5 Degrees
- Differential Gain 1.0%
- Overflow Flag
- Single −5.2V Power Supply
- Differential ECL Outputs
- Available In A 64 Pin DIP, 68 Contact LCC And 68 Pin Ceramic Pin Grid Array
- Available Per Standard Military Drawing

A

Applications

- Video Data Conversion
- Radar Data Conversion
- High-Speed Data Acquisition

Functional Block Diagram



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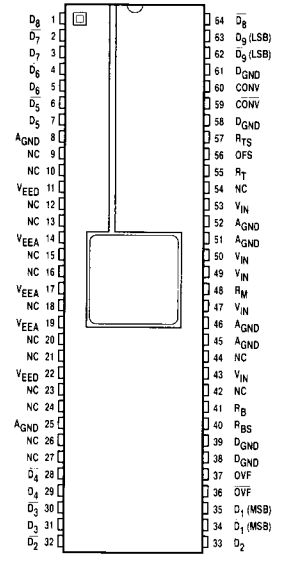
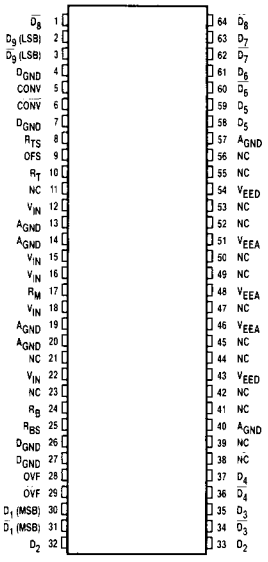
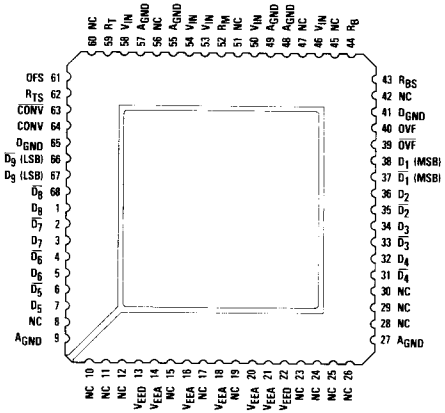
Pin Assignments



64 Pin DIP – J0 Package



64 Pin DIP – J3 Package

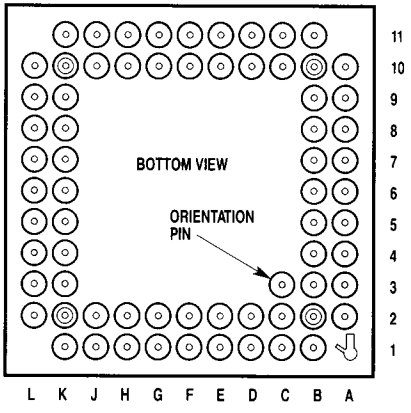


68 Contact LCC – C1 Package

Pin Assignments

68 Pin Ceramic Pin Grid Array, G8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	NC	B9	V_{EEA}	F10	D_8	K4	A_{GND}
A3	V_{EED}	B10	NC	F11	$\overline{D_7}$	K5	V_{IN}
A4	NC	B11	A_{GND}	G1	D_1	K6	V_{IN}
A5	NC	C1	NC	G2	$\overline{D_1}$	K7	NC
A6	NC	C2	NC	G10	D_9	K8	A_{GND}
A7	NC	C10	D_5	G11	$\overline{D_8}$	K9	V_{IN}
A8	NC	C11	NC	H1	$\overline{OVF}$	K10	R_{TS}
A9	NC	D1	D_4	H2	OVF	K11	$\overline{CONV}$
A10	V_{EED}	D2	$\overline{D_4}$	H10	D_{GND}	L2	NC
B1	NC	D10	D_6	H11	D_9	L3	NC
B2	A_{GND}	D11	$\overline{D_5}$	J1	NC	L4	A_{GND}
B3	V_{EEA}	E1	D_3	J2	D_{GND}	L5	R_M
B4	V_{EEA}	E2	$\overline{D_3}$	J10	CONV	L6	NC
B5	V_{EEA}	E10	D_7	J11	D_{GND}	L7	V_{IN}
B6	V_{EEA}	E11	$\overline{D_6}$	K1	R_{BS}	L8	A_{GND}
B7	V_{EEA}	F1	D_2	K2	R_B	L9	R_T
B8	NC	F2	$\overline{D_2}$	K3	V_{IN}	L10	OVS



Functional Description

General Information

The TDC1049 has three functional sections: a comparator array, encoding logic and output register. The comparator array compares the input signal with 512 reference voltages to produce an N-of-512 code or "thermometer" code. The comparators referenced to voltages less than the input signal will be on and those referenced to voltages greater than the input signal will be off. The encoding logic converts the N-of-512 code into 9-bit binary data. The output register holds the output between updates.

Power

For optimum performance, separate analog and digital power, V_{EEA} and V_{EED} should be supplied to the TDC1049. Separate analog and digital power supplies or a common supply with separate analog and digital paths and high-frequency decoupling can be used. The return path for the current drawn from V_{EEA} and V_{EED} is A_{GND} and D_{GND}, respectively. The returns A_{GND} and D_{GND} should also be kept separate and connected together at the power supply terminals. It is recommended that provisions be made on the printed circuit board for shorting jumpers between analog and digital ground as close to the A/D converter as possible. The installation of the jumpers depends upon the printed circuit board layout and overall system performance once the system is in operation. The voltage difference between V_{EEA} and V_{EED} must be less than $\pm 0.1V$. The same voltage difference limit applies to the difference between A_{GND} and D_{GND}. All power and ground inputs to the converter must be connected.

Reference

The TDC1049 converts analog signals in the range $V_{RB} < V_{IN} < V_{RT}$ into digital form. V_{RB} (the voltage applied to R_B) at the bottom of the reference resistor chain, and V_{RT} (the voltage applied to R_T) at the top of the reference resistor chain, should both be between $+0.1V$ and $-2.1V$. Within that range, V_{RT} must be more positive than V_{RB}. The linearity specification is based upon a 2.0V difference between V_{RT} and V_{RB}. The nominal voltages are $V_{RT} = 0.0V$ and $V_{RB} = -2.0V$. To avoid damage to the converter, the voltage across V_{RT} and V_{RB} must not exceed 2.2V. A decoupling capacitor is recommended between R_B and A_{GND}. Noise introduced at this point, as well as the other reference inputs (R_T, R_{TS}, R_M, R_{BS}, OFS), may result in encoding errors.

A midpoint tap, R_M, allows the converter to be adjusted for optimum integral linearity. It can also be used to achieve a nonlinear transfer function, but adjustment of R_M is not required to meet 9-bit linearity. If this node is driven by external circuitry, it should be driven from a low-impedance source; if not used, it must be left open.

Parasitic resistances, R1 and R2, introduce offset errors at the top and bottom of the reference resistor chain. Sense points, R_{TS}, R_{BS} and OFS, may be used to reduce the effect of these offset errors. Overflow Sense (OFS) may be used to reduce the effect of the offset at the overflow (most positive) comparator whenever the Overflow (OVF, $\overline{OVF}$) flags are used. Sense points are not required for 9-bit linearity and, if not used, they must be left open.

Convert

The TDC1049 requires a differential ECL clock (CONV and $\overline{CONV}$) signal. The conversion occurs (the comparators are latched) within t_{STO} (Sampling Time Offset) of the rising edge of CONV. The 512 to 9 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output register on the next rising edge of CONV. Data for sample N is available at the output t_D (Output Delay Time) after the rising edge of sample N+1.

Analog Input

The TDC1049 uses latching comparators which are connected to the analog inputs V_{IN}. For optimal performance, the source impedance of the driver amplifier should be less than 25Ω. The input signal will not damage the TDC1049 if it remains within the range of V_{EEA} to $+0.5V$. If the input signal is between the V_{RT} and V_{RB}, the output will be a binary number between 0 and 511 inclusive. All five analog inputs must be connected.

Outputs

The outputs of the TDC1049 are differential ECL. The recommended pull-down resistance is 500Ω to $-2V$, or a 220/330Ω termination between D_{GND} and V_{EED}. The OVF signal indicates that the analog input has exceeded the threshold of the most positive comparator. Data is held valid at the output register for at least t_{HO} (Output Hold Time) after the rising edge of CONV. New data becomes valid t_D after the rising edge of CONV.

No Connects

There are several pins labeled NC (No Connect). These pins are not connected internally and may be either left open or connected to analog ground to aid heat transfer from the package and to reduce electrical noise.

Package Interconnections

Signal Name	Function	Value	J0 Package Pins	J3 Package Pins	C1 Package Pins	G8 Package Pins
V_{EEA}	Analog Supply Voltage	−5.2V	46, 48, 51	14, 17, 19	14, 16, 18, 20, 21	B9, B7, B6, B5, B4
V_{EED}	Digital Supply Voltage	−5.2V	43, 54	11, 22	13, 22	A3, A10
D_{GND}	Digital Ground	0.0V	4, 7, 26, 27	38, 39, 58, 61	41, 65	J2, J11, H10
A_{GND}	Analog Ground	0.0V	13, 14, 19, 20, 40, 57	8, 25, 45, 46, 51, 52	9, 27, 48, 49, 55, 57	B2, K4, L4, K8, L8, B11
R_T	Reference Resistor, Top	0.0V	10	55	59	L9
R_{TS}	Reference Resistor, Top Sense	0.0V	8	57	62	K10
R_B	Reference Resistor, Bottom	−2.0V	24	41	44	K2
R_{BS}	Reference Resistor, Bottom Sense	−2.0V	25	40	43	K1
R_M	Reference Resistor, Midpoint	−1.0V	17	48	52	L5
OFS	Overflow Sense	0.0V	9	56	61	L10
CONV	Convert	ECL	5	60	64	J10
$\overline{CONV}$	Convert, Complement	ECL	6	59	63	K11
V_{IN}	Analog Signal Input	0V to −2V	12, 15, 16, 18, 22	43, 47, 49, 50, 53	46, 50, 53, 54, 58	K3, K5, K6, L7, K9
D_1 MSB	Most Significant Bit	ECL	30	35	38	G1
$\overline{D_1}$ MSB	Most Significant Bit Complement	ECL	31	34	37	G2
D_2		ECL	32	33	36	F1
$\overline{D_2}$		ECL	33	32	35	F2
D_3		ECL	34	31	34	E1
$\overline{D_3}$		ECL	35	30	33	E2
D_4		ECL	36	29	32	D1
$\overline{D_4}$		ECL	37	28	31	D2
D_5		ECL	58	7	7	C10
$\overline{D_5}$		ECL	59	6	6	D11
D_6		ECL	60	5	5	D10
$\overline{D_6}$		ECL	61	4	4	E11
D_7		ECL	62	3	3	E10
$\overline{D_7}$		ECL	63	2	2	F11
D_8		ECL	64	1	1	F10
$\overline{D_8}$		ECL	1	64	68	G11
D_9 LSB	Least Significant Bit	ECL	2	63	67	G10
$\overline{D_9}$ LSB	Least Significant Bit Complement	ECL	3	62	66	H11
OVF	Overflow Output	ECL	28	37	40	H2
$\overline{OVF}$	Overflow Output Complement	ECL	29	36	39	H1
NC	No Connect	Open	11, 21, 23, 38, 39, 41, 42, 44, 45, 47, 49, 50, 52, 53, 55, 56	9, 10, 12, 13, 15, 16, 18, 20, 21, 23, 24, 26, 27, 42, 44, 54	8, 10, 11, 12, 15, 17, 19, 23, 24, 25, 26, 28, 29, 30, 42, 45, 47, 51, 56, 60	B1, C2, C1, J1, L2, L3, L6, K7, C11, B10, A9, B8, A8, A7, A6, A5, B4, A4, A2

Output Coding Table [1]

V_{IN}	OVF	D_1 MSB ... D_9 LSB
+0.0039V	1	000000000
0.0000V	0	000000000
−0.0039V	0	000000001
•	•	•
•	•	•
•	•	•
−0.9980V	0	011111111
−1.0020V	0	100000000
−1.0059V	0	100000001
•	•	•
•	•	•
•	•	•
−1.9961V	0	111111110
−2.0000V	0	111111111

Note: 1. Voltages are code midpoints.

Figure 1. Timing Diagram

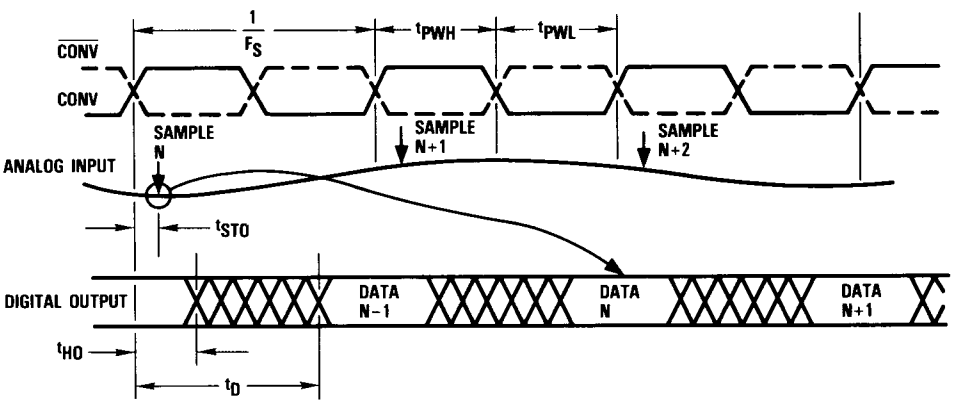
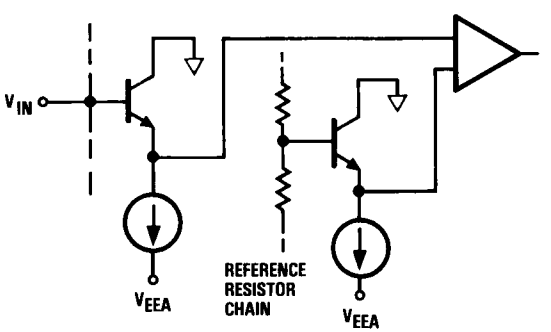
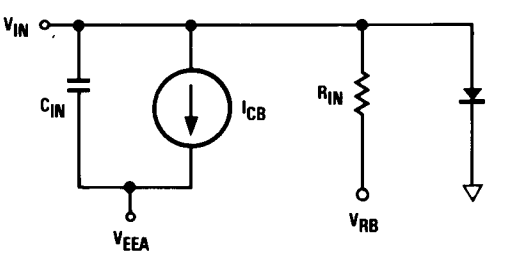


Figure 2. Simplified Analog Input Equivalent Circuits





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

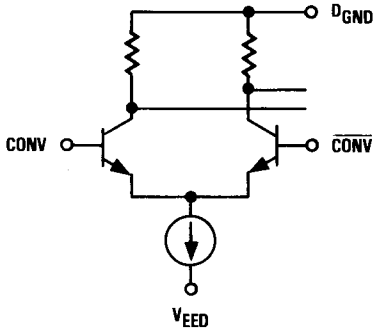


Figure 4. Output Circuits

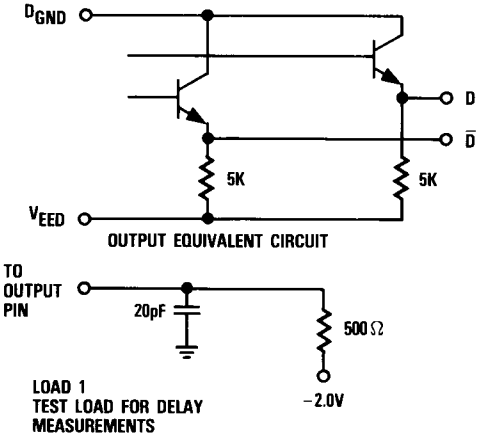
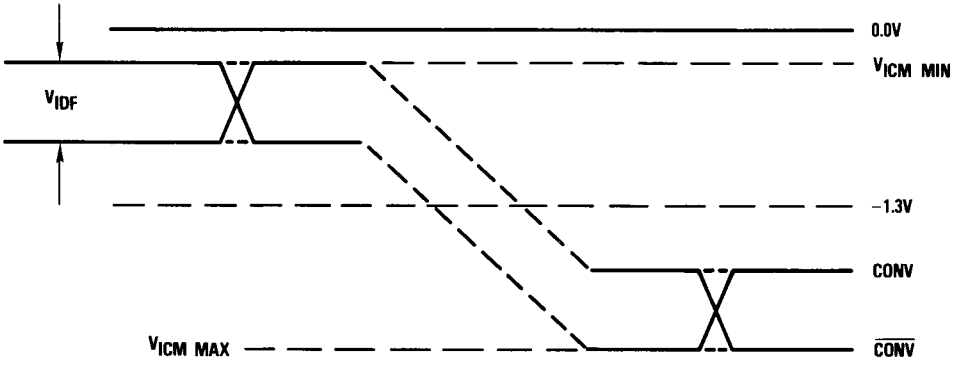


Figure 5. CONVert, $\overline{CONV}$ert Switching Levels



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND}) ..... +0.5 to −7.0V
V_{EEA} (measured to A_{GND}) ..... +0.5 to −7.0V
A_{GND} (measured to D_{GND}) ..... +1.0 to −1.0V
V_{EEA} (measured to V_{EED}) ..... +0.5 to −0.5V

Input Voltages [2]

CONV, $\overline{CONV}$ (measured to D_{GND}) ..... +0.5 to V_{EE}
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND}) ..... +0.5 to V_{EE}
V_{RT} (measured to V_{RB}) ..... +2.5 to −2.5V

Output

Short-circuit duration (single output in HIGH state to ground) ..... Infinite

Temperature

Operating, case ..... −60 to +140°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{EED}	Digital Supply Voltage (measured to D_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential	−0.1	0.0	+0.1	−0.1	0.0	+0.1	V
t_{PWL}	CONV Pulse Width, LOW	12			12			ns
t_{PWH}	CONV Pulse Width, HIGH	15			15			ns
V_{ICM}	Input Voltage, Common Mode	−0.5		−2.5	−0.5		−2.5	V
V_{IDF}	Input Voltage, Differential	0.3		1.2	0.3		1.2	V
V_{IN}	Input Voltage Range	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
V_{RT}	Most Positive Reference Input [1]	−0.1	0.0	0.1	−0.1	0.0	+0.1	V
V_{RB}	Most Negative Reference Input [1]	−1.9	−2.0	−2.1	−1.9	−2.0	−2.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	1.8	2.0	2.2	1.8	2.0	2.2	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Note: 1. V_{RT} Must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{EE}	Supply Current	V_{EED}, V_{EEA} = Max					
		T_A = 0°C to 70°C		−950			mA
		T_A = 70°C		−750			mA
		T_C = −55°C to 125°C				−1090	mA
		T_C = 125°C				−750	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom	10	36	10	36	mA
R_{REF}	Total Reference Resistance		56	200	56	200	Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}	16		16		kOhms
C_{IN}	Analog Input Capacitance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		160		160	pF
I_{CB}	Input Constant Bias Current	V_{EEA} = Max, V_{IN} = 0V		500		750	μA
I_I	Input Current, CONV, $\overline{CONV}$	V_{EED} = Max, V_I = −0.7V		150		180	μA
V_{OL}	Output Voltage, Logic LOW [1]	V_{EED} = Nom		−1.6		−1.5	V
V_{OH}	Output Voltage, Logic HIGH [1]	V_{EED} = Nom	−0.95		−1.1		V
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		20		20	pF

Note: 1. Test Load = 500Ω to −2V on each output.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_S	Maximum Conversion Rate	V_{EED}, V_{EEA} = Min	30		30		Msps
t_{STO}	Sampling Time Offset	V_{EED}, V_{EEA} = Min	−2	6	−2	6	ns
t_D	Output Delay [1]	V_{EED}, V_{EEA} = Min		27		27	ns
t_{HO}	Output Hold Time [1]	V_{EED}, V_{EEA} = Min	3		3		ns

Note: 1. Test Load = 500Ω to −2V on each output, C_{LOAD} = 20pF.

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.15		0.20	%
		V_{RT}, V_{RB} = Nom, V_{RM} Adjusted		0.10		0.10	%
E_{LD}	Linearity Error Differential	V_{RT}, V_{RB} = Nom		0.1		0.1	%
Q	Code Size	V_{RT}, V_{RB} = Nom	15	185	15	185	% Nominal
E_{OTS}	Offset Error, Top	V_{IN} = V_{RT}, R_{TS} Connected		±4		±4	mV
E_{OT}	Offset Error, Top	V_{IN} = V_{RT}		30		30	mV
E_{OBS}	Offset Error, Bottom	V_{IN} = V_{RB}, R_{BS} Connected		±4		±4	mV
E_{OB}	Offset Error, Bottom	V_{IN} = V_{RB}		−30		−30	mV
T_{CO}	Offset Error, Temperature Coefficient			20		20	µV/°C
t_{TR}	Transient Response, Full-Scale			20		20	ns
BW	Bandwidth, Full Power Input	±0.9dB Frequency Response	15		15		MHz
SNR	Signal-to-Noise Ratio	30Msps Conversion Rate, 10MHz Bandwidth					
	Peak Signal/RMS Noise	1.25MHz Input	57		57		dB
		5.0MHz Input	53		53		dB
	RMS Signal/RMS Noise	1.25MHz Input	48		48		dB
		5.0MHz Input	44		44		dB
E_{AP}	Aperture Error			50		50	ps
DP	Differential Phase Error	F_S = 4 x NTSC		0.5		0.5	Degree
DG	Differential Gain Error	F_S = 4 x NTSC		1.5		1.5	%

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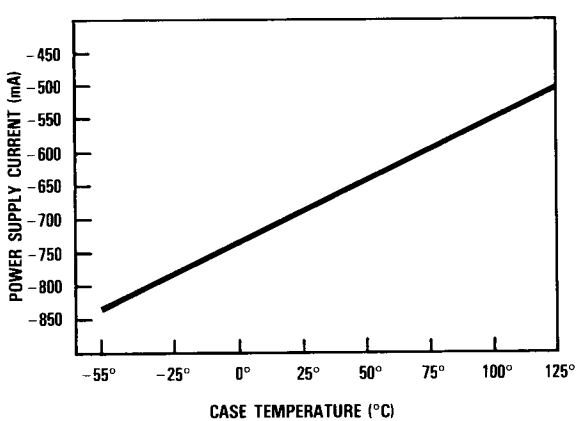
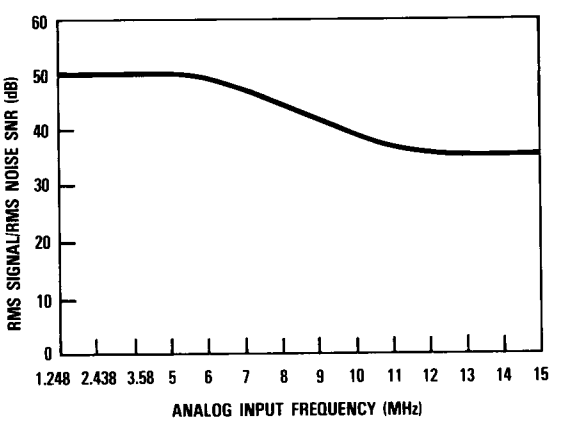
Typical Performance Curves

A. Power Supply Current vs. Temperature



B. SNR vs. Analog Input Frequency



Evaluation Board

The TDC1049E1C1 is a Eurocard-style printed circuit board designed to optimize the performance of, and to aid in the evaluation of, the TDC1049 A/D converter. The board dimensions are 100mm x 160mm with a standard 64 pin double-row DIN male connector installed. A complementary 64 pin double-row DIN female connector is included with the board. The circuitry on the board includes reference voltage generator, wideband video input amplifier, AC-coupled differential clock generators for the A/D converter and output register, and a TDC1112 12-bit D/A converter which may be used in evaluating certain parameters of the TDC1049.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The board is calibrated and tested at the factory and is supplied complete with TDC1049 and TDC1112 installed.

The TDC1049E1C1 is based upon the TDC1049G8C integrated circuit packaged in a 68 pin ceramic pin grid array style package. It supersedes the TDC1049E1C which is based upon the TDC1049J0C 64 pin DIP package.

Power and Ground

Four power supply voltages are required for the operation of the TDC1049E1C: $V_{CC} = +5V$, $V_{EE} = -5.2V$, $V+ = +15V$ and $V- = -15V$. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

Voltage Reference Generator

The TDC1049E1C1 has two voltage reference generator circuits for driving the RT and RB terminal of the TDC1049. The RT generator, U5D-Q1, drive the RT terminal to 0.0V. A variable $-2V$ is supplied to RB from U5C and Q2. The GAIN potentiometer provides $\pm 10\%$ adjustment range on the RB voltage. Diodes D3 through D10 act as clamps which protect the TDC1049 from power-on conditions that might violate absolute maximum ratings and damage the TDC1049.

Video Input Amplifier

The input amplifier of the TDC1049E1C, U4, has been designed to accept a $\pm 0.5V$ input range and translate that signal to the 0V to $-2V$ range of the TDC1049. The output of this amplifier can be monitored at the AOUT SMA connector which is connected to the V_{IN} terminals of the TDC1049 through a 470Ω resistor. The OFFSET potentiometer, R27, gives a $\pm 0.5V$ offset adjustment range to the board.

A/D Converter Inputs

The clock to the TDC1049, CONV, is normally brought onto the board through the SMA connector labeled "CONV." By installing jumper J1, this signal is routed through the edge connector pin B2. A terminating resistor, R41 is installed on the board for terminating a 50Ω clock signal cable. The clock generator accept virtually any waveform and provides differential ECL signals to the TDC1049. The duty-cycle of the TDC1049 clock may be adjusted by installing the 2 kΩ "PW" potentiometer, R42.

The analog signal input to the TDC1049E1C1 is brought onto the board by way of the SMA connector labeled "A_{IN}." A terminating resistor, R17, is included on the board for terminating a 50Ω analog input signal cable.

A/D Converter Data Outputs and D/A Converter Data Inputs

The nine data outputs of the TDC1049 (after registers U2 and U3) are brought to edge connector pins B3 through B11. These pins are located directly across the edge connector from the corresponding data inputs of the TDC1112 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

The clock to the TDC1112, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1112. The clock input to the TDC1112 is also brought to the edge connector pin B24. Resistors, R7 and R8, provide a Thevenin equivalent 130Ω termination for the CONV signal. R5 and R6 bias the $\overline{\text{CONV}}$ input to the TDC1112 near the ECL threshold level.

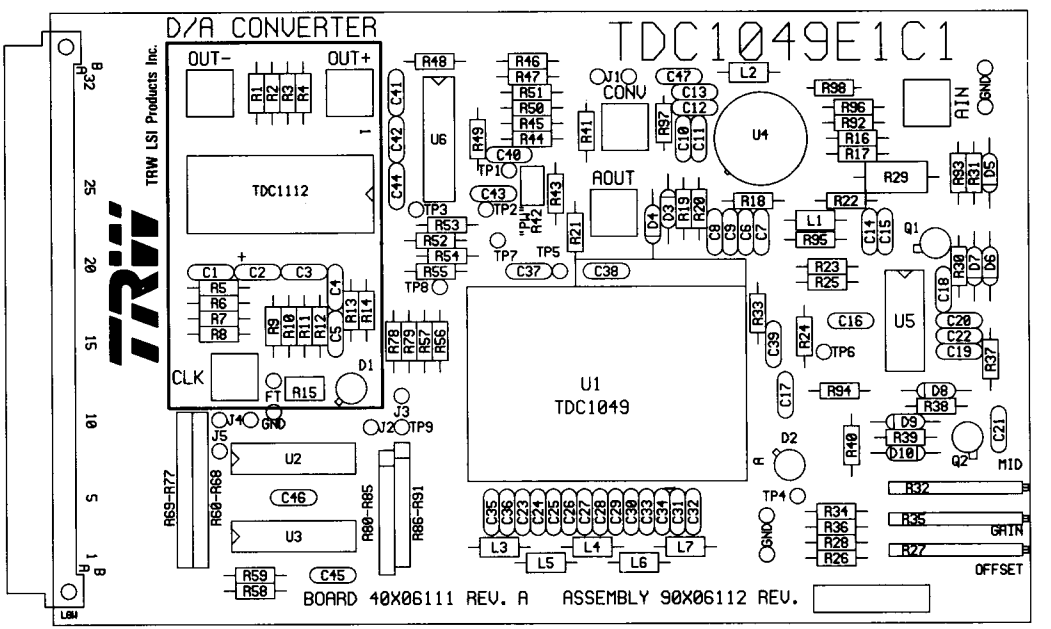
D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT– as well as edge connector pins B27 and B26. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

Potentiometer R11 is used to adjust the reference voltage to the TDC1112. This voltage is adjusted to –1.0V as part of the factory test and calibration procedure.

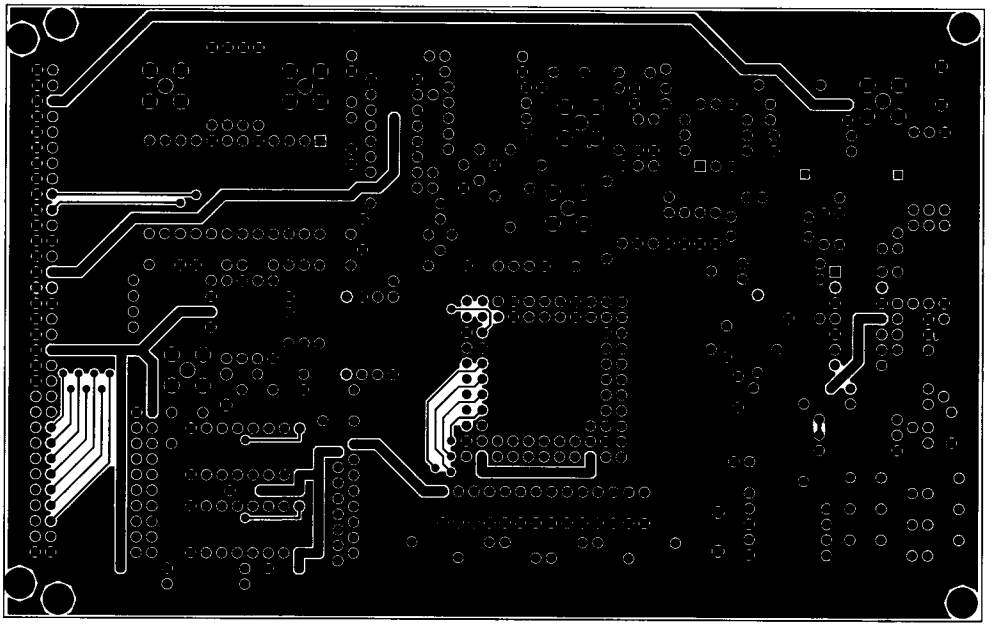
Placing a jumper in the location labeled "FT" will put the TDC1112 into feedthrough (unclocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1112 reconstruction.

A

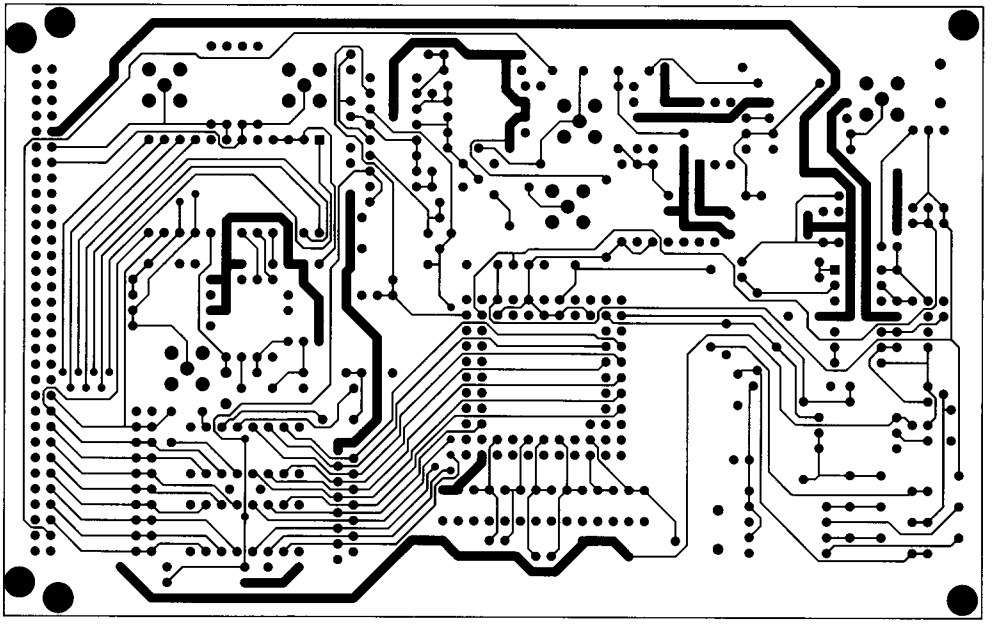
TDC1049E1C Silkscreen Layout



TDC1049E1C Component Side Layout



TDC1049E1C Circuit Side Layout



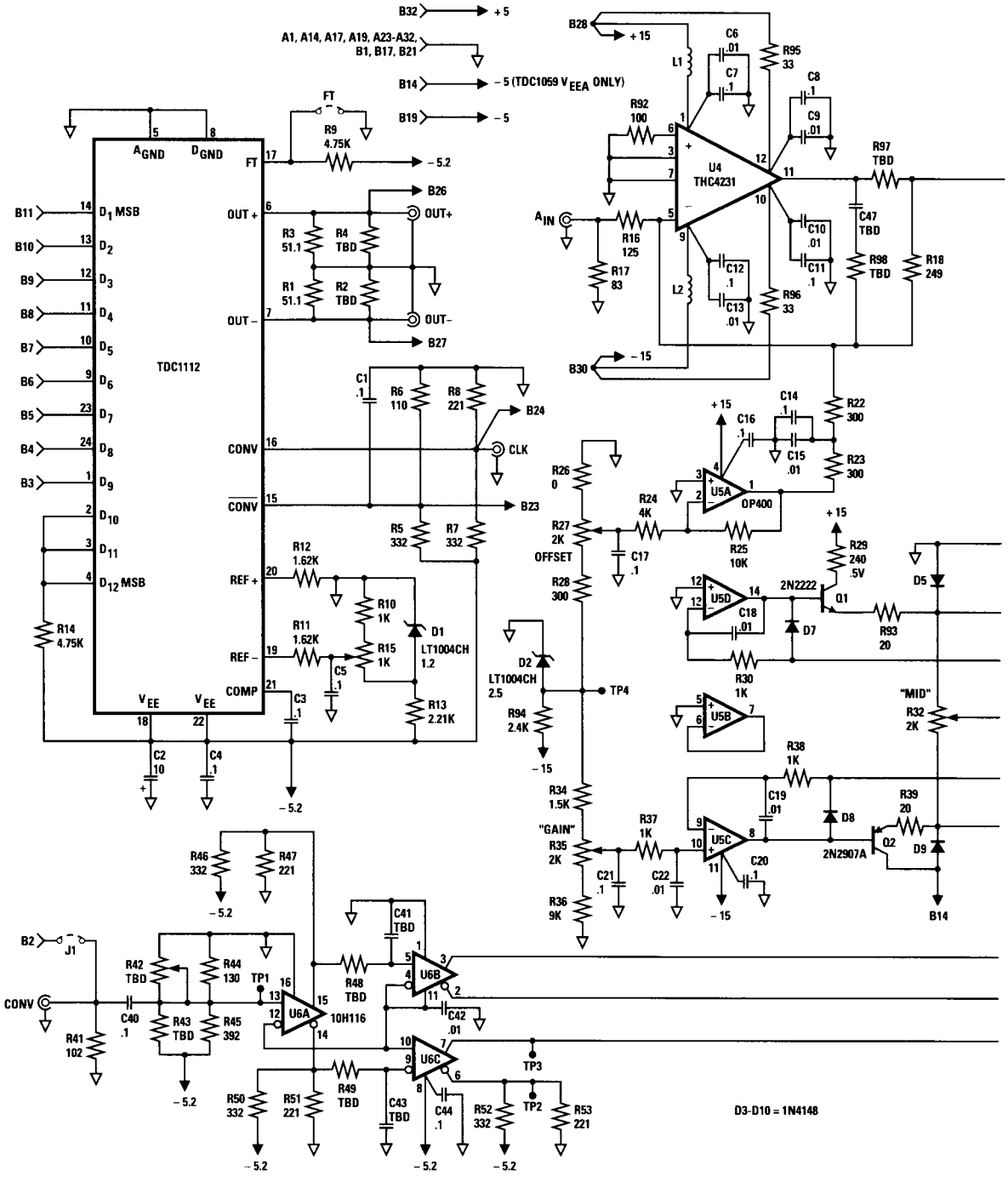
TDC1049E1C Eurocard Edge Connector Pinout

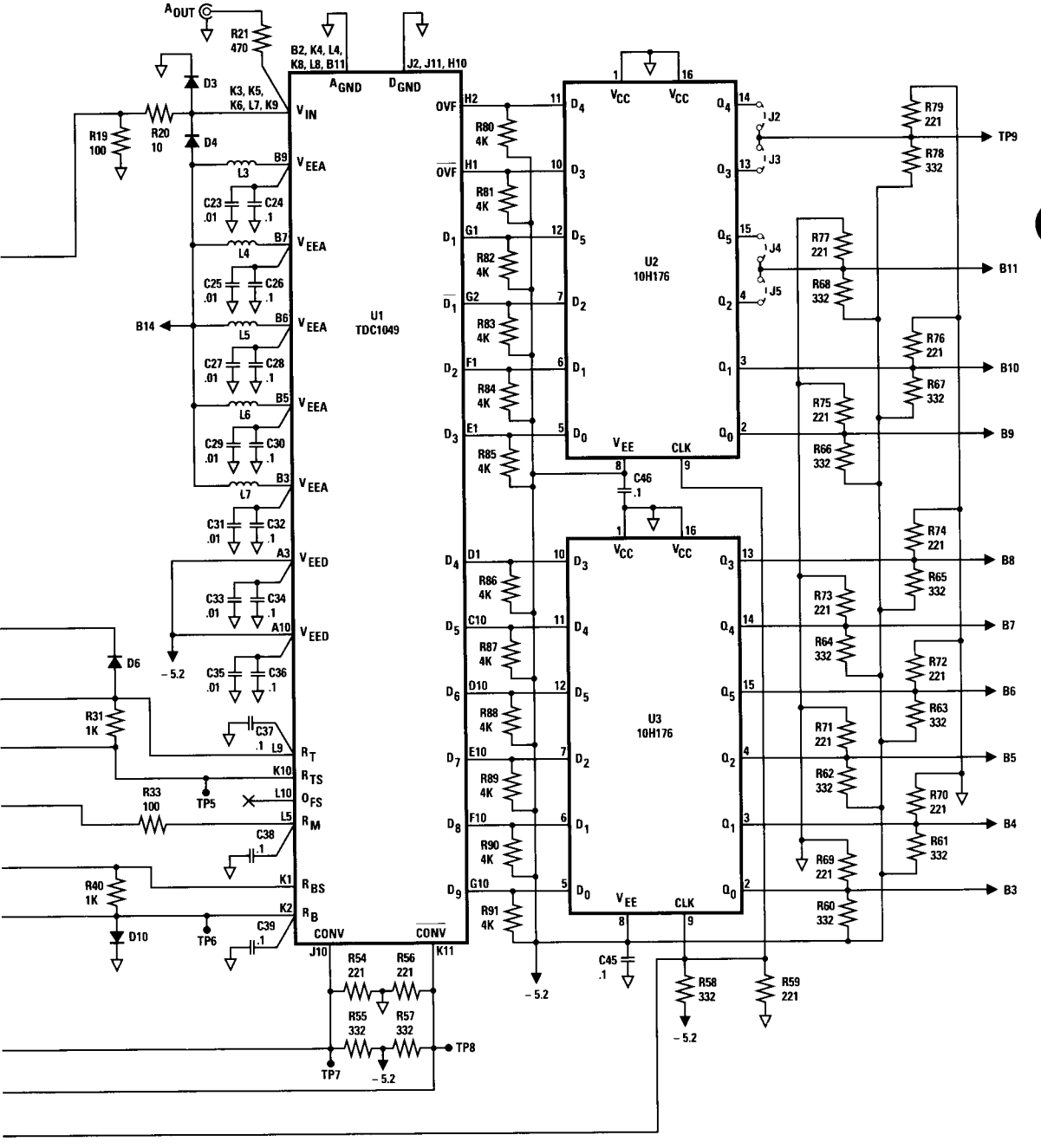
GND	A32	B32	V_{CC} (+5V)
GND	A31	B31	NC
GND	A30	B30	V− (−15V)
GND	A29	B29	NC
GND	A28	B28	V+ (+15V)
GND	A27	B27	D/A OUT−
GND	A26	B26	D/A OUT+
GND	A25	B25	NC
GND	A24	B24	D/A CONV
GND	A23	B23	D/A $\overline{\text{CONV}}$
GND	A22	B22	NC
GND	A21	B21	GND
GND	A20	B20	NC
GND	A19	B19	V_{EE} (−5.2V)
GND	A18	B18	NC
GND	A17	B17	GND
GND	A16	B16	NC
GND	A15	B15	NC
GND	A14	B14	V_{EE} (−5.2V)
GND	A13	B13	NC
GND	A12	B12	NC
D/A D_1 MSB	A11	B11	A/D D_1 MSB
NCD/A D_2	A10	B10	A/D D_2
D/A D_3	A9	B9	A/D D_3
D/A D_4	A8	B8	A/D D_4
D/A D_5	A7	B7	A/D D_5
D/A D_6	A6	B6	A/D D_6
D/A D_7	A5	B5	A/D D_7
D/A D_8	A4	B4	A/D D_8
D/A D_9 LSB	A3	B3	A/D D_9 LSB
A/D $\overline{\text{CONV}}$	A2	B2	A/D CONV
GND	A1	B1	GND

Mating Connectors for TDC1049E1C

AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

Figure 6. TDC1049E1C A/D Converter Schematic Diagram




AOUT
R21 470
D3
K3, K5, K6, L7, K9
R19 100
R20 10
D4
B2, K4, L4, K8, L8, B11
J2, J11, H10
AGND
DGND
VIN
VEEA
VEED
U1 TDC1049
B14
L3
L4
L5
L6
L7
C23 .01
C24 .1
C25 .01
C26 .1
C27 .01
C28 .1
C29 .01
C30 .1
C31 .01
C32 .1
C33 .01
C34 .1
C35 .01
C36 .1
C37 .1
C38 .1
C39 .1
B9
B7
B6
B5
B3
A3
A10
- 5.2
D6
R31 1K
L9
K10
R33 100
TP5
L10
L5
K1
R40 1K
K2
D10
TP6
RT
RTS
OFS
RM
RBS
RB
CONV
CONV
J10
K11
R54 221
R56 221
R55 332
R57 332
TP7
TP8
OVF
OVF
D1
D1
D2
D3
D4
D5
D6
D7
D8
D9
H2
H1
G1
G2
F1
E1
D1
C10
O10
E10
F10
G10
R80 4K
R81 4K
R82 4K
R83 4K
R84 4K
R85 4K
R86 4K
R87 4K
R88 4K
R89 4K
R90 4K
R91 4K
U2 10H176
U3 10H176
VCC
VEE
CLK
C46 .1
C45 .1
R58 332
R59 221
J2
J3
J4
J5
TP9
B11
B10
B9
B8
B7
B6
B5
B4
B3
R79 221
R78 332
R77 221
R68 332
R76 221
R67 332
R75 221
R66 332
R74 221
R65 332
R73 221
R64 332
R72 221
R63 332
R71 221
R62 332
R70 221
R61 332
R69 221
R60 332

A

Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

Standard Military Drawing	Nearest Equivalent TRW Product No.	Package
5962-88532-01XC	TDC1049J0V	64 Pin Ceramic DIP
5962-88532-01YC	TDC1049J3V	64 Pin Ceramic DIP
5962-88532-01ZA	TDC1049C1V	68 Contact Chip Carrier

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1049J0C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Ceramic DIP	1049J0C
TDC1049J0V	EXT – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Ceramic DIP	1049J0V
5962-88532 01XC	EXT – T_C = –55°C to 125°C	Per Standard Military Drawing	64 Pin Ceramic DIP	5962-88532 01XC
TDC1049C1C	STD – T_A = 0°C to 70°C	Commercial	68 Contact Ceramic LCC	1049C1C
TDC1049C1V	EXT – T_C = –55°C to 125°C	MIL-STD-883	68 Contact Ceramic LCC	1049C1V
5962-88532 01ZA	EXT – T_C = –55°C to 125°C	Per Standard Military Drawing	68 Contact Ceramic LCC	5962-88532 01ZA
TDC1049G8C	STD – T_A = 0°C to 70°C	Commercial	68 Pin Ceramic PGA	1049G8C
TDC1049G8V	EXT – T_C = –55°C to 125°C	MIL-STD-883	68 Pin Ceramic PGA	1049G8V
TDC1049E1C	STD – T_A = 0°C to 70°C	– –	Eurocard PC Board	TDC1049E1C