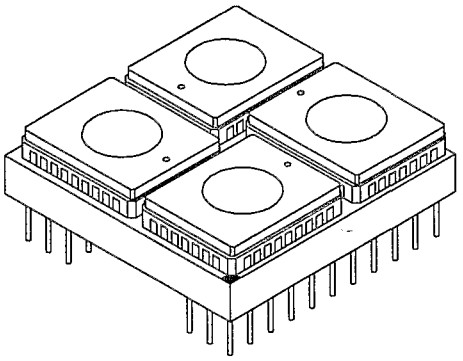
DPV3232V

32K X 32 UVEPROM VERSAPAC



DESCRIPTION:

The DPV3232V is a 66-pin Pin Grid Array (PGA) consisting of four 32K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a rotary pattern resulting in the smallest possible module outline.

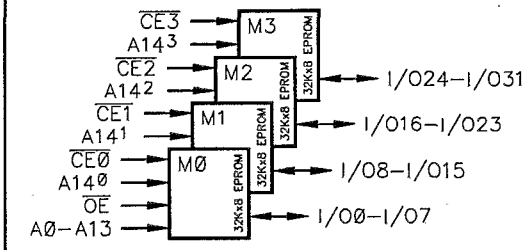
The pins have been arranged around a central 0.6" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing four 0.1µf decoupling capacitors.

FEATURES:

- Organizations Available:
  128K X 8, 64K X 16 or 32K X 32
- Access Times:
  55*, 70, 90, 120, 150, 170, 200, 250ns
- Fully Static Operation - No clock or refresh required
- Programming Voltage 12.5 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (1.0ms Pulses Typ.)
- Common Data Inputs and Outputs
- TTL-compatible Inputs and Outputs
- 66-Pin PGA (Pin Grid Array) Package
- Same Package as other Versapac Versions (EEPROM, SRAM and MIXED)
- Module Weight is 15 grams

* Commercial only.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0-A13, $A14^0$-$A14^3$	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
V_{PP}	Programming Voltage
N.C.	No Connect

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PIN-OUT DIAGRAM

1	I/08	12	$A14^1$	23	I/014				34	I/024	45	VDD	56	I/030
2	I/09	13	$\overline{CE1}$	24	I/013				35	I/025	46	$\overline{CE3}$	57	I/029
3	I/010	14	VSS	25	I/012				36	I/026	47	$A14^3$	58	I/028
4	A13	15	I/015	26	I/011				37	A6	48	I/031	59	I/027
5	VPP	16	A10	27	$\overline{OE}$				38	A7	49	A3	60	A0
6	N.C.	17	A11	28	N.C.		(TOP VIEW)		39	N.C.	50	A4	61	A1
7	N.C.	18	A12	29	$A14^0$				40	A8	51	A5	62	A2
8	N.C.	19	VDD	30	I/06				41	A9	52	$A14^2$	63	I/022
9	I/00	20	$\overline{CE0}$	31	I/05				42	I/016	53	$\overline{CE2}$	64	I/021
10	I/01	21	N.C.	32	I/04				43	I/017	54	VSS	65	I/020
11	I/02	22	I/07	33	I/03				44	I/018	55	I/023	66	I/019

ABSOLUTE MAXIMUM RATINGS[1]			
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [2]	-0.5 to +7.0	V
$V_{I/O}$	Input/Output Voltage [2]	-0.5 to +7.0	V
V_{PP}	Programming Voltage [2]	-0.5 to +13.0	V

RECOMMENDED OPERATING RANGE[2]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage[4]	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+1.0	V
V_{IL}	Input LOW Voltage	-0.2		0.8	V
V_{PP}	V_{PP} Supply Voltage[5]	12.25	12.5	12.75	V

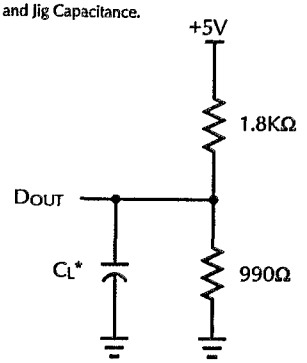
CAPACITANCE [3]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	15	pF	V_{IN} = 0V
C_{ADR}	Address Input	50		
C_{OE}	Output Enable	50		
$C_{I/O}$	Data Input/Output	25		

AC TEST CONDITIONS: Including Programming	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

Output Load		
Float	C_L	Parameters Measured
1	100 pF	except t_{DF} and t_{DFP}
2	5 pF	t_{DF} and t_{DFP}

Figure 1. Output Load

* Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS[6]: Over operating ranges										
Symbol	Characteristics	Test Conditions		X8		X16		X32		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = V_{DD}		-40	40	-40	40	-40	40	µA
I_{OUT}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{IN}=V_{DD} or V_{SS}		-40	40	-20	20	-10	10	µA
I_{CC}	V_{DD} Operation Current, Read	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA Cycle = min. Duty = 100%	120-250ns		85		150		280	mA
			55-90ns		225		270		360	
I_{SB1}	V_{DD} Standby Current I_{OUT} = 0mA (TTL)	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	120-250ns		20		20		20	mA
			55-90ns		180		180		180	
I_{SB2}	V_{DD} Standby Current (CMOS)	$\overline{CE}$ = V_{DD} ± 0.3V, I_{OUT} = 0mA V_{IN} ≥ V_{DD} -3.0V or V_{IN} ≤ 0.3V	120-250ns		1200		1200		1200	µA
			55-90ns		180		180		180	mA
I_{PP1}	V_{PP} Supply Current Programming	$\overline{CE}$, = V_{IL}, $\overline{OE}$ = V_{IH}			30		60		120	mA
I_{PP3}	V_{PP} Supply Current Read [4]	$\overline{CE}$, $\overline{OE}$ = V_{IL}, I_{OUT} > 0mA			800		800		800	µA
V_{OL}	Output LOW Voltage	I_{OUT} = 2.1mA			0.45		0.45		0.45	V
V_{OH1}	Output HIGH Voltage	I_{OUT} = -400µA		2.4		2.4		2.4		V
V_{IL}	Input LOW Level			-0.2	0.8	-0.2	0.8	-0.2	0.8	V
V_{IH}	Input HIGH Level			2.2	V_{DD}+1	2.2	V_{DD}+1	2.2	V_{DD}+1	V

FUNCTIONS AND PIN CONNECTIONS						
Mode	Function	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	I/O0 - I/O31
Read Operations	Read	L	L	5V	5V	Data Out
	Output Deselect	L	H			High Impedance
	Standby	H	X			High Impedance
Program Operations (T_A = +25 ± 5°C)	Program	L	H	12.5V	6V	Data In
	Program Inhibit	H	H			High Impedance
	Program Verify	H	L			Data Out

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges											
No.	Symbol	Parameter	-55*		-70		-90		-120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address Access Time [8]		55		70		90		120	ns
2	t_{CE}	Chip Enable to Output Valid [7]		55		70		90		120	ns
3	t_{OE}	Output Enable to Output Valid [7, 8]		30		30		35		35	ns
4	t_{DF}	$\overline{OE}$ or $\overline{CE}$ HIGH to Output Float [3, 9]	0	30	0	30	0	35	0	35	ns
5	t_{OH}	Output Hold from Address Change	0		0		0		0		ns

* Commercial only.

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges											
No.	Symbol	Parameter	-150		-170		-200		-250		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address Access Time [8]		150		170		200		250	ns
2	t_{CE}	Chip Enable to Output Valid [7]		150		170		200		250	ns
3	t_{OE}	Output Enable to Output Valid [7, 8]		70		70		75		100	ns
4	t_{DF}	$\overline{OE}$ or $\overline{CE}$ HIGH to Output Float [3, 9]	0	50	0	50	0	55	0	60	ns
5	t_{OH}	Output Hold from Address Change	0		0		0		0		ns

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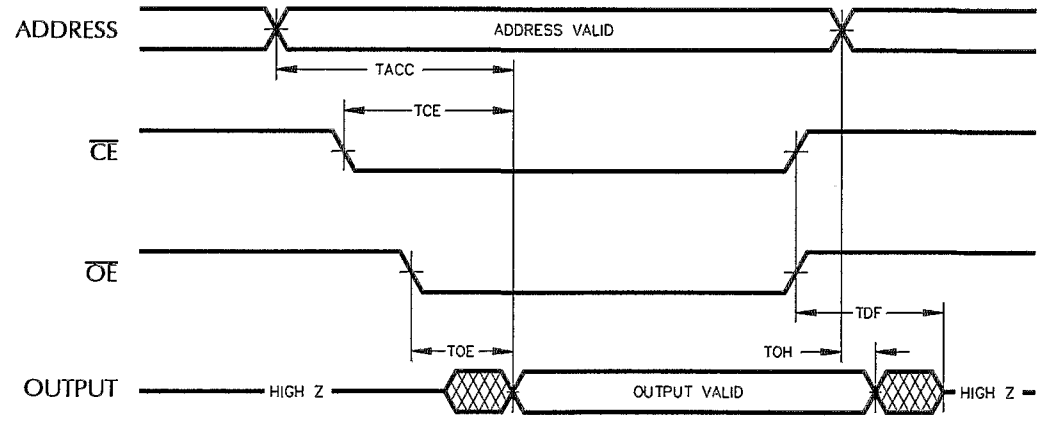
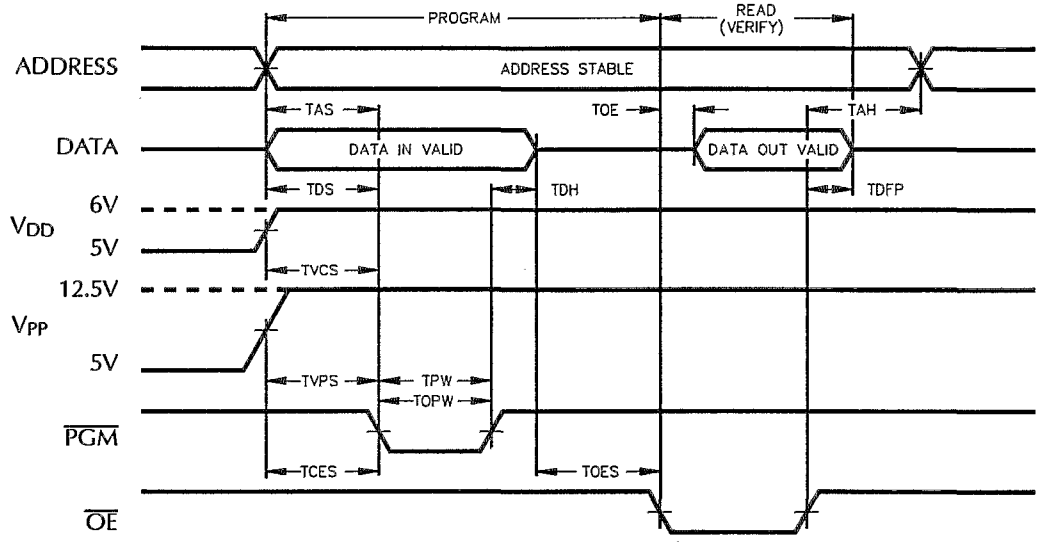
AC PROGRAMMING CONDITIONS AND CHARACTERISTICS: Over operating ranges					
No.	Symbol	Parameter	Min.	Max.	Unit
6	t_{AS}	Address Set-up Time	2		µs
7	t_{CES}	Chip Enable Set-up Time	2		µs
8	t_{OES}	Output Enable Set-up Time	2		µs
9	t_{DS}	Data Set-up Time	2		µs
10	t_{VCS}	V_{DD} Set-up Time [5]	2		µs
11	t_{VPS}	V_{PP} Set-up Time [5]	2		µs
12	t_{AH}	Address Hold Time	0		µs
13	t_{DH}	Data Hold Time	2		µs
14	t_{DFP}	Output Enable HIGH Output Float Delay [3]	0	130	ns
15	t_{PW}	Programming Pulse Width [10]	0.95	1.05	ms
16	t_{OPW}	Over Programming Pulse Width [11]	2.85	78.75	ms

READ TIMING



PROGRAMMING TIMING [4]



PROGRAMMING AND ERASING INFORMATION

Programming

Upon delivery from Dense-Pac, or after erasure *(See Erasure section)*, the DPV3232V contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV3232V through the procedure of programming. A 0.1µF capacitor between V_{PP} and V_{SS} is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.0V and +12.5V to be applied to V_{DD} and V_{PP} respectively.

Individual bytes or address locations can be selected and programmed by using the programming algorithm shown in Figure 2. In the programming mode, $\overline{CE}$ is set at V_{IL}, $\overline{OE}$ is set at V_{IH}, V_{DD} is set at +6.0V, and V_{PP} is set at +12.5V. After the applied address and input data signals are stable, programming is accomplished by a 1.0ms V_{IL} pulse on the $\overline{CE}$ pin *(refer to the Programming Timing Diagram)*.

The programmed byte is then verified. If the programming was successful, then a 3ms over program pulse is applied. If the programming was unsuccessful after the first 1ms pulse, then up to 25 1ms pulses are applied with a verification after each pulse. When the byte passes, an over program pulse of 3ms times the number of initial programming pulses *(78.75ms max.)* is applied.

If the device fails to program after 25 attempts, the programming is considered failed. After the first byte is programmed, continue the algorithm through all the required addresses. Then lower V_{DD} and V_{PP} to +5.0Vdc and compare the data programmed with the original data to determine if the device passes. A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

Erasure

To clear all locations of their programmed contents it is necessary to expose the DPV3232V to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase a DPV3232V. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å) with an intensity of 12,000µW/cm^2] for 21 minutes.

The DPV3232V and similar devices can be erased by light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV3232V. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

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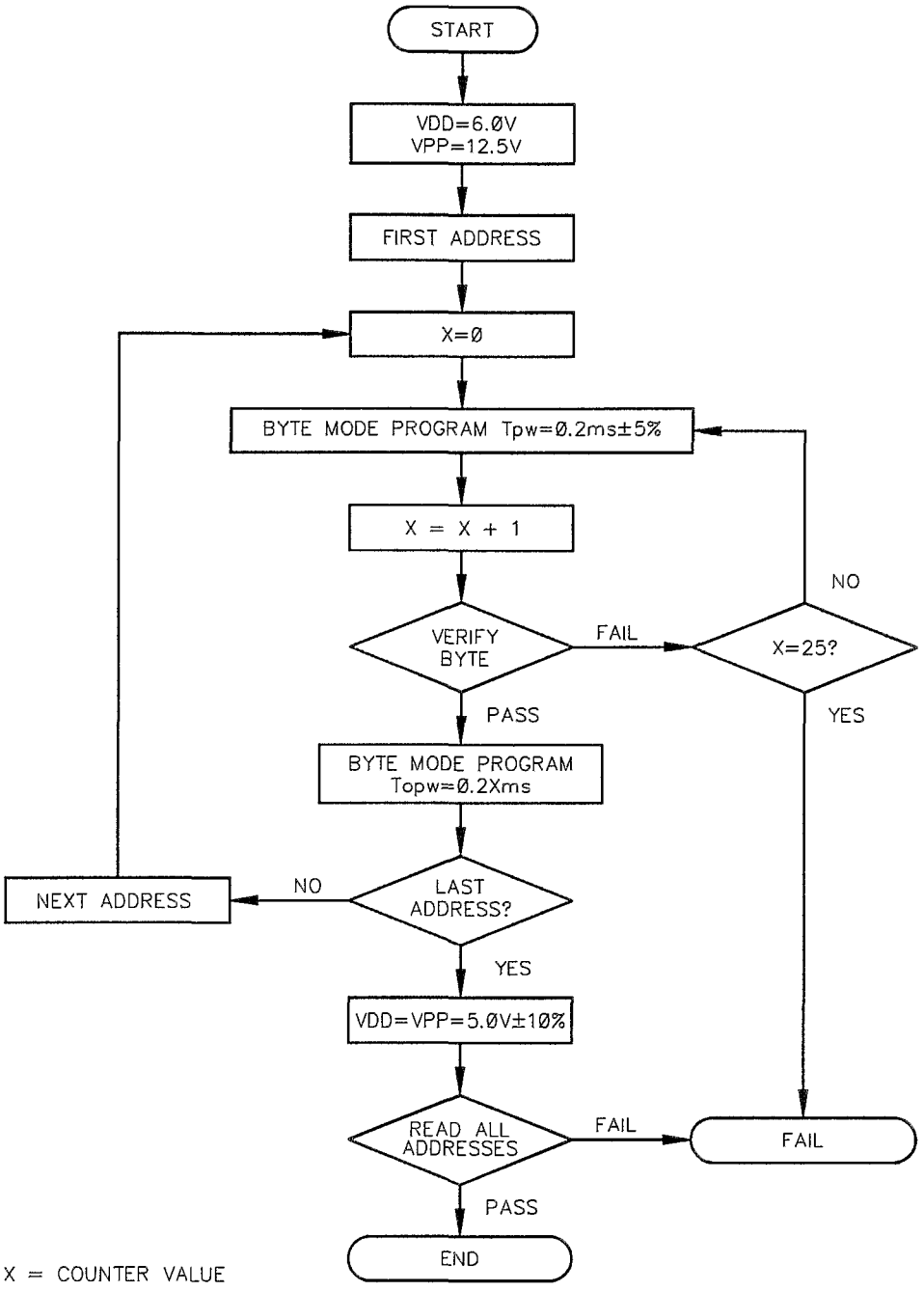
NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. All voltages are with respect to V_{SS}.
3. This parameter is guaranteed and not 100% tested.
4. V_{DD} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP}.
5. V_{PP} must not be greater than 13.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with V_{PP} = 13.0V. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from 5.0V to 13.0V or vice-versa.
6. t_A = -55°C to +125°C, V_{DD} = 5.0V ± 0.5V, and V_{PP} = V_{DD} reading. t_A = +25°C ± 5°C, V_{DD} = 6.0 ± 0.25V, V_{PP} = 12.5V ± 0.3V programming.
7. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the following edge of $\overline{CE}$ without impact on t_{CE}.
8. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the following Address is valid without impact on t_{ACC}.
9. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
10. Initial Program Pulse Width Tolerance is 1ms ± 5%.
11. The length of the overprogram pulse may vary from 2.85ms to 78.75ms as a function of the iteration counter value X.

Figure 2. Programming Flow Chart



ORDERING INFORMATION

DP	V3232	V	– XXX	X
PREFIX	DEVICE TYPE	PACKAGE	SPEED	GRADE

C	COMMERCIAL	0° to +70°C
I	INDUSTRIAL	−40° to +85°C
M	MILITARY	−55° to +125°C
B *	MIL−PROCESSED	−55° to +125°C

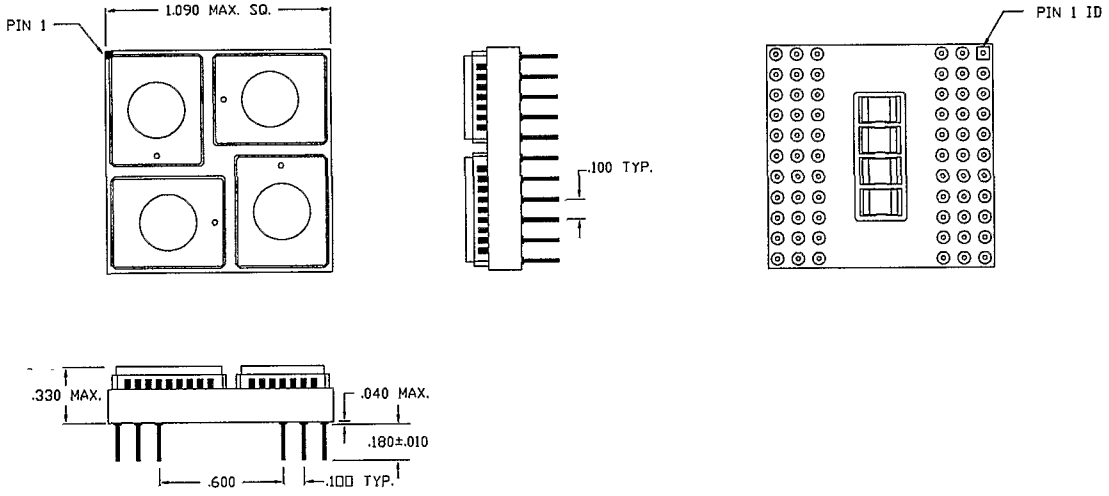
55	55ns	(COMMERCIAL ONLY)
70	70ns	
90	90ns	
120	120ns	
150	150ns	
170	170ns	
200	200ns	
250	250ns	

V 66−PIN PGA VERSAPAC

UVEPROM 128KX8, 64KX16 OR 32KX32

* B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAMS



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