

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

** The contents of this document are subject to change without notice*

DATA SHEET

HY5DU1294022-75/80/10

HY5DU1298022-75/80/10

HY5DU1291622-75/80/10

HY5DV1294022-75/80/10

HY5DV1298022-75/80/10

HY5DV1291622-75/80/10

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

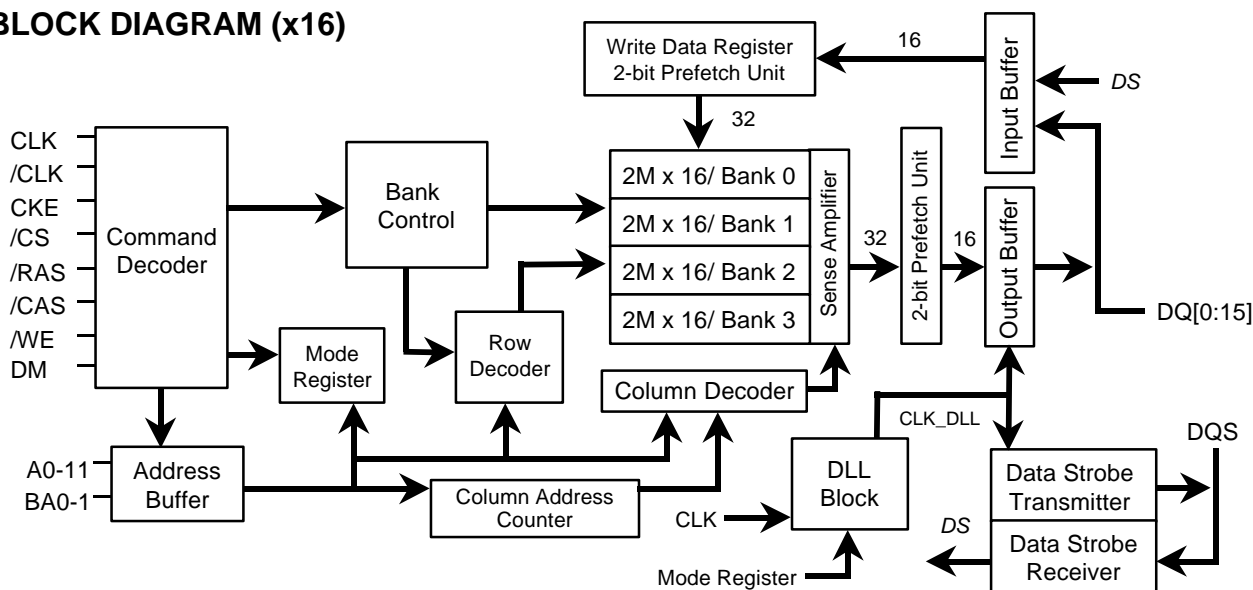
DESCRIPTION

HY5DU(V)1294022-75/80/10, HY5DU(V)1298022-75/80/10 and HY5DU(V)1291623-75/80/10 are high speed 2.5V(U-part) and 3.3V(V-part) (I/O VDDQ=2.5V for all U,V-parts) 128M Double Data Rate(DDR) Synchronous DRAM's fabricated with the Hyundai high performance CMOS process. While all address and control inputs are latched on the rising edge of the clock(falling edge of the /clock), data, data strobe and data mask inputs are sampled on both rising and falling edge of the clock. The data path is internally pipelined and 2-bit pre-fetched to achieve higher bandwidth. Because data rate is doubled through reading and writing at both rising and falling edge of the clock, 2X higher data bandwidth can be achieved.

FEATURES

- 2.5V VDD(U-part), 3.3V VDD(V-part) and 2.5V VDDQ power supply for both parts
- Internal 4 banks with single pulsed RAS
- Fully differential clock operation with clock frequency 100MHz/125MHz/133MHz
- Data output on data strobe(DQS) edge when read (edged DQ)
- Data input on data strobe(DQS) center when write (centered DQ)
- Data strobe synchronized with output data for read and input data for write
- Programmable CAS latency 2.0/2.5/3.0 supported
- Programmable burst length 2/4/8 with both sequential and interleave mode
- Delay Locked Loop(DLL) installed with DLL reset mode
- SSTL_2 interface for all inputs and outputs
- Write mask byte control with LDM and UDM
- Byte-wide data strobe with LDQS and UDQS
- Auto refresh and self refresh supported
- 4K/64ms refresh cycle
- 400mil 66 pin 0.65mm pin pitch TSOP-II package

BLOCK DIAGRAM (x16)



HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

ORDERING INFORMATION

HY 5D U 129 40 2 2 L TC - 10

HYUNDAI

Memory Products

PRODUCT GROUP

- 55 - FP DRAM
- 56 - EDO DRAM
- 57 - SDRAM
- 5D - DDR SDRAM

PROCESS & POWER SUPPLY

- BLANK - CMOS 5.0V VDD
- V - CMOS 3.3V VDD
- U - CMOS 2.5V VDD

DENSITY & REFRESH CYCLE

- 64 - 64M bits, 8K refresh
- 65 - 64M bits, 4K refresh
- 128 - 128M bits, 8K refresh
- 129 - 128M bits, 4K refresh

DATA WIDTH

- 40 - x4
- 80 - x8
- 16 - x16
- 32 - x32

NUMBER OF BANKS

- 1 - 2 banks
- 2 - 4 banks

SPEED

- 75 - 7.5ns(133MHz)
- 80 - 8ns(125MHz)
- 10 - 10ns(100MHz)
- 12 - 12ns(83MHz)
- 15 - 15ns(66MHz)
- 10P - PC/100, CL=2/3
- 10S - PC/100, CL=2

PACKAGE

- JC - 400mil SOJ
- TC - 400mil TSOP-II

POWER CONSUMPTION

- BLANK - Normal
- L - Low power

DIE GENERATION

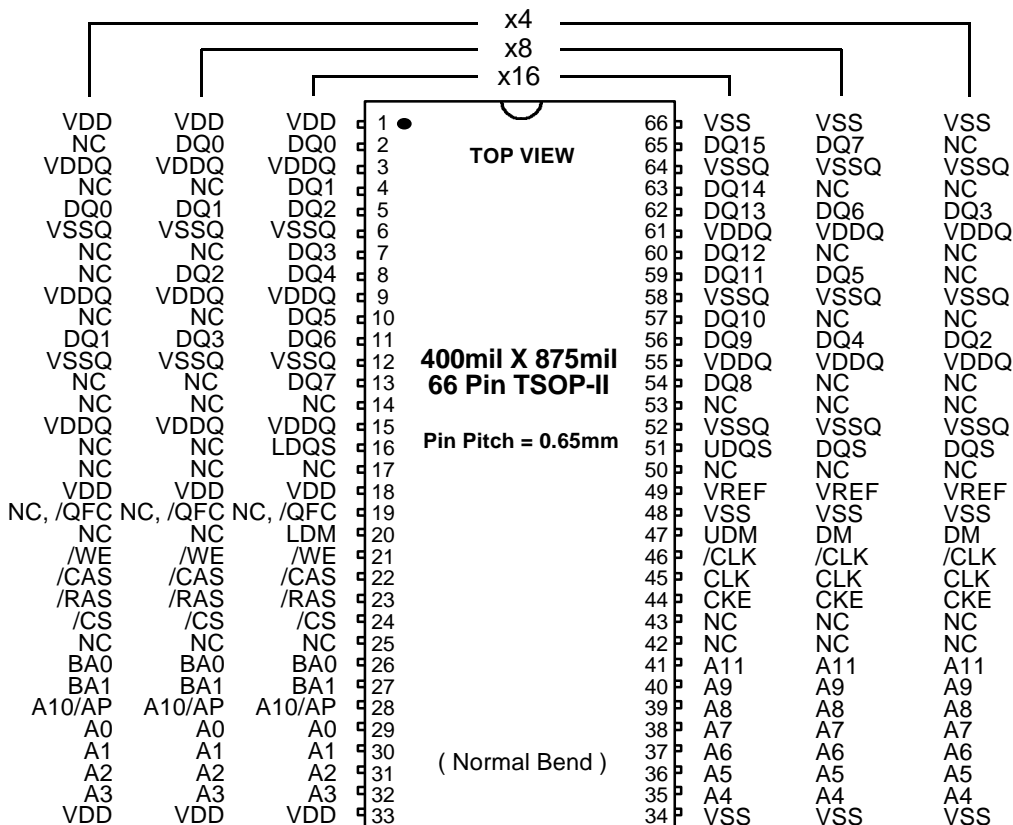
- BLANK - 1st Gen.
- A - 2nd Gen.
- B - 3rd Gen.
- C - 4th Gen.

INTERFACE

- 0 - LVTTTL
- 1 - SSTL-3
- 2 - SSTL-2
- 3 - Mixed Interface

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

PIN CONFIGURATION & DESCRIPTION



Pin	Description
A0 - A11	Row / Column Address
BA0, BA1	Bank Select Address
DQ0 - DQ15	Data Input/Output
/CS	Chip Select
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
LDM, UDM	Write Mask(Lower/Upper Byte)
CLK, /CLK	Clock Input
CKE	Clock Enable
LDQS, UDQS	Data Strobe(Lower/Upper Byte)
VREF	Reference Voltage
VDD, VSS	Power, Ground
VDDQ, VSSQ	I/O Power, I/O Ground
/QFC	DQ FET Switch Control(optional)
NC	No Connection

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

ADDRESS MAPPING TABLE

Organization	Bank Select	Row Address	Column Address	Autoprecharge
x4	BA0, BA1	A0 ~ A11	A0~A9, A11	A10
x8	BA0, BA1	A0 ~ A11	A0~A9	A10
x16	BA0, BA1	A0 ~ A11	A0~A8	A10

COMMAND TRUTH TABLE

Function	Symbol	CKE _{n-1}	CKE _n	/CS	/RAS	/CAS	/WE	A11	A10	BA	A9-0
Device Deselect	DSEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V	V
Read w/ Autoprecharge	READAP	H	X	L	H	L	H	V	H	V	V
Write	WRITE	H	X	L	H	L	L	V	L	V	V
Write w/ Autoprecharge	WRITEAP	H	X	L	H	L	L	V	H	V	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V	V
Precharge Selected Bank	PRE	H	X	L	L	H	L	X	L	V	X
Precharge All Banks	PALL	H	X	L	L	H	L	X	H	X	X
Read Burst Stop	BST	H	X	L	H	H	L	X	X	X	X
Auto Refresh	AREF	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	SREF	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	SREX	L	H	H	X	X	X	X	X	X	X
Power Down Entry	PDEN	H	L	X	X	X	X	X	X	X	X
Power Down Exit	PDEX	L	H	H	X	X	X	X	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V	V

WRITE DATA MASK TRUTH TABLE

Function	CKE _{n-1}	CKE _n	UDM	LDM
Data Write/Output Enable	H	X	L	L
Data Mask/Output Disable	H	X	H	H
Upper Byte Write Enable / Lower Byte Mask	H	X	L	H
Lower Byte Write Enable / Upper Byte Mask	H	X	H	L

Notes : 'H' - Logic High Level, 'L' - Logic Low Level, 'X' - Don't Care, 'V' - Valid Data Input

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

OPERATION COMMAND TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DSEL	NOP or power down ³
	L	H	H	H	X	NOP	NOP or power down ³
	L	H	H	L	X	BST	ILLEGAL ⁴
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL ⁴
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL ⁴
	L	L	H	H	BA, RA	ACT	Row Activation
	L	L	H	L	BA, A10	PRE/PALL	NOP
	L	L	L	H	X	AREF/SREF	Auto Refresh or Self Refresh ⁵
	L	L	L	L	OPCODE	MRS	Mode Register Set
ROW ACTIVE	H	X	X	X	X	DSEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL ⁴
	L	H	L	H	BA, CA, A10	READ/READAP	Begin read : optional AP ⁶
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	Begin write : optional AP ⁶
	L	L	H	H	BA, RA	ACT	ILLEGAL ⁴
	L	L	H	L	BA, A10	PRE/PALL	Precharge ⁷
	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
READ	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Terminate burst
	L	H	L	H	BA, CA, A10	READ/READAP	Term burst, new read:optional AP ⁸
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL ⁴
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
WRITE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL ⁴
	L	H	L	H	BA, CA, A10	READ/READAP	Term burst, new read:optional AP ⁸
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	Term burst, new write:optional AP

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

OPERATION COMMAND TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	L	L	H	H	BA, RA	ACT	ILLEGAL ⁴
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharge
	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
READ WITH AUTOPRE-CHARGE	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL ¹⁰
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL ¹⁰
	L	L	H	H	BA, RA	ACT	ILLEGAL ^{4,10}
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ^{4,10}
	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
WRITE WITH AUTOPRE-CHARGE	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
	H	X	X	X	X	DSEL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL ¹⁰
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL ¹⁰
	L	L	H	H	BA, RA	ACT	ILLEGAL ^{4,10}
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ^{4,10}
PRE-CHARGE	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
	H	X	X	X	X	DSEL	NOP - Enter IDLE after tRP
	L	H	H	H	X	NOP	NOP - Enter IDLE after tRP
	L	H	H	L	X	BST	ILLEGAL ⁴
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL ^{4,10}
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL ^{4,10}
	L	L	H	H	BA, RA	ACT	ILLEGAL ^{4,10}
	L	L	H	L	BA, A10	PRE/PALL	NOP - Enter IDLE after tRP
L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹	
L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹	

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

OPERATION COMMAND TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
ROW ACTIVATING	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tRCD
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tRCD
	L	H	H	L	X	BST	ILLEGAL ⁴
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL ^{4,10}
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL ^{4,10}
	L	L	H	H	BA, RA	ACT	ILLEGAL ^{4,9,10}
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ^{4,10}
	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
WRITE RECOVERING	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
	H	X	X	X	X	DSEL	NOP - Enter ROW ACT after tDPL
	L	H	H	H	X	NOP	NOP - Enter ROW ACT after tDPL
	L	H	H	L	X	BST	ILLEGAL ⁴
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL ^{4,10}
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ^{4,11}
WRITE RECOVERING WITH AUTOPRECHARGE	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
	H	X	X	X	X	DSEL	NOP - Enter precharge after tDPL
	L	H	H	H	X	NOP	NOP - Enter precharge after tDPL
	L	H	H	L	X	BST	ILLEGAL ⁴
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL ^{4,8,10}
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL ^{4,10}
	L	L	H	H	BA, RA	ACT	ILLEGAL ^{4,10}
REFRESHING	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ^{4,11}
	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
	H	X	X	X	X	DSEL	NOP - Enter IDLE after tRC
REFRESHING	L	H	H	H	X	NOP	NOP - Enter IDLE after tRC
	L	H	H	L	X	BST	ILLEGAL ¹¹
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL ¹¹

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

OPERATION COMMAND TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
REFRESH- ING	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL ¹¹
	L	L	H	H	BA, RA	ACT	ILLEGAL ¹¹
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ¹¹
	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
	L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹
MODE REGISTER ACCESSING	H	X	X	X	X	DSEL	NOP - Enter IDLE after tMRD
	L	H	H	H	X	NOP	NOP - Enter IDLE after tMRD
	L	H	H	L	X	BST	ILLEGAL ¹¹
	L	H	L	H	BA, CA, A10	READ/READAP	ILLEGAL ¹¹
	L	H	L	L	BA, CA, A10	WRITE/WRITEAP	ILLEGAL ¹¹
	L	L	H	H	BA, RA	ACT	ILLEGAL ¹¹
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL ¹¹
	L	L	L	H	X	AREF/SREF	ILLEGAL ¹¹
L	L	L	L	OPCODE	MRS	ILLEGAL ¹¹	

Notes :

- 'H' - Logic High Level, 'L' - Logic Low Level, 'X' - Don't Care, 'V' - Valid Data Input, BA - Bank Address AP - Auto Precharge, CA - Column Address, RA - Row Address, NOP - NO Operation
- All entries assume that CKE was active(high level) during the preceding clock cycle.
- If both banks are idle and CKE is inactive(low level), then in power down mode.
- Illegal to bank in specified state. Function may be legal in the bank indicated by Bank Address(BA), depending on the state of that bank.
- If both banks are idle and CKE is inactive(low level), then self refresh mode.
- Illegal if tRCD is not met
- Illegal if tRAS is not met.
- Must satisfy bus contention, bus turn around, and/or write recovery requirements
- Illegal if tRRD is not met.
- Illegal for single bank, but legal for other banks in multi-bank devices.
- Illegal for all banks.

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

CKE FUNCTION TRUTH TABLE

Current State	CKE _{n-1}	CKE _n	/CS	/RAS	/CAS	/WE	ADD	Action
SELF¹ REFRESH	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit self refresh, enter idle after tSREX
	L	H	L	H	H	H	X	Exit self refresh, enter idle after tSREX ³
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue self refresh
POWER² DOWN	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit power down, enter idle
	L	H	L	H	H	H	X	Exit power down, enter idle
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP, continue power down mode
ALL⁴ BANKS IDLE	H	H	X	X	X	X	X	See operation command truth table
	H	L	L	L	L	H	X	Enter self refresh
	H	L	H	X	X	X	X	Enter power down
	H	L	L	H	H	H	X	Enter power down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	L	X	ILLEGAL
Any State other than above	L	L	X	X	X	X	X	NOP
	H	H	X	X	X	X	X	See operation command truth table
	H	L	X	X	X	X	X	ILLEGAL ⁵
	L	H	X	X	X	X	X	INVALID
	L	L	X	X	X	X	X	INVALID

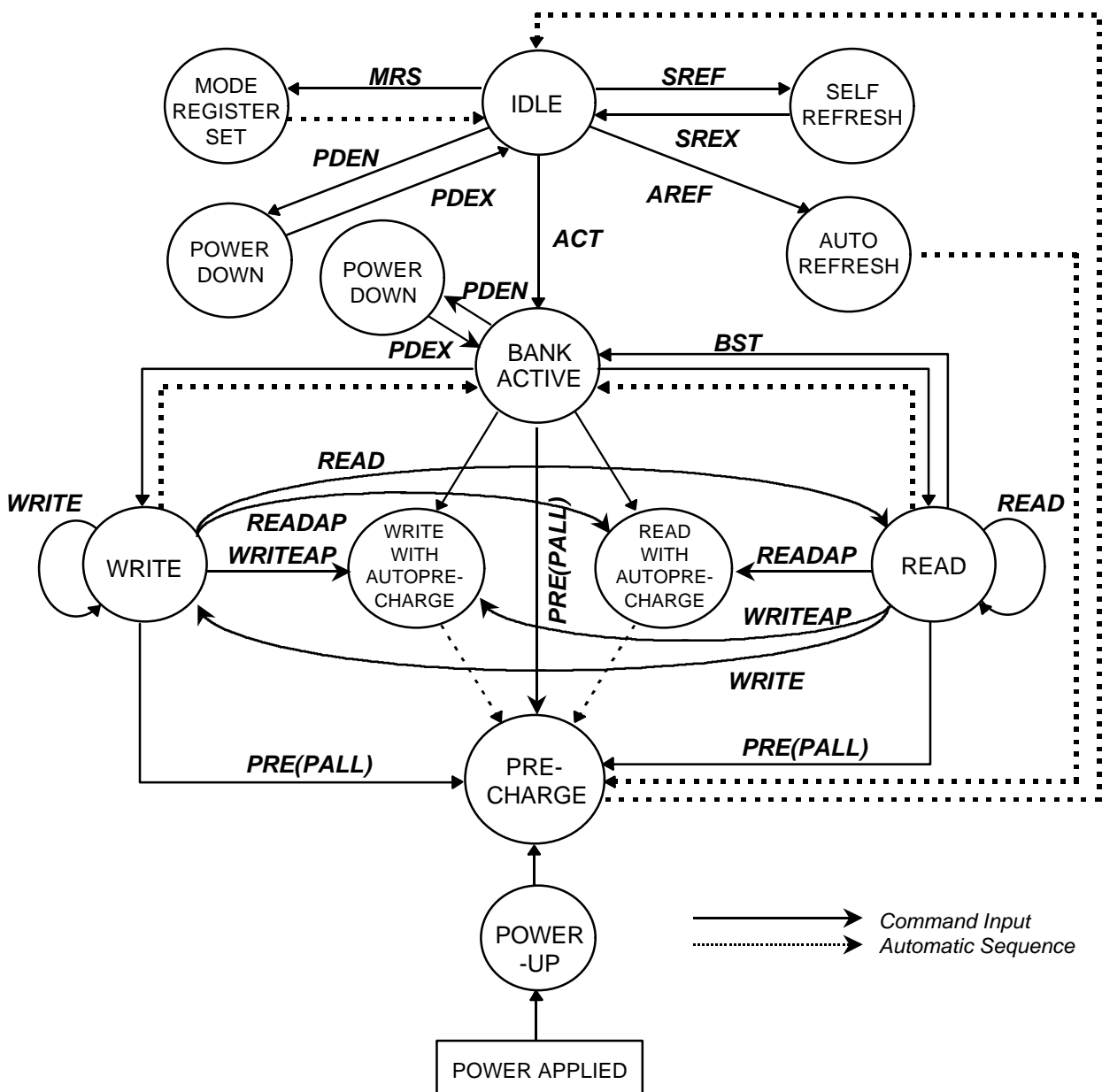
Notes :

When CKE=L, all DQ and DQS must be in Hi-Z state

1. CKE and /CS must be kept high for a minimum of 200 stable input clocks before issuing any command
2. All command can be stored after 2 clocks from low to high transition of CKE
3. Illegal if CLK is suspended or stopped during the power down mode
4. Self refresh can be entered only from the all banks idle state
5. Disabling CLK may cause malfunction if any bank is in active state

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

SIMPLIFIED STATE DIAGRAM



HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

MODE REGISTER TABLE

The mode register of DDR SDRAM provides a variety of different options. The mode register can be programmed by the Mode Register Set(MRS) command. Once mode register field is determined, the information will be held until reset by another MRS command.

BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	RFU*			DR*	TM*	CAS Latency(CL)			BT*	Burst Length(BL)		

*BT=Burst Type, TM=Test Mode, DR=DLL Reset, RFU=Reserved for Future Use
RFU Address fields (A11,A10, A9) must be "0" during MRS entry

A8	DLL Reset
0	No
1	Yes

A7	Test Mode
0	Normal Operation
1	Test Mode Entry

A3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2.0
0	1	1	3.0
1	0	0	Reserved
1	0	1	(1.5)
1	1	0	2.5
1	1	1	Reserved

A2	A1	A0	Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

BURST SEQUENCE TABLE

The burst type can be determined either sequential or interleave by MRS command. DDR SDRAM provides any starting address for bursting read and write data as SDR SDRAM.

Start Address	Sequential	Interleave
A0=0	0,1	0, 1
A0=1	1,0	1, 0
A1=0, A0=0	0, 1, 2, 3	0, 1, 2, 3
A1=0, A0=1	1, 2, 3, 0	1, 0, 3, 2
A1=1, A0=0	2, 3, 0, 1	2, 3, 0, 1
A1=1, A0=1	3, 0, 1, 2	3, 2, 1, 0
A2=0, A1=0, A0=0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
A2=0, A1=0, A0=1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
A2=0, A1=1, A0=0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
A2=0, A1=1, A0=1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
A2=1, A1=0, A0=0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
A2=1, A1=0, A0=1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
A2=1, A1=1, A0=0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
A2=1, A1=1, A0=1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

EXTENDED MODE REGISTER TABLE - refer to page 17 for details, field for BA=1 is still reserved

BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	RFU									QFC	ZO	DLL

A2	DQ FET Switch Control
0	/QFC Disable
1	/QFC Enable

A1	Output Impedance Control
0	Full SSTL_2 Class II Driver
1	Half SSTL_2 Class II Driver

A0	DLL ON/OFF
0	DLL Enable
1	DLL Disable

Output Impedance Control

Detailed requirements for half strength driver will be supplemented

DQ FET Switch Control

Detailed timing requirements will be supplemented

HYUNDAI 4 Banks X 8/4/2M X 4/8/16 bits DDR SDRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Rating	Unit
T _A	Ambient temperature	0 ~ 70	°C
T _{STG}	Storage temperature	-55 ~ 125	°C
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5 ~ 3.6	Volts
V _{DD} (U-part)	Voltage on V _{DD} relative to V _{SS}	-0.5 ~ 3.6	Volts
V _{DD} (V-part)	Voltage on V _{DD} relative to V _{SS}	-1.0 ~ 4.6	Volts
V _{DDQ}	Voltage on V _{DDQ} relative to V _{SS}	-0.5 ~ 3.6	Volts
I _{OS}	Output short circuit current	50	mA
P _D	Power dissipation	1	W
T _{SOLDER}	Soldering temperature X time	260 X10	°C X sec

Notes : Operation other than above table can adversely affect the device reliability

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70 °C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V _{DD} (U-part)	Power supply voltage	3.0	3.3	3.6	Volts
V _{DD} (V-part)	Power supply voltage	2.3	2.5	2.7	Volts
V _{DDQ} ¹	Power supply voltage	2.3	2.5	2.7	Volts
V _{SS} , V _{SSQ}	Power supply voltage	0	0	0	Volts
V _{IL} (DC) ²	Input DC low voltage	-0.3	-	V _{REF} - 0.18	Volts
V _{IH} (DC)	Input DC high voltage	V _{REF} + 0.18	-	V _{DDQ} + 0.3	Volts
V _{IL} (AC)	Input AC low voltage	-	-	V _{REF} - 0.35	Volts
V _{IH} (AC)	Input AC high voltage	V _{REF} + 0.35	-	-	Volts
V _{OL} ³	Output low voltage	-	-	V _{TT} - 0.76	Volts
V _{OH} ⁴	Output high voltage	V _{TT} + 0.76	-	-	Volts
V _{TT}	Termination voltage	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04	Volts
V _{REF} ⁵	Reference voltage	1.15	1.25	1.35	Volts
R _T	Termination resistor	-	50	-	Ohms
R _S	Series resistor	-	25	-	Ohms

Notes : 1. V_{DDQ} must not exceed the level of V_{DD}

2. V_{IL,min} (AC) = -1.5V (pulse width < 5ns)

3. I_{OL} = 15.2mA, 4. I_{OH} = -15.2mA 5. The value of V_{REF} is approximately equal to 0.5V_{DDQ}

CAPACITANCE

(T_A = 25 °C, f = 1MHz)

Symbol	Parameter	Pin	Min.	Max.	Unit
C _{IN}	Input capacitance	Addresses, all inputs	2.5	3.5	pF
C _{CLK}	Clock capacitance	CLK, /CLK	2.5	3.5	pF
C _{IO}	I/O capacitance	DQ0 - DQ15, DQS, DM	4.0	5.5	pF

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DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Maximum	Unit
I _{LI}	Input leakage current	V _{applied} =0 to 3.6V w/ all other pins=0V	5	uA
I _{LO}	Output leakage current	V _{applied} =0 to 2.7V w/ DOUT is disabled	5	uA
I _{CC1}	Operating current	No CAS activity, 1 bank active t _{RC} =minimum cycle	TBD	mA
I _{CC2N}	Precharge standby current (Non-power down mode)	CKE ≥ V _{IH(min)} in all banks idle state t _{CK} =minimum cycle	TBD	mA
I _{CC2P}	Precharge standby current (Power down mode)	CKE ≤ V _{IL(max)} in all banks idle state t _{CK} =minimum cycle	TBD	mA
I _{CC3N}	Active standby current (Non-power down mode)	CKE ≥ V _{IH(min)} in all banks active state t _{CK} =minimum cycle	TBD	mA
I _{CC3P}	Active standby current (Power down mode)	CKE ≤ V _{IL(max)} in all banks active state t _{CK} =minimum cycle	TBD	mA
I _{CC4}	Burst operating current	With CAS activity, t _{CK} =minimum cycle	TBD	mA
I _{CC5}	Refresh current	t _{RC} =minimum cycle with auto refresh mode	TBD	mA
I _{CC6}	Self refresh current	CKE ≤ 0.2V at self refresh mode	TBD	mA

AC CHARACTERISTICS I - TIMING

Symbol	Parameter	- 7.5		- 8		- 10		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{CK}	Clock cycle time	CL=2.0	8	15	10	15	10	15	ns
		CL=2.5	7.5	15	7.5	15	8	15	ns
		CL=3.0	7.5	15	7.5	15	8	15	ns
f _D	Maximum data rate	-	266	-	250	-	200	Mb/s	
t _{CH}	Clock high level width	0.45	-	0.45	-	0.45	-	t _{CK}	
t _{CL}	Clock low level width	0.45	-	0.45	-	0.45	-	t _{CK}	
t _{AC}	DQ edge to clock edge skew	- 0.1	0.1	- 0.1	0.1	- 0.1	0.1	t _{CK}	
t _{DQSCK}	DQS edge to clock edge skew	- 0.1	0.1	- 0.1	0.1	- 0.1	0.1	t _{CK}	
t _{DQCK}	DQ edge to clock edge skew	- 0.1	0.1	- 0.1	0.1	- 0.1	0.1	t _{CK}	
t _{DQSQ}	DQS edge to DQ edge skew	- 0.075	0.075	- 0.075	0.075	- 0.075	0.075	t _{CK}	
t _{HZQ}	DQ output Lo-Z to Hi-Z delay	-	3	-	3	-	4	ns	

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AC CHARACTERISTICS I - TIMING

Symbol	Parameter	- 7.5		- 8		- 10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tdv	Data valid window	0.35	-	0.35	-	0.35	-	tck
tdqsv	Data strobe valid window	0.35	-	0.35	-	0.35	-	tck
trPRE	Read DQS preamble time	0.9	1.1	0.9	1.1	0.9	1.1	tck
trPST	Read DQS postamble time	0.4	0.6	0.4	0.6	0.4	0.6	tck
twPRES	Write DQS preamble setup time	0	-	0	-	0	-	tck
twPREH	Write DQS preamble hold time	0.25	-	0.25	-	0.25	-	tck
twPST	DQS last falling edge to Hi-Z	0.4	0.6	0.4	0.6	0.4	0.6	tck
tdQSS	CLK to first rising edge of DQS	0.75	1.25	0.75	1.25	0.75	1.25	tck
tis ¹	Input setup time to clock	0.15	-	0.15	-	0.15	-	tck
tih ¹	Input hold time to clock	0.15	-	0.15	-	0.15	-	tck
tdDQSS ²	DQ setup time to DQS	0.075	-	0.075	-	0.075	-	tck
tdDQSH ²	DQ hold time to DQS	0.075	-	0.075	-	0.075	-	tck
tdMDQSS ²	DM setup time to DQS	0.075	-	0.075	-	0.075	-	tck
tdMDQSH ²	DM hold time to DQS	0.075	-	0.075	-	0.075	-	tck
tdRL	Last data-in to read command	1	-	1	-	1	-	tck
tdPL	Last data-in to precharge	10	-	10	-	10	-	ns
trAS	RAS active time	45	100K	48	100K	50	100K	ns
trP	RAS precharge time	15	-	15	-	20	-	ns
trC	RAS cycle time	60	-	63	-	70	-	ns
trFC	Auto-refresh command cycle	75	-	80	-	80	-	ns
trCD	RAS to CAS delay	15/20	-	15/20	-	20	-	ns
trRD	RAS to RAS delay	2	-	2	-	2	-	tck
tCCD	CAS to CAS delay	1	-	1	-	1	-	tck
tMRD	Mode register set delay	2	-	2	-	2	-	tck
tpDEX	Power down exit time	10	-	10	-	10	-	ns
tsREX	Self-refresh exit time	200	-	200	-	200	-	ns
tr	Input transition time	0.5	-	0.5	-	0.5	-	ns
trEF	Refresh time	-	64	-	64	-	64	ms

Notes :

1. Data sampled at the rising edge of the clock : Addresses, CKE, /CS, /RAS, /CAS, /WE
2. Data sampled at both the rising edge and falling edge of data strobe : DQ, DM
3. tRCD=15ns/20ns each one represents different parts

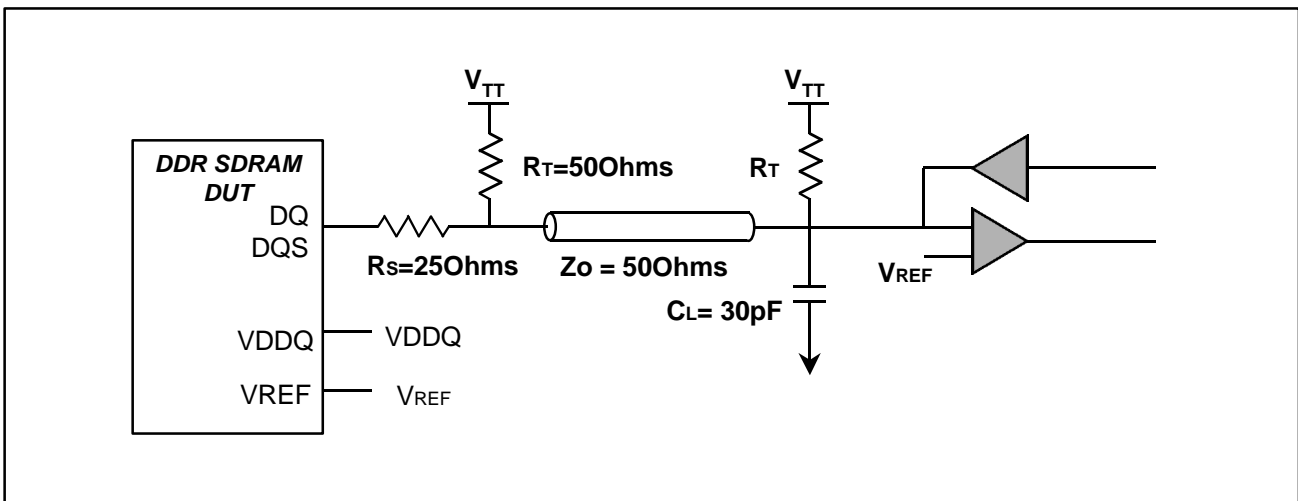
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AC CHARACTERISTICS II - TEST LOAD

(V_{DDQ}=2.5V, T_A = 0~70 °C)

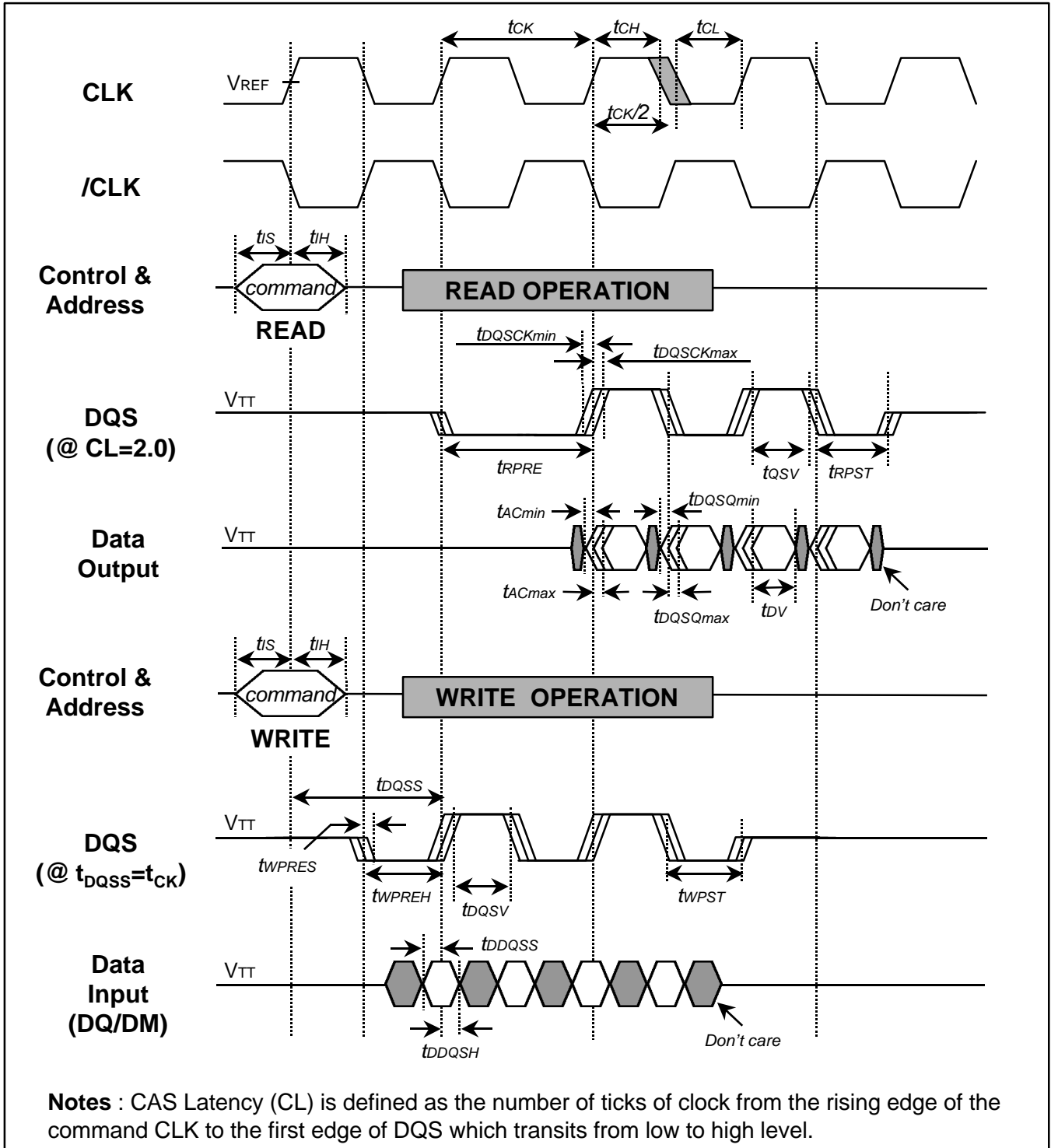
Parameter	Condition	Unit
Reference voltage, V _{REF}	V _{DDQ} x 0.5	Volts
Termination voltage, V _{TT}	V _{DDQ} x 0.5	Volts
Timing measurement reference level	V _{REF}	Volts
Input signal level	0.4 / 2.4	Volts
Input signal slew rate	1	V/ns
Output load	See test load circuits below	-

AC CHARACTERISTICS III - REFERENCE TEST LOAD CIRCUITS



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AC CHARACTERISTICS IV - TIMING DIAGRAM



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PACKAGE INFORMATION

Unit : mm(inch)

