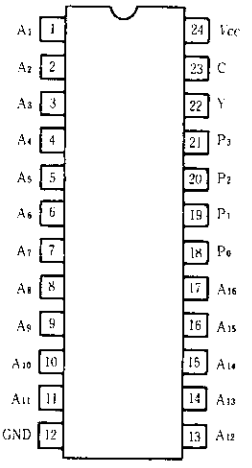
HD74HC678 ● 16-bit Address Comparator

The HD74HC678 address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A_1 through A_7 must be low and that inputs A_8 through A_{16} must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low. The HD74HC678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

■ PIN ARRANGEMENT

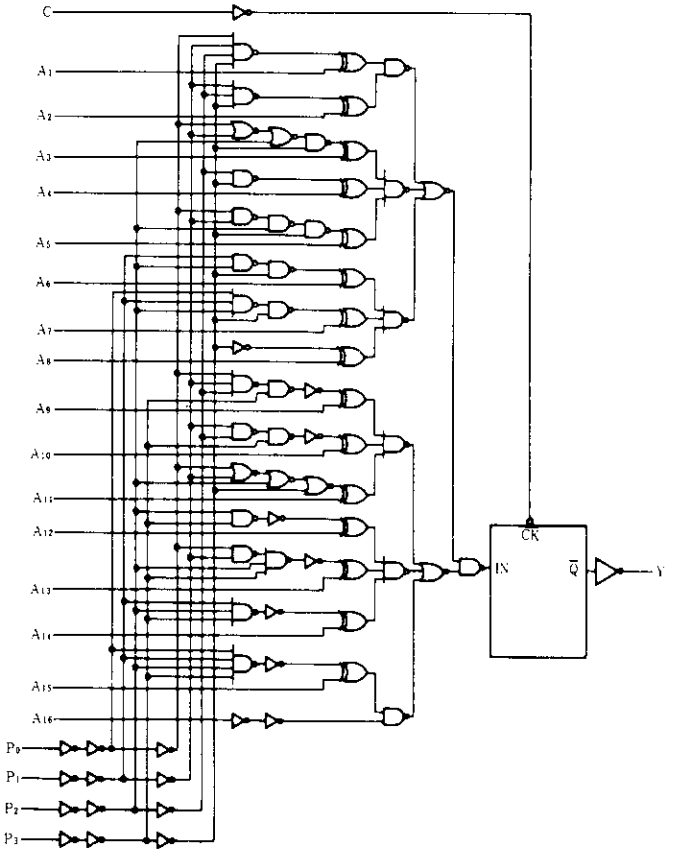


(Top View)

■ FEATURES

- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ LOGIC DIAGRAM



FUNCTION TABLE

	Inputs																			Output
C	P_3	P_2	P_1	P_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	Y
H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
H	All other combinations																				H
L	Any combination																				Latched

DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta = 25°C min	typ	max	Ta = −40~+85°C min	max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in} = V_{IH} or V_{IL}	I_{OH} = −20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH} = −4mA	4.18	—	—	4.13	—	
		6.0		I_{OH} = −5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in} = V_{IH} or V_{IL}	I_{OL} = 20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL} = 4mA	—	—	0.26	—	0.33	
		6.0		I_{OL} = 5.2mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in} = V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in} = V_{CC} or GND, I_{out} = 0 μA		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	P to Y	—	—	330	—	410	ns
		4.5		—	30	66	—	82	
		6.0		—	—	56	—	70	
	t_{PLH} t_{PHL}	2.0	A to Y	—	—	210	—	265	ns
		4.5		—	21	42	—	53	
		6.0		—	—	36	—	45	
	t_{PLH} t_{PHL}	2.0	C to Y	—	—	150	—	190	ns
		4.5		—	13	30	—	38	
		6.0		—	—	26	—	33	
Set up time	t_{su}	2.0	A to C	100	—	—	125	—	ns
		4.5		20	12	—	25	—	
		6.0		17	—	—	21	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	—	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF