LC²MOS High Speed µP-Compatible 8-Bit ADC with Track/Hold Function

AD7820

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS, microprocessor compatible 8-bit analog-to-digital converter which was a half-flash conversion technique to achieve a conversion time of 1.6µs. The converter has a 0V to +5V analog input voltage range with a single +5V supply.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	AD7820T(X)/883B
−2	AD7820U(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} to DGND	0V, +7V
Digital Input Voltage to GND (Pins 6-8, 13)	−0.3V, V_{DD}
Digital Output Voltage to GND (Pins 2-5, 14-18)	−0.3V, V_{DD}
V_{REF} (+) to GND	V_{REF} (−), V_{DD}
V_{REF} (−) to GND	0V, V_{REF} (+)
V_{IN} to GND	−0.3V, V_{DD}
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-20 and E-20A
θ_{JA} = 120°C/W for Q-20 and E-20A

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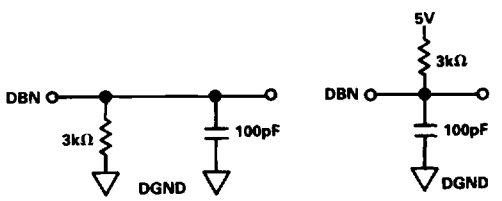
Table 1.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1, 2]	Units
Resolution	RES	−1, 2	8				This is the minimum resolution for which no missing codes are guaranteed.	Bits
Total Unadjusted Error[3]	TUE	−1	1	1	1			± LSB max
		−2	1/2	1	1/2	1/2		
Analog Input Leakage Current	I_{IN}	−1, 2	3	3	3			± μA max
Analog Input Capacitance	C_I	−1, 2	45					pF typ
Reference Input Resistance	R_I	−1, 2	1	1	1			kΩ min
			4	4	4			kΩ max
Digital Input High Level	V_{IH}	−1, 2	2.4	2.4	2.4		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	V min
			3.5	3.5	3.5		Mode (Pin 7)	
Digital Input Low Level	V_{IL}	−1, 2	0.8	0.8	0.8		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	V max
			1.5	1.5	1.5		Mode (Pin 7)	
Digital Input High Current	I_{IH}	−1, 2	1.0	1.0	1.0		$\overline{CS}$, $\overline{RD}$	μA max
			3.0	3.0	3.0		$\overline{WR}$	
			200.0	200.0	200.0		Mode (Pin 7)	
Digital Input Low Current	I_{IL}	−1, 2	1.0	1.0	1.0		$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ Mode (Pin 7)	− μA max
Digital Input Capacitance	C_I	−1, 2	8.0				$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ Mode (Pin 7)	pF max
Digital Output High Level	V_{OH}	−1, 2	4.0	4.0	4.0		DB0–DB7, $\overline{OFL}$, $\overline{INT}$ I_{SOURCE} = 360μA	V min
Digital Output Low Level	V_{OL}	−1, 2	0.4	0.4	0.4		DB0–DB7, $\overline{OFL}$, $\overline{INT}$ I_{SINK} = 1.6mA	V max
Digital Output Low Level	V_{OL}	−1, 2	0.4				RDY; I_{SINK} = 2.6mA	V max
Floating State Leakage Current	I_{OUT}	−1, 2	3.0	3.0	3.0		DB0–DB7	μA max
Digital Output Capacitance	C_{OUT}	−1, 2	8.0				(Typically 5pF)	pF max
Slew Rate, Tracking		−1, 2	0.1					V/μs
Supply Current from V_{DD}	I_{DD}	−1, 2	15.0	20.0	20.0		$\overline{CS}$ = $\overline{RD}$ = 0V	mA max
Power Supply Sensitivity		−1, 2	1/4	1/4	1/4		V_{DD} = 5V ± 5%	± LSB max
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time	t_{CS}	−1, 2	0					ns min
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Hold Time	t_{CH}	−1, 2	0					ns min
$\overline{CS}$ to RDY Delay. Pull-Up Resistor 2kΩ[4]	t_{RDY}	−1, 2	100				70ns max at +25°C	ns max
Conversion Time ($\overline{RD}$ Mode)	t_{CRD}	−1, 2	2.5	1.6	2.5			μs max
Data Access Time ($\overline{RD}$ Mode)[5]	t_{ACCO}	−1, 2	t_{CRD} + 50				(t_{CRD} + 20) ns max at +25°C	ns max
$\overline{RD}$ to INT Delay ($\overline{RD}$ Mode)[4]	t_{INTH}	−1, 2	225				175ns max at +25°C	ns max
Data Hold Time[6]	t_{DH}	−1, 2	100				60ns max at +25°C	ns max
Delay Time Between Conversions	t_P	−1, 2	600				500ns min at +25°C	ns min
Write Pulse Width	t_{WR}	−1, 2	600					ns max
			50					ns max
Delay Time Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}	−1, 2	700				600ns max at +25°C	ns min
Data Access Time[5] ($\overline{WR}$/$\overline{RD}$ Mode, See Fig. 4)	t_{ACC1}	−1, 2	250				160ns max at +25°C	ns max
$\overline{RD}$ to $\overline{INT}$ Delay	t_{R1}	−1, 2	225				140ns max at +25°C	ns max
$\overline{WR}$ to $\overline{INT}$ Delay[4]	t_{INTL}	−1, 2	1700				1000ns max at +25°C	ns max

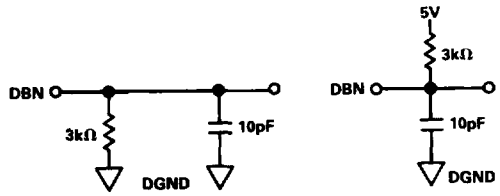
Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Data Access Time[5] ($\overline{WR}$/$\overline{RD}$ Mode, See Fig. 3)	t_{ACC2}	−1, 2	110				70ns max at +25°C	ns max
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)[4]	t_{IHWR}	−1, 2	150				100ns max at +25°C	ns max
Data Access Time after $\overline{INT}$ (Stand-Alone Operation)	t_{ID}	−1, 2	75				50ns max at +25°C	ns max

NOTES
[1]V_{DD} = +5V; $V_{REF}(+)$ = +5V; $V_{REF}(-)$ = GND = 0V unless otherwise specified. Specifications apply for $\overline{RD}$ mode (Pin 7 = 0V).
[2]All input control signals are specified with $t_r = t_f$ = 20ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
[3]Includes gain error, offset error and linearity error.
[4]C_L = 50pF.
[5]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[6]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.



a. High-Z to V_{OH} b. High-Z to V_{OL}

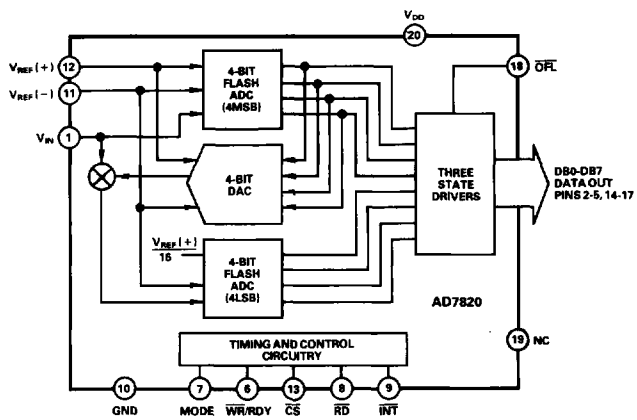
Figure 1. Load Circuits for Data Access Time Test



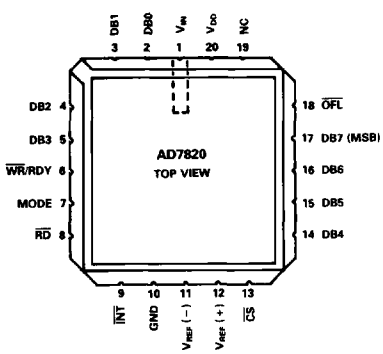
a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

3.2.1 Functional Block Diagram and Terminal Assignments.



E Package (LCC)

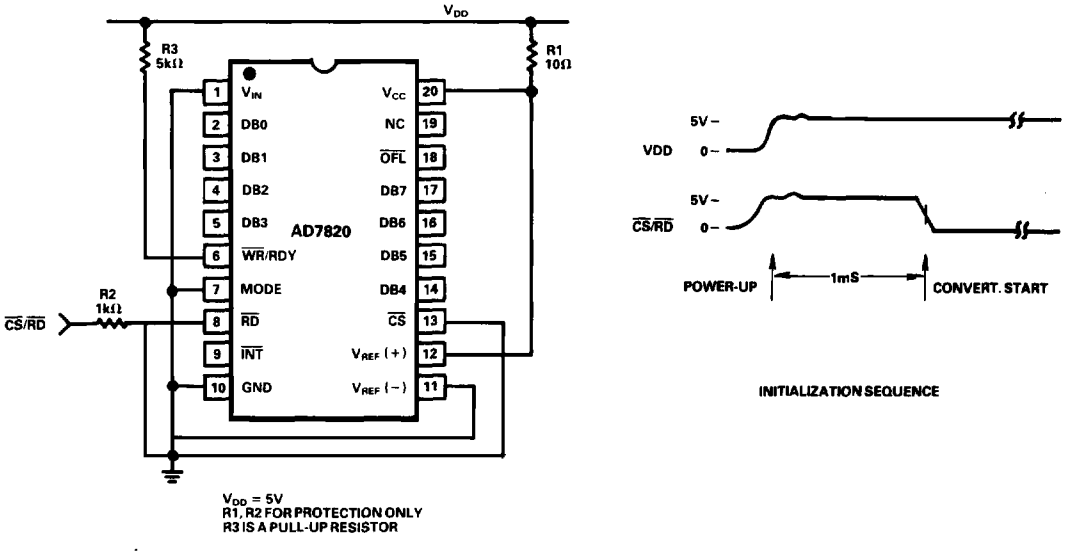


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



5.0 Digital Interface.

The AD7820 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low the converter is in the RD mode, with this pin high the AD7820 is set up for the WR-RD mode.

5.1 WR-RD Mode.

In the WR-RD mode, pin 6 is configured as the WRITE input for the AD7820. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 3). $\overline{INT}$ typically goes low 700ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0-DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

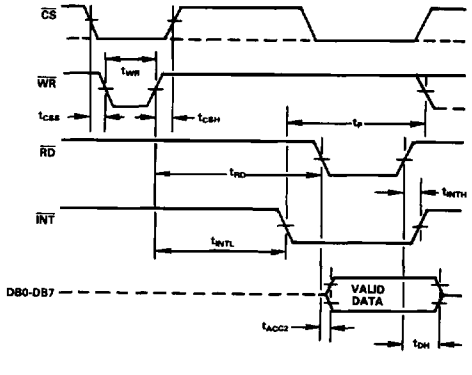


Figure 3. WR-RD Mode (t_{RD}>t_{INTL})

The alternative option can be used to shorten the conversion time. To achieve this, the status of the $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low 600ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data outputs (DB0-DB7). $\overline{INT}$ also goes low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 4.

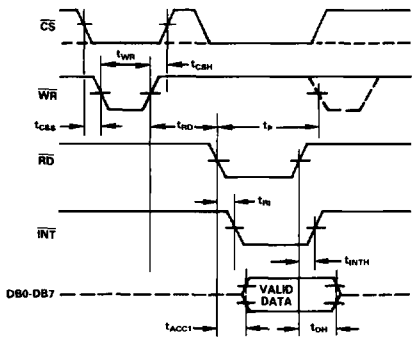


Figure 4. WR-RD Mode ($t_{RD}>t_{INTL}$)

5.2 RD Mode.

The timing diagram for the RD mode is shown in Figure 5. In the RD mode configuration, conversion is initiated by taking $\overline{RD}$ low. The $\overline{RD}$ line is then kept low until output data appears. It is very useful with microprocessors which can be forced into a WAIT state, with the microprocessor starting a conversion, waiting, and then reading data with a single READ instruction. In this mode, pin 6 of the AD7820 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low at the completion of conversion. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

The AD7820 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid typically 700ns after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 6.

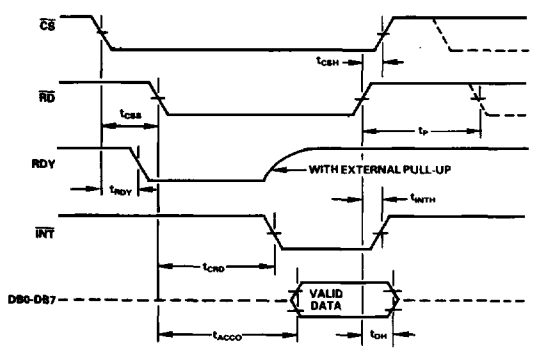


Figure 5. RD Mode

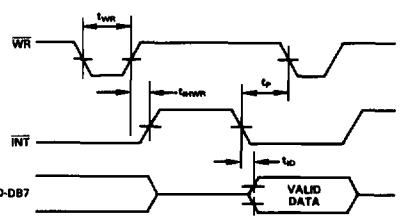


Figure 6. WR-RD Mode Stand-Alone Operation, $\overline{CS}=\overline{RD}=0$