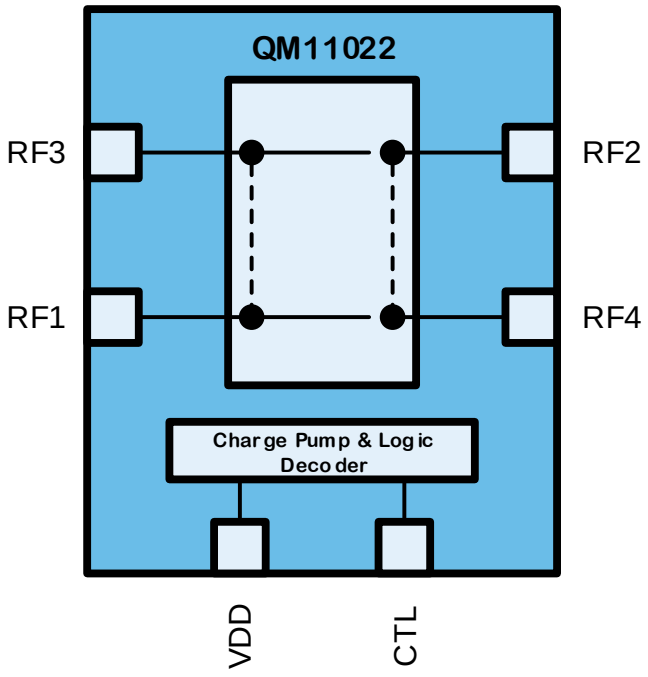
QM11022

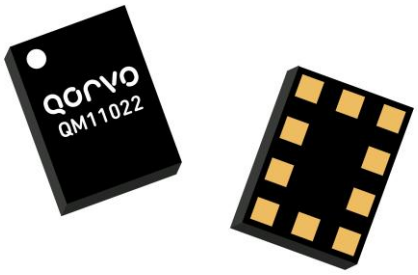
General Purpose DPDT Transfer Switch

Product Description

The QM11022 is a dual-pole double-throw transfer switch designed for general purpose switching applications where RF port transfer (port swapping) control is needed. The low insertion loss along with excellent linearity performance makes the QM11022 ideal for multi-mode GSM, EDGE, UMTS, and LTE handset applications. The RF ports can be directly connected in 50Ω systems and control logic is compatible with 1.3V to 2.7V systems. The supply voltage is intended for connection to 2.8V systems but the device is operable from 2.4V to 5.5V. The compact 1.1mm x 1.5mm size offers mobile handset designers an easy-to-use switch component for quick integration into multimode, multi-band systems.

Functional Block Diagram





10 Pin 1.1 x 1.5 x 0.59 mm Package

Feature Overview

- Low Insertion Loss
- High Port-to-Port Isolation
- GPIO Interface for 1.3V to 2.7V Control Logic
- Broadband Performance Suitable for All Cellular Modulation Schemes up to 6GHz
- Very Low Current Consumption
- Linearity and Harmonic Performance Ideally Suited for LTE Applications
- DC blocking capacitors are not required in typical applications

Applications

- Cellular Handset Applications
- Cellular Modems and USB Devices
- Multi-Mode GSM, EDGE, WCDMA, and LTE Applications

Ordering Information

PART NO.	DESCRIPTION
QM11022SB	5-pc Sample Bag
QM11022SR	100-pc, 7” Reel
QM11022TR13-5K	5000-pc, 13” Reel
QM11022PCK	Fully Assembled EVB

Absolute Maximum Ratings

PARAMETER	RATING
Storage Temperature	-65 to +150 °C
Operating Temperature	-30 to +90°C
V_{DD}	6.0 V
C_{TL1}	3.0 V
Maximum Input Power	
Momentary Infrequent Occurrence	39 dBm, 1:1 VSWR, +90°C, 25% DC
Continuous Operation	37.5 dBm, 1:1 VSWR, +25°C, 25% DC 36.5 dBm, 1:1 VSWR, +90°C, 25% DC

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD} Supply Voltage	2.4	2.8	5.5	V
V_{DD} Supply Current		57	80	µA
C_{TL} Logic Low Voltage	0.00	0.00	0.45	V
C_{TL} Logic High Voltage	1.3	1.8	2.7	V
C_{TL} Logic High Current		0.1	5	µA
Turn-On Time (50%V_{DD} to 90% RF)			20	µs
Switching Speed (IL Based, 10% to 90%)		1.8	3	µs

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

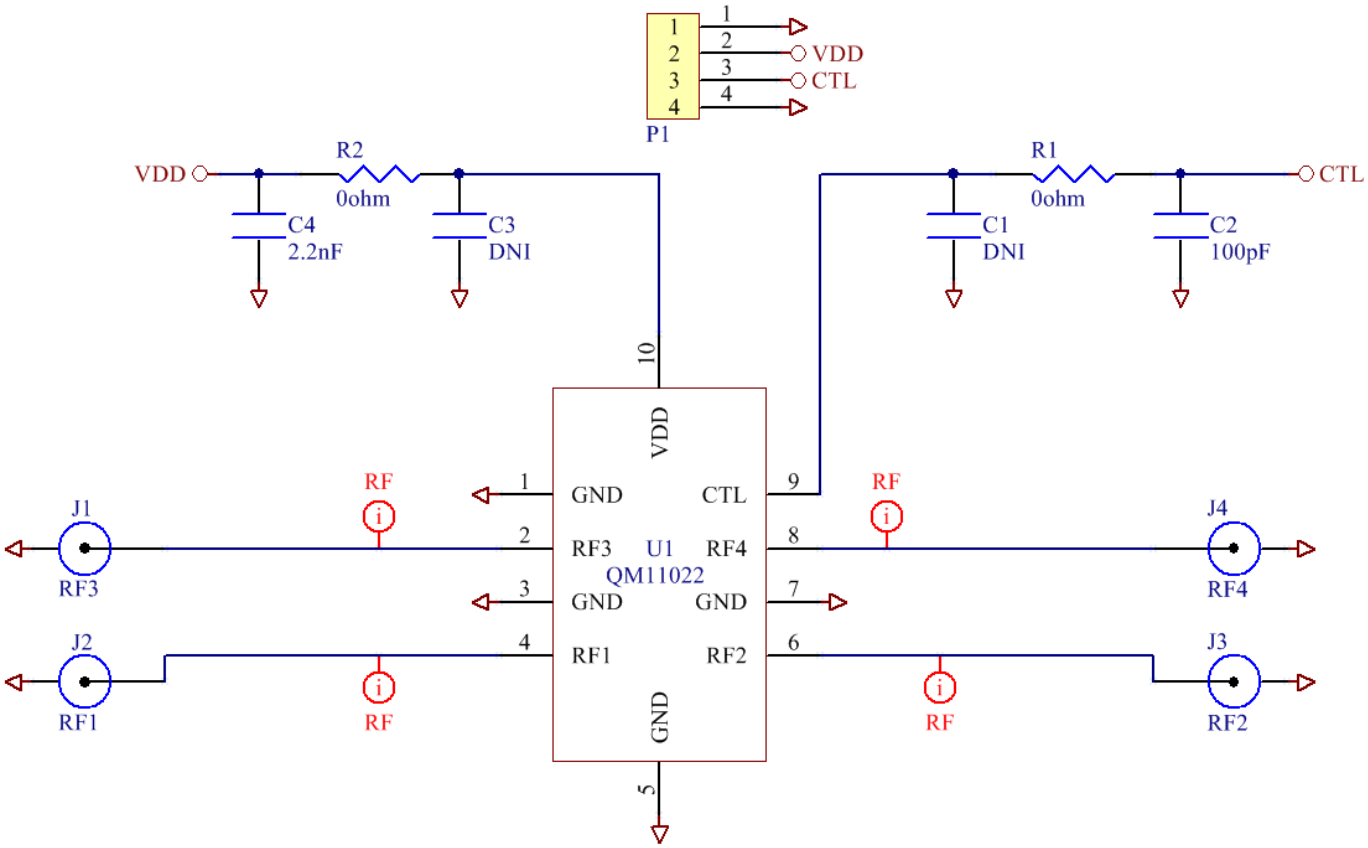
Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{DD} = 2.8V, Logic State = RF1-RF4; RF2-RF3 and RF1-RF3; RF2-RF4

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Frequency Range		600		960	MHz
Insertion Loss					
RF1 to RF3	Logic State = RF1-RF3, RF2-RF4		0.27		dB
RF1 to RF4	Logic State = RF1-RF4, RF2-RF3		0.27		dB
RF2 to RF3	Logic State = RF1-RF4, RF2-RF3		0.28		dB
RF2 to RF4	Logic State = RF1-RF3, RF2-RF4		0.26		dB
Isolation					
RF1 to RF2, RF3 to RF4	Logic State = RF1-RF4, RF2-RF3		34		dB
RF1 to RF2, RF3 to RF4	Logic State = RF1-RF3, RF2-RF4		35		dB
Harmonics					
2nd Harmonic	Frequency = 824MHz to 915MHz; Pin = 26dBm; CW		-90		dBm
3nd Harmonic			-81		dBm
Up to 12.75GHz			-115		dBm
2nd Harmonic (B13)	Frequency = 786.5MHz; Pin = 26dBm; CW		-87		dBm
2nd Harmonic	Frequency = 824MHz; Pin = 35dBm; CW		-68		dBm
3rd Harmonic			-53		dBm
IIP2	F1 = 26dBm; F2 = -20dBm				
Band 5 & 6	F1 = 836.5MHz; F2 = 1718MHz; Rx Freq = 881.5MHz		132		dBm
IIP3	F1 = 20dBm; F2 = -15dBm				
Band 5 & 6	F1 = 836.5MHz; F2 = 791.5MHz; Rx Freq = 881.5MHz		77		dBm
VSWR					
RF1, RF2, RF3, RF4	824MHz to 960MHz		1.06		:1

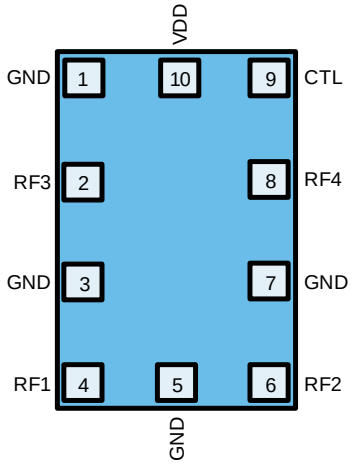
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Frequency Range		1425		2200	MHz
Insertion Loss					
RF1 to RF3	Logic State = RF1-RF3, RF2-RF4		0.30		dB
RF1 to RF4	Logic State = RF1-RF4, RF2-RF3		0.31		dB
RF2 to RF3	Logic State = RF1-RF4, RF2-RF3		0.32		dB
RF2 to RF4	Logic State = RF1-RF3, RF2-RF4		0.30		dB
Isolation					
RF1 to RF2, RF3-RF4	Logic State = RF1-RF4, RF2-RF3		27		dB
RF1 to RF2, RF3-RF4	Logic State = RF1-RF3, RF2-RF4		27		dB
Harmonics					
2nd Harmonic	Frequency = 1710MHz to 1910MHz; P_{in} = 26dBm; CW		-80		dBm
3nd Harmonic			-79		dBm
Up to 12.75GHz			-122		dBm
2nd Harmonic	Frequency = 1910MHz; P_{in} = 33dBm; CW		-69		dBm
3nd Harmonic			-56		dBm
IIP2	F1 = 26dBm; F2 = -20dBm				
Band II (PCS)	F1 = 1880MHz; F2 = 3840MHz; Rx Freq = 1960MHz		127		dBm
IIP3	F1 = 20dBm; F2 = -15dBm				
Band 2 (PCS)	F1 = 1880MHz; F2 = 1800MHz; Rx Freq = 1960MHz		76		dBm
Band 1 (IMT)	F1 = 1950; F2 = 1760MHz; Rx Freq = 2140MHz		74		dBm
VSWR					
RF1, RF2, RF3, RF4	1427MHz to 2170MHz		1.1		:1
Frequency Range		2300		2690	MHz
Insertion Loss					
RF1 to RF3	Logic State = RF1-RF3, RF2-RF4		0.33		dB
RF1 to RF4	Logic State = RF1-RF4, RF2-RF3		0.34		dB
RF2 to RF3	Logic State = RF1-RF4, RF2-RF3		0.36		dB
RF2 to RF4	Logic State = RF1-RF3, RF2-RF4		0.33		dB
Isolation					
RF1 to RF2, RF3-RF4	Logic State = RF1-RF4, RF2-RF3		25		dB
RF1 to RF2, RF3-RF4	Logic State = RF1-RF3, RF2-RF4		25		dB
Harmonics					
2nd Harmonic	Frequency = 2500MHz to 2570MHz; P_{in} = 26dBm; CW		-78		dBm
3nd Harmonic			-76		dBm
IIP2	F1 = 20dBm; F2 = -15dBm				
Band 7	F1 = 2535MHz; F2 = 120MHz; Rx Freq = 2655MHz		128		dBm
IIP3	F1 = 20dBm; F2 = -15dBm				
Band 7	F1 = 2535MHz; F2 = 2415MHz; Rx Freq = 2655MHz		73		dBm
VSWR					
RF1, RF2, RF3, RF4	2300MHz to 2690MHz		1.1		:1

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Frequency Range		3400		3800	MHz
Insertion Loss					
RF1 to RF3	Logic State = RF1-RF3, RF2-RF4		0.42		dB
RF1 to RF4	Logic State = RF1-RF4, RF2-RF3		0.41		dB
RF2 to RF3	Logic State = RF1-RF4, RF2-RF3		0.45		dB
RF2 to RF4	Logic State = RF1-RF3, RF2-RF4		0.39		dB
Isolation					
RF1 to RF2, RF3-RF4	Logic State = RF1-RF4, RF2-RF3		21		dB
RF1 to RF2, RF3-RF4	Logic State = RF1-RF3, RF2-RF4		21		dB
VSWR					
RF1, RF2, RF3, RF4	3400MHz to 3800MHz		1.2		:1
Frequency Range		5000		6000	MHz
Insertion Loss					
RF1 to RF3	Logic State = RF1-RF3, RF2-RF4		0.55		dB
RF1 to RF4	Logic State = RF1-RF4, RF2-RF3		0.51		dB
RF2 to RF3	Logic State = RF1-RF4, RF2-RF3		0.61		dB
RF2 to RF4	Logic State = RF1-RF3, RF2-RF4		0.55		dB
Isolation					
RF1 to RF2, RF3-RF4	Logic State = RF1-RF4, RF2-RF3		19		dB
RF1 to RF2, RF3-RF4	Logic State = RF1-RF3, RF2-RF4		18		dB
VSWR					
RF1, RF2, RF3, RF4	5000MHz to 6000MHz		1.3		:1

Application Circuit Schematic



Pin Configuration and Description



Top View

PIN NO.	LABEL	DESCRIPTION
1	GND	Ground
2	RF3	RF Port connecting to either RF1 or RF2. Avoid applying DC voltage
3	GND	Ground
4	RF1	RF Port connecting to either RF3 or RF4. Avoid applying DC voltage
5	GND	Ground
6	RF2	RF Port connecting to either RF3 or RF4. Avoid applying DC voltage
7	GND	Ground
8	RF4	RF Port connecting to either RF1 or RF2. Avoid applying DC voltage
9	C_{TL}	Logic Control pin
10	V_{DD}	Power Supply pin

Control Logic

The Switch is controlled by V_{DD} and C_{TL}.

LOGIC STATE	V_{DD}	C_{TL}	DESCRIPTION
Off	0V	Low	Off or Standby – low current state
RF1-RF3;RF2-RF4	"V_{DD}"	Low	RF1 connected to RF3 and RF2 connected to RF4
RF1-RF4;RF2-RF3	"V_{DD}"	High	RF1 connected to RF4 and RF2 connected to RF3

NOTE: The switch is in the Off or Standby state only when the V_{DD} supply is low. The RF performance is undefined in the Off State

Power On and Off Sequence

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the part. First apply V_{DD} before applying a high to C_{TL}.

Power On –

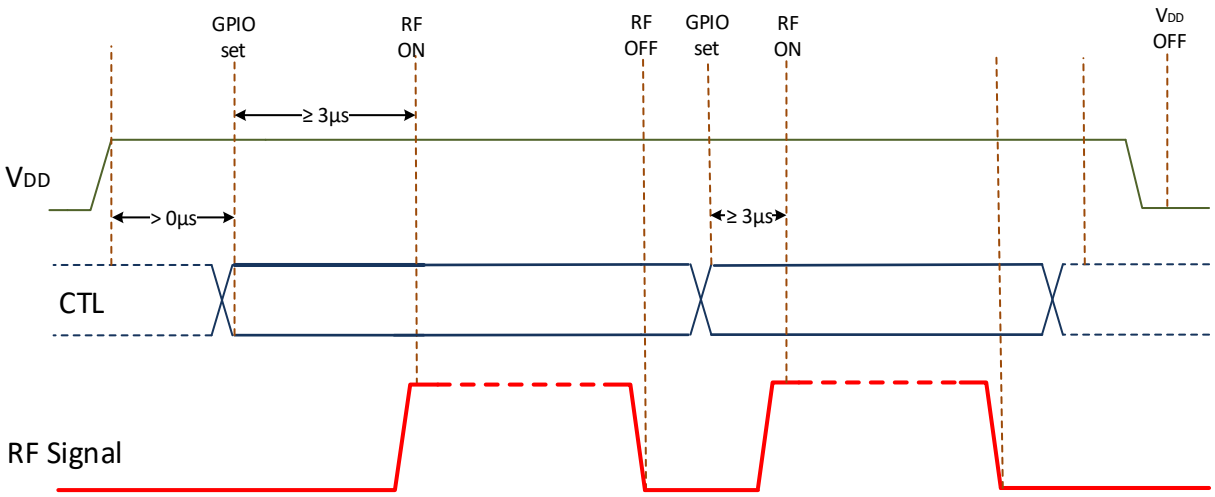
1. Apply voltage supply – V_{DD}
2. Apply Logic signal – C_{TL}
3. Wait 5µs or greater and then apply the RF signal

Changing Switch Position

1. Remove RF
2. Change control voltage – C_{TL}
3. Wait 5µs or greater and then apply the RF signal

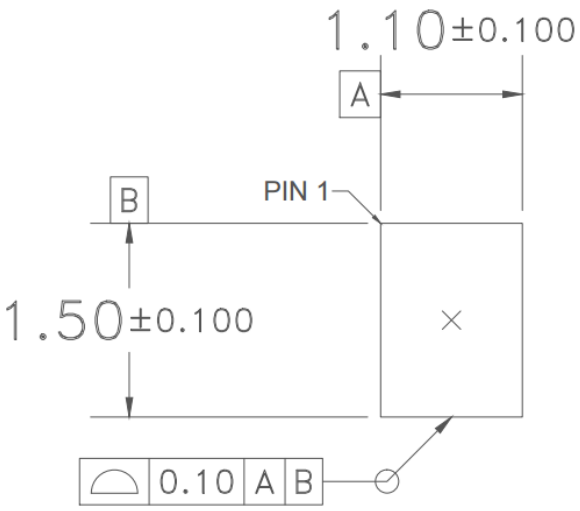
Power Off –

1. Remove the RF signal
2. Remove the logic signal – C_{TL}
3. Remove the voltage supply – V_{DD}

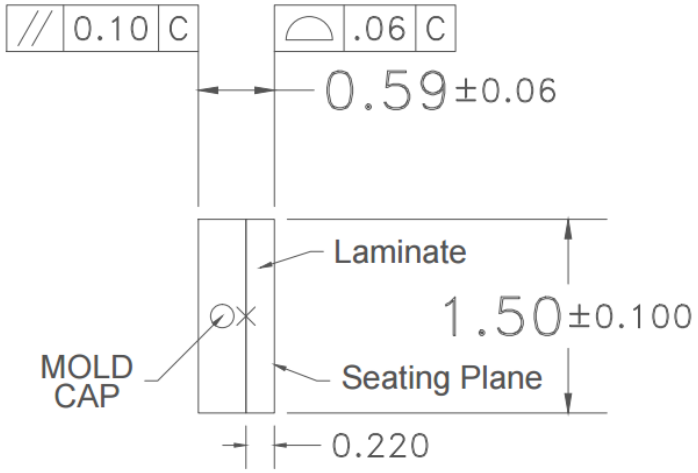


Mechanical Information

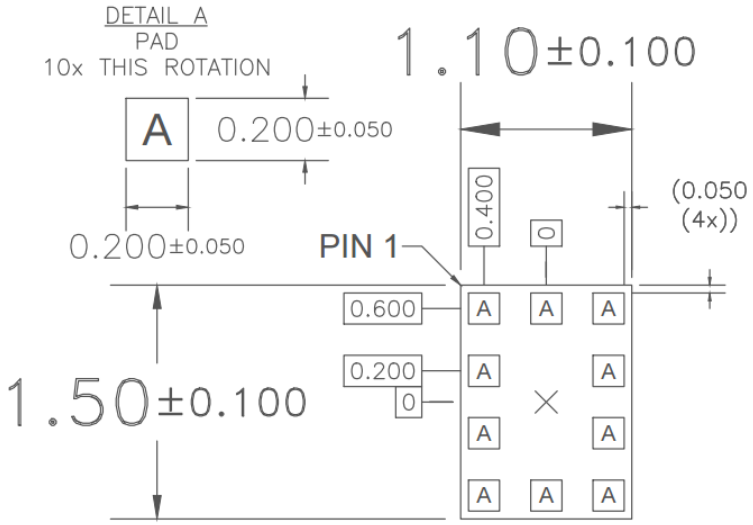
Package Drawing

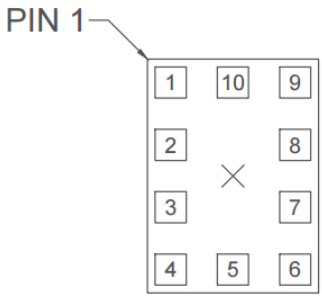


Top View



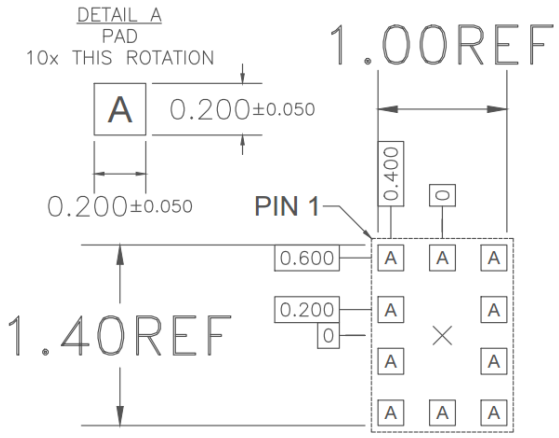
Side View



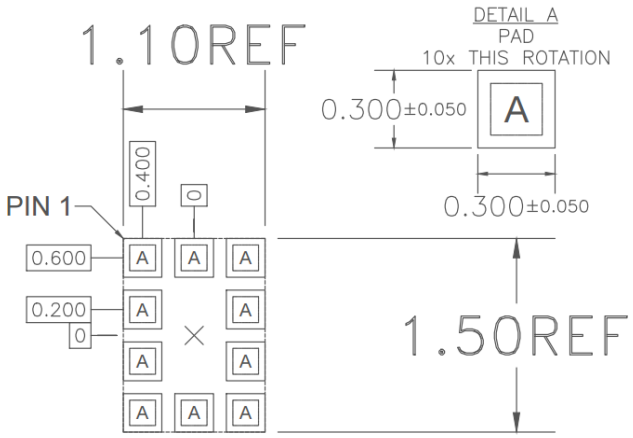


Top View xRay

PCB Design Requirements



Recommended Land Pattern

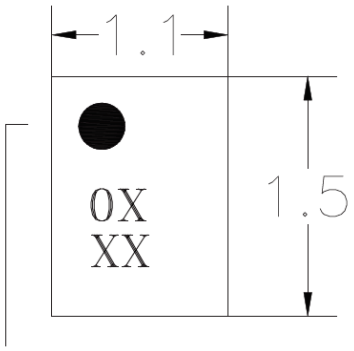


Recommended Land Pattern Mask

Notes:

1. All dimensions are in milimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

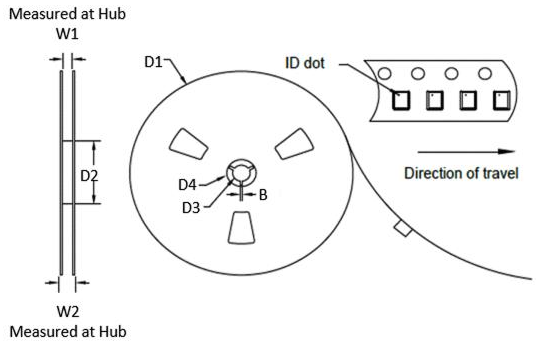
Branding Diagram

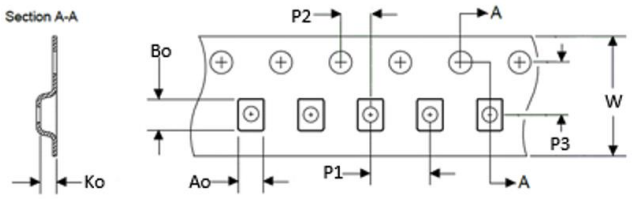


Pin 1 Indicator
0XXX
"0" is the one digit product code
"XXX" is the 3 digit Trace Code
assigned by sub-con

Unit: mm

Tape and Reel Information





Feature	Measure	Symbol	Size (mm)
Flange	Diameter	D1	330.0
	Thickness	W2	14.2
	Space Between Flange	W1	8.8
Hub	Outer Diameter	D2	102.0
	Arbor Hole Diameter	D3	13.0
	Key Slit Width	B	2.0
	Key Slit Diameter	D4	20.2

Feature	Measure	Symbol	Size (mm)
Cavity	Length	Ao	1.3
	Width	Bo	1.7
	Depth	Ko	0.74
	Pitch	P1	4.0
Centerline Distance	Cavity to Perforation (Length)	P2	2.0
	Cavity to Perforation (Width)	P3	3.5
Carrier Tape	Width	W	8.0

(Unless otherwise specified, all dimension tolerances per EIA-481)

Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 2	ESDA/JEDEC JS-001-2012
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Revision History

Revision Code	Date	Comments
A	6/30/2016	Initial Production Release
B	8/19/2016	Updated Functional Block Diagram
C	9/21/2016	Updated Performance Data
D	10/20/2016	Fixed Typo in CDM ESD Rating
F	2/17/2017	Updated Isolations
H	5/25/2017	Fixed Typo in Isolation States; updated Pin locations on functional block diagram
I	6/07/2017	Updated Timing Diagram
J	7/18/2018	Updated PCB part number
K	4/03/2019	Updated Timing Diagram
L	6/25/2019	Fixed typo on Functional Block Diagram, added Branding Diagram and T&R info

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
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