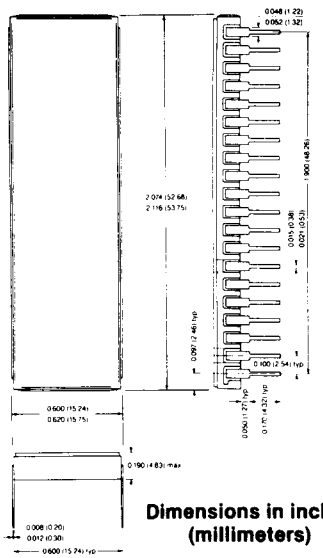
MICRO NETWORKS

MN7208
MN7216

DATA ACQUISITION SYSTEM
FRONT-END

FEATURES

- **Complete DAS Front End:**
  Analog Input Multiplexer
  Instrumentation Amplifier
  Load/Sequence Control Logic
- **Small 40-Pin DIP**
- **16-Single-Ended or 8-Differential Input Channels**
- **10μsec Channel Switching and In-Amp Settling Time**
- **Full Mil Operation −55°C to +125°C**
- **Use with MN6000 Series Sampling A/D Converters for Multi-Channel Digitizing**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**



Dimensions in inches (millimeters)

DESCRIPTION

The MN7208 and MN7216 are thin-film hybrid circuits containing two 8-channel multiplexers, random and sequential address control logic and a precision instrumentation amplifier. This DAS front-end function is packaged in a 40-pin side-brazed DIP and can be used with Micro Networks MN6000 Series of sampling A/D converters to configure a complete, 16-channel single-ended or an 8-channel full differential data acquisition system in as few as 2 dual in-line packages. Extremely versatile, the MN7208/7216 can be used in a wide variety of multi-channel data acquisition applications.

The multiplexer section of the MN7208 and MN7216 features over voltage protected analog inputs and break-before-make channel switching. The internal control logic allows both random and sequential channel addressing. The precision instrumentation amplifier's fast settling time and internal gain setting resistors combine to offer high-speed and precision gain accuracy and low drift.

Channel access and settling time for both the MN7208 and MN7216 to ±0.01% for a 20V step is 10μsec maximum. These devices, when used with the MN6774 12-Bit, 100kHz sampling A/D converter, can be configured into a μP-interfaced 12-Bit, 50kHz data acquisition system (multi-channel A/D) complete with multiplexer, instrumentation amplifier, T/H amplifier, A/D converter and all interface and address decode logic.

The MN7208 and MN7216 have been designed to offer the user maximum flexibility when designing for multi-channel data conversion applications where small size and physical/electrical compatibility are paramount considerations. Standard devices are specified fully for 0°C to +70°C (J and K models) or −55°C to +125°C (S and T models) operation. For military/aerospace or harsh-environment industrial applications, "S" and "T" models are available with environmental stress screening. Contact factory for availability of fully compliant MIL-H-38534 devices.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN7208/MN7216 DATA ACQUISITION SYSTEM FRONT-END

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN7208J, K; MN7216J, K	0°C to +70°C
MN7208S, S/B, T, T/B	−55°C to +125°C
MN7216S, S/B, T, T/B	−55°C to +125°C
Positive Supply (+V_{CC}, Pin 28)	0 to +18 Volts
Negative Supply (−V_{CC} Pin 24)	0 to −18 Volts
Logic Supply (+V_{DD}, Pin 34)	−0.5 to +7 Volts
Analog Inputs:	
CH_0 — CH_{15} (Pins 1-16)	±V_{CC} ±20 Volts
−RG, G500, +Amp, −Amp, G10 (Pins 17-20, 23)	±V_{CC}
Digital Inputs:	
Address Inputs (Pins 37-40)	0 to +7 Volts
Load, Reset, Clock (Pins 27, 36, 35)	0 to +7 Volts
MUX Enable (Pin 25)	0 to +7 Volts

ORDERING INFORMATION

PART NUMBER **MN7208 T/B CH**

- Select 8-channel differential (MN7208) or 16-channel single-ended (MN7216) model.
- Select suffix J,K,S or T for desired performance and specified temperature range.
- Add "/B" suffix to "S" or "T" models for Environmental Stress Screening.
- Add "CH" suffix to "S/B" or "T/B" models for MIL-H-38534 compliant devices.

Contact factory for availability of "CH" device types.

SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V unless otherwise noted)

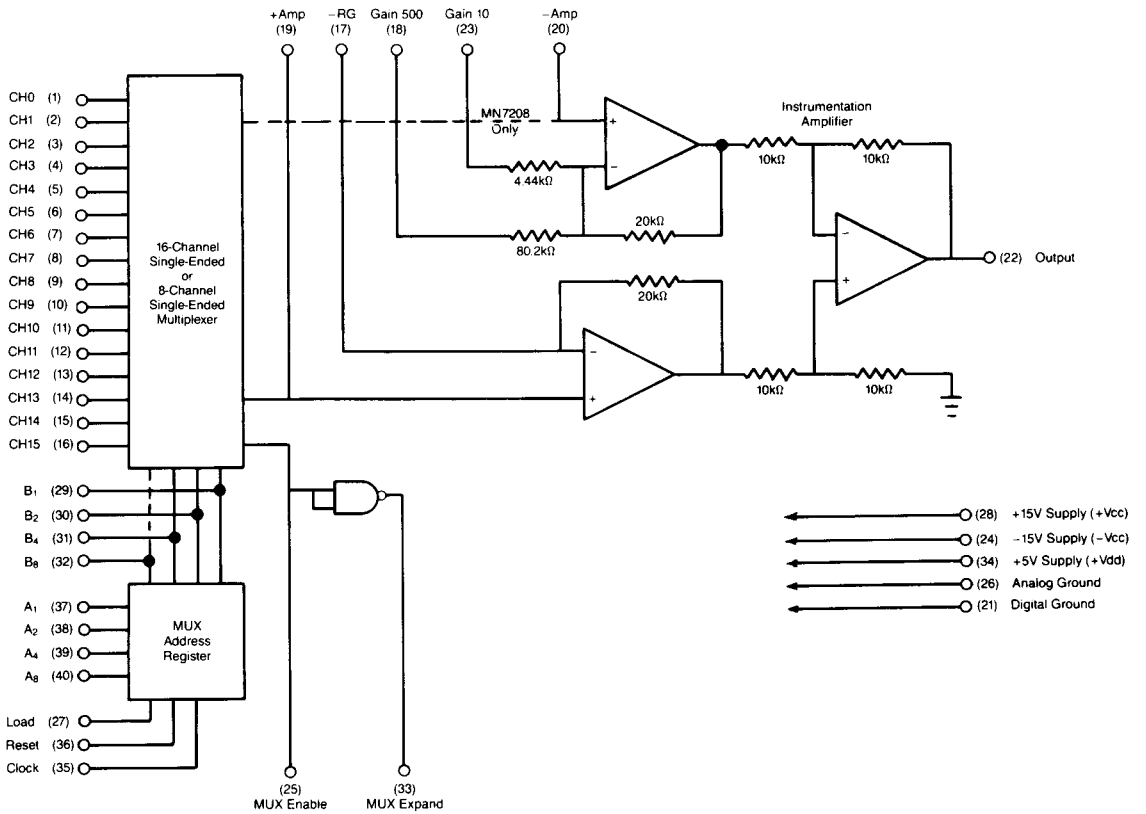
ANALOG INPUTS (Multiplexer Inputs)	MIN.	TYP.	MAX.	UNITS
Voltage Range: Single-Ended (MN7216)		±10		Volts
Differential (MN7208)		±10		Volts
Common Mode	±10	±12		Volts
Input Impendance: Single-Ended (MN7216)		5//6		mΩ/pF
Differential (MN7208)		2//1		mΩ/pF
DIGITAL INPUTS (MUX Address, Load, Reset, Clock, MUX Enable)				
Logic Levels: MUX Enable (Note 2): Logic "1"	+4.0			Volts
Logic "0"			+0.8	Volts
MUX Address, Load, Reset, Clock: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: MUX Enable (Note 2): Logic "1" (V_{IH} = 4.0V)			−1	mA
Logic "0" (V_{IL} = 0.4V)			−4.6	mA
MUX Address, Load, Reset, Clock: Logic "1" (V_{IH} = 2.4V)			+20	μA
Logic "0" (V_{IL} = 0.4V)			−0.4	mA
ANALOG OUTPUT (Instrumentation Amplifier)				
Output Voltage	±10	±12		Volts
Output Current	±5	±25		mA
Capacitive Load (Stability)		5000		pF
DYNAMIC CHARACTERISTICS				
Large Signal Bandwidth		270		kHz
Output Slew Rate		17		V/μsec
Settling Time (20V Step to ±0.01%, G=1)		7	10	μsec
POWER SUPPLIES				
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
−15 Supply	−14.55	−15	−15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Current Drains: +15V Supply		+4	+7	mA
−15V Supply		−3	−6	mA
+5V Supply		+28	+35	mA
Power Consumption		245	370	mW

TRANSFER CHARACTERISTICS	J	K	S	T	UNITS
Offset Error (Max): Initial G=1	±5	±5	±5	±5	mV
(RTI) G=10	±0.5	±0.5	±0.5	±0.5	mV
G=500	±200	±200	±200	±200	μV
Over Temperature (Note 3): G=1	±10	±5	±10	±5	mV
G=10	±1	±0.5	±1	±0.5	mV
G=500	±400	±200	±400	±200	μV
Offset Drift (Max): G=1	±100	±50	±100	±50	μV/°C
(RTI) G=10	±70	±35	±70	±35	μV/°C
G=500	±10	±5	±10	±5	μV/°C
Gain Error (Max, Note 5) Initial: G=1	±0.04	±0.04	±0.04	±0.04	%
G=10	±0.05	±0.05	±0.05	±0.05	%
G=500	±0.05	±0.05	±0.05	±0.05	%
Over Temperature (Note 3): G=1	±0.08	±0.04	±0.08	±0.04	%
G=10	±0.10	±0.05	±0.10	±0.05	%
G=500	±0.10	±0.05	±0.10	±0.05	%
Gain Drift (Max): G=1	±20	±10	±20	±10	ppm/°C
G=10	±20	±10	±20	±10	ppm/°C
G=500	±20	±10	±20	±10	ppm/°C
Gain Nonlinearity (Max, Note 4) (G=1): Initial	±0.005	±0.003	±0.005	±0.003	%FSR
Over Temperature (Note 3)	±0.01	±0.006	±0.01	±0.006	%FSR

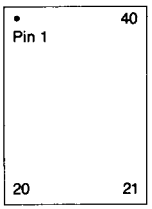
NOTES:

1. System specifications listed reflect the performance of both the multiplexer and instrumentation amplifier serially connected.
2. Internal 1K resistor connected to +5V for operation with standard TTL logic.
3. J and K models specified for 0°C to +70°C operation. S and T models specified for −55°C to +125°C operation.
4. Gain linearity error is defined as the maximum deviation from the best-fit straight line approximation to the system's input-output transfer function and is expressed as a percentage of the system's full scale voltage swing (FSR).
5. Gain error is defined as the error in the slope of the system's input-output transfer function and is expressed in percent.

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Channel 0	40	Address Input A_1
2	Channel 1	39	Address Input A_2
3	Channel 2	38	Address Input A_4
4	Channel 3	37	Address Input A_8
5	Channel 4	36	Reset
6	Channel 5	35	Clock
7	Channel 6	34	+5V Supply (+Vdd)
8	Channel 7	33	MUX Expand
9	Channel 8	32	Address Output B_8
10	Channel 9	31	Address Output B_4
11	Channel 10	30	Address Output B_2
12	Channel 11	29	Address Output B_1
13	Channel 12	28	+15V Supply (+Vcc)
14	Channel 13	27	Load
15	Channel 14	26	Analog Ground
16	Channel 15	25	MUX Enable
17	−RG	24	−15V Supply (−Vcc)
18	Gain 500	23	Gain 10
19	+Amp	22	Output
20	−Amp	21	Digital Ground

APPLICATIONS INFORMATION

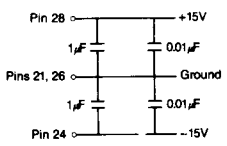
DESCRIPTION OF OPERATION — The MN7208 and MN7216 are data acquisition system building blocks. Each device contains an analog input multiplexer, address decode control logic circuitry and an instrumentation amplifier. The MN7208 provides an eight channel differential input multiplexer, while the MN7216 provides 16 single-ended inputs. Control logic circuitry enables either random or sequential channel addressing. Multiplexer outputs are connected internally to the instrumentation amplifier inputs. The instrumentation amplifier can be configured in gains of 1, 10 and 500 via the internal gain setting resistors or set to any user defined value with the use of external resistors.

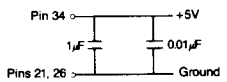
LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified performance from the MN7208/7216. The unit's analog and digital ground pins are not connected to each other internal to the device, therefore, they should be tied together outside the device package and connected to system analog ground through a large ground plane beneath the unit.

Coupling between analog inputs and digital signals should be minimized to avoid noise pickup. Care should be taken to avoid long runs or runs close to digital lines.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1uF tantalum capacitors in parallel with 0.01μF ceramic capacitors can be used if necessary to conserve board space.

POWER SUPPLY DECOUPLING





MULTIPLEXER AND CONTROL LOGIC — The Load (pin 27) input controls the random or sequential mode of operation. If Load Input (pin 27) is set to a logic 1, the device will access input channels sequentially with every rising edge of the Clock Input. If set to a logic 0, the device will access the channel selected via the Address Inputs (A1-A8, pins 37-40). In either mode of operation, the state of the Load Input is latched on the rising edge of the signal applied to Clock Input (pin 35).

Other control lines include Reset (pin 36) and MUX Enable (pin 25). As they imply, Reset can be used to initialize or reset the multiplexer to channel 0 and the MUX Enable input can be used in systems which require input channel expansion.

In addition to address inputs, address outputs are provided for use in identifying converted data. Applications requiring additional channel inputs can utilize the MUX Expand output for enabling additional multiplexers. These features can be better understood by referencing the Truth Tables for both the MN7208 and MN7216.

INSTRUMENTATION AMPLIFIER — The instrumentation amplifier can be configured for gains of 1, 10 and 500 utilizing internal gain setting resistors. Gains are selected via external pin connections (see section labeled Gain Selection). User definable gains can be set using external resistors.

GAIN SELECTION — Gain selection is accomplished via external pin connections. To operate the MN7208/7216 in a gain of 1, pin 17 should be left open. If a gain of 10 is desired, connect pin 17 to pin 23. If a gain of 500 is desired, connect pin 17 to pin 18. Care should be taken when laying out circuit runs to avoid introducing errors. Keep connections as short and direct as possible.

The gain may be set to values other than 1, 10 and 500 by using an external gain setting resistor. The equation for choosing the value of the external resistor is shown below.

$$RG=[40k/(G-1)]-50 \text{ Ohms}$$

INPUT - OUTPUT TRUTH TABLES

MN7216 — Truth Table

DIGITAL INPUTS							DIGITAL OUTPUTS					
Address Inputs						MUX	Address Outputs					
A_3	A_2	A_1	A_0	Load	Reset	Clock	Enable	B_3	B_2	B_1	B_0	Expand	Output
X	X	X	X	X	X	X	X	X	X	X	X	H	+Amp
X	X	X	X	X	L	↑	H	L	L	L	L	L	CH0
H	H	H	H	L	H	↑	H	H	H	H	H	L	CH15
L	H	H	H	L	H	↑	H	L	H	H	H	L	CH7
L	L	L	H	L	H	↑	H	L	L	L	H	L	CH1
L	L	L	L	L	H	↑	H	L	L	L	L	L	CH0
X	X	X	X	H	H	↑	H	L	L	L	H	L	CH1
X	X	X	X	H	H	↑	H	L	L	H	L	L	CH2
X	X	X	X	H	H	↑	H	L	L	H	H	L	CH3
X	X	X	X	H	H	↑	H	L	H	L	L	L	CH4
X	X	X	X	H	H	↑	H	L	H	L	H	L	CH5
X	X	X	X	H	H	↑	H	L	H	H	L	L	CH6
X	X	X	X	H	H	↑	H	L	H	H	H	L	CH7
X	X	X	X	H	H	↑	H	H	L	L	L	L	CH8
X	X	X	X	H	H	↑	H	H	L	L	H	L	CH9
X	X	X	X	H	H	↑	H	H	L	H	L	L	CH10
X	X	X	X	H	H	↑	H	H	L	H	H	L	CH11
X	X	X	X	H	H	↑	H	H	H	L	L	L	CH12
X	X	X	X	H	H	↑	H	H	H	L	H	L	CH13
X	X	X	X	H	H	↑	H	H	H	H	L	L	CH14
X	X	X	X	H	H	↑	H	H	H	H	H	L	CH15
X	X	X	X	H	H	↑	H	L	L	L	L	L	CH0

MN7208 — Truth Table

DIGITAL INPUTS						DIGITAL OUTPUTS			
Address Inputs					MUX	Address Outputs			
A_2	A_1	A_0	Load	Reset	Clock	Enable	B_2	B_1	B_0	Expand	Output
X	X	X	X	X	X	X	X	X	X	H	+Amp
X	X	X	X	L	↑	H	L	L	L	L	CH0
H	H	H	L	H	↑	H	H	H	H	L	CH7
L	H	H	L	H	↑	H	L	H	H	L	CH3
L	L	H	L	H	↑	H	L	L	H	L	CH1
L	L	L	L	H	↑	H	L	L	L	L	CH0
X	X	X	H	H	↑	H	L	L	H	L	CH1
X	X	X	H	H	↑	H	L	H	L	L	CH2
X	X	X	H	H	↑	H	L	H	H	L	CH3
X	X	X	H	H	↑	H	H	L	L	L	CH4
X	X	X	H	H	↑	H	H	L	H	L	CH5
X	X	X	H	H	↑	H	H	H	L	L	CH6
X	X	X	H	H	↑	H	H	H	H	L	CH7
X	X	X	H	H	↑	H	L	L	L	L	CH0
X	X	X	H	H	↑	H	L	L	H	L	CH1

NOTES:

1. "H" indicates TTL logic high (+2.0V minimum) for MUX Address, Load, Reset and Clock digital inputs. For MUX Enable, "H" indicates a logic high of +4.0V minimum.
2. "L" indicates TTL logic zero (+0.8V maximum) for all digital inputs.
3. "X" indicates "don't care."
4. "↑" indicates a "L" to "H" (low to high) transition.

TYPICAL PERFORMANCE SPECIFICATIONS

Typical MUX Performance Specifications	
Number of Channels: MN7208	8 Full Differential
MN7216	16 Single Ended
Input Voltage Range	±10V
Input Impendance	250mΩ/100pF
Logic Levels: Logic "1" (min)	+4.0V
Logic "0" (max)	+0.8V
Logic Currents: Logic "1"	±1μA
Logic "0"	±1μA
Access Time	500nsec
On Resistance	1.5kΩ
Cross Talk (1kΩ Source, 1KHz, 20Vp-p)	−68dB

Typical Instrumentation Amplifier Performance Specifications	
Voltage Range (min)	±10V
Input Impedance: Differential (MN7208)	$5\times10^{12}\Omega$//6pF
Single Ended (MN7216)	$2\times10^{12}\Omega$//1pF
Input Bias Current	20pA
Input Offset Current	2pA
Common Mode Rejection Ration (min): G=1	70dB
G=100	100dB
Gain Error (G=1): Initial (+25°C)	±0.04%
Over Temperature	±0.08%
Gain (G=1) Nonlinearity (max)	±0.01%
Large Signal Bandwidth	270kHz
Output Slew Rate	17V/μsec
Output Voltage Swing (min)	±10V
Output Current (min)	±5mA
Output Load Capacitance (Stability)	5000pF

CONFIGURING A DATA ACQUISITION SYSTEM

The MN7208/16 can be used with 12- and 16-bit sampling A/D converters to configure multi-channel data acquisition systems. The MN7208/16 provides a single-package solution for front-end signal conditioning/processing including multiplexing with control logic circuitry and an instrumentation amplifier (selectable fixed gains of 1, 10, 500 or user defined via external resistors). The Sampling A/D converter provides the T/H amplifier, necessary control logic circuitry, reference, clock, A/D and in some cases, a complete microprocessor interface. When these two products are used together, complete Data Acquisition Systems can be configured in a space efficient manner.

Single channel acquisition and conversion is accomplished by selecting the desired channel, stobing clock input and initiating the conversion cycle. The T/H amplifier internal to the Sampling A/D acquires and tracks the analog input during the MUX switching and settling time. Once settled and acquired, conversions can be initiated.

The circuit and timing diagram below illustrates a 16-channel, single-ended, 12-bit data acquisition system with a minimum of components. In this case, the MN7216 can be used with either the MN6227/28, MN6231/32 or the MN6774 Sampling A/D converters.

For the sake of simplicity, the sampling A/D is shown configured in a stand-alone mode of operation (these particular devices include a complete microprocessor interface and can be operated under full microprocessor control). The MN7216 is configured to operate in the sequential mode with an instrumentation amplifier gain of +10.

In the example, Reset is brought low prior to the rising edge of Master Clock, resetting the MUX address to channel 0. Additionally, the rising edge of Master Clock triggers the B1 input of the one-shot, creating a delayed start convert signal for the Sampling A/D. This delay allows for MUX switching, instrumentation amplifier settling and T/H acquisition times. The acquisition time delay is set by the values of R1 and C1. When the Q1 output of the one-shot times out, its falling edge triggers the A2 input, thereby creating the sampling A/D converters start convert signal. The values of R2 and C2 set the width of the start convert signal. When the conversion is complete (signaled by the falling edge of the sampling A/D converter's Status output), valid output data can be read. The next rising edge of Master Clock increments the channel address to Channel 1 and initiates the settling/acquisition conversion process again.

Other system options might include random MUX addressing, in which case, the address inputs A1 thru A8 would be set to the desired address prior to the rising edge of the Master Clock signal. In this case, Load (pin 27) would be tied to ground.