10-Bit 60 MSPS A/D Converter

AD9020

FEATURES
Monolithic 10-Bit/60 MSPS Converter
TTL Outputs
Bipolar (±1.75 V) Analog Input
56 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/Guidance Systems
Infrared Systems

GENERAL DESCRIPTION

The AD9020 A/D converter is a 10-bit monolithic converter capable of word rates of 60 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

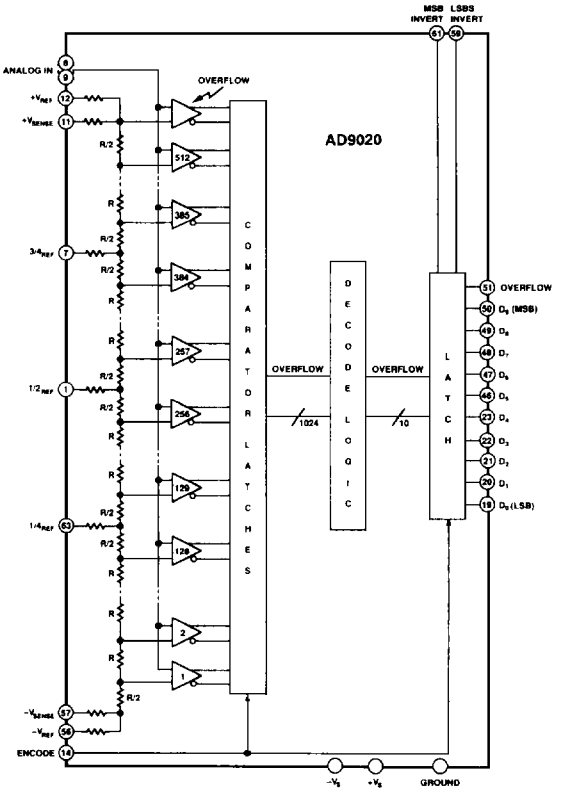
Encode and outputs are TTL-compatible, making the AD9020 an ideal candidate for use in low power systems. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0 to +70°C and −55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9020 A/D Converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9020/883B data sheet for detailed specifications.

FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6 V
$-V_S$	−6 V
ANALOG IN	−2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$	−2 V to +2 V
$+V_{REF}$ to $-V_{REF}$	4.0 V
DIGITAL INPUTS	−0.5 V to $+V_S$
$3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ Current	±10 mA
Digital Output Current	20 mA
Operating Temperature	
AD9020JE/KE/JZ/KZ	0 to +70°C
Storage Temperature	−65°C to +150°C
Maximum Junction Temperature[2]	+175°C
Lead Soldering Temp (10 sec)	+300°C

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ELECTRICAL CHARACTERISTICS ($\pm V_S$ = ±5 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 40 MSPS unless otherwise noted)[3]

Parameter (Conditions)	Temp	Test Level	AD9020JE/JZ Min	AD9020JE/JZ Typ	AD9020JE/JZ Max	AD9020KE/KZ Min	AD9020KE/KZ Typ	AD9020KE/KZ Max	Units
RESOLUTION			10			10			Bits
DC ACCURACY[3]									
Differential Nonlinearity	+25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	+25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current[4]	+25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	+25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance[4]	+25°C	V		45			45		pF
Analog Bandwidth	+25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	+25°C	I	22	37	56	22	37	56	Ω
	Full	VI	14		66	14		66	Ω
Ladder Tempco	Full	V		0.1			0.1		Ω/°C
Reference Ladder Offset									
Top of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Bottom of Ladder	+25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Offset Drift Coefficient	Full	V		50			50		μV/°C
SWITCHING PERFORMANCE									
Conversion Rate	+25°C	I	60			60			MSPS
Aperture Delay (t_A)	+25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Delay (t_{OD})[5]	+25°C	I	6	10	13	6	10	13	ns
Output Time Skew[5]	+25°C	I		3	5		3	5	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
Effective Number of Bits (ENOB)									
f_{IN} = 2.3 MHz	+25°C	I	8.6	9.0		8.6	9.0		Bits
f_{IN} = 10.3 MHz	+25°C	IV	8.0	8.4		8.0	8.4		Bits
f_{IN} = 15.3 MHz	+25°C	IV	7.5	8.0		7.5	8.0		Bits
Signal-to-Noise Ratio[6]									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	50	53		50	53		dB
f_{IN} = 15.3 MHz	+25°C	I	47	50		47	50		dB
Signal-to-Noise Ratio[6] (Without Harmonics)									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		51	54		dB
f_{IN} = 15.3 MHz	+25°C	I	48	52		48	52		dB

Parameter (Conditions)	Temp	Test Level	AD9020JE/JZ Min	AD9020JE/JZ Typ	AD9020JE/JZ Max	AD9020KE/KZ Min	AD9020KE/KZ Typ	AD9020KE/KZ Max	Units
DYNAMIC PERFORMANCE (CONTINUED)									
Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	I	61	67		61	67		dBc
f_{IN} = 10.3 MHz	+25°C	I	55	59		55	59		dBc
f_{IN} = 15.3 MHz	+25°C	I	49	53		49	53		dBc
Two-Tone Intermodulation Distortion Rejection[7]	+25°C	V		70			70		dBc
Differential Phase	+25°C	V		0.5			0.5		Degree
Differential Gain	+25°C	V		1			1		%
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			20			20	μA
Logic "0" Current	Full	VI			800			800	μA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I	6			6			ns
Pulse Width (Low)	+25°C	I	6			6			ns
DIGITAL OUTPUTS									
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (I_{OL} = 10 mA)	Full	VI			0.4				V
POWER SUPPLY									
$+V_S$ Supply Current	+25°C	I		440	530		440	530	mA
	Full	VI			542			542	mA
$-V_S$ Supply Current	+25°C	I		140	170		140	170	mA
	Full	VI			177			177	mA
Power Dissipation	+25°C	I		2.8	3.3		2.8	3.3	W
	Full	VI			3.4			3.4	W
Power Supply Rejection Ratio (PSRR)[8]	Full	VI		6	10		6	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (part soldered onto board): 68-pin leaded ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow); θ_{JA} = 15°C/W (air flow = 500 LFM). 68-pin ceramic LCC: θ_{JC} = 2.6°C/W; θ_{JA} = 15°C/W (no air flow); θ_{JA} = 13°C/W (air flow = 500 LFM).

[3]$3/4_{REF}$, $1/2_{REF}$, and $1/4_{REF}$ reference ladder taps are driven from dc sources at +0.875 V, 0 V, and −0.875 V, respectively. Accuracy of the overflow comparator is not tested and not included in linearity specifications.

[4]Measured with ANALOG IN = $+V_{SENSE}$.

[5]Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D_0–D_9. Output skew measured as worst-case difference in output delay among D_0–D_9.

[6]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[7]Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

[8]Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in $+V_S$ or $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

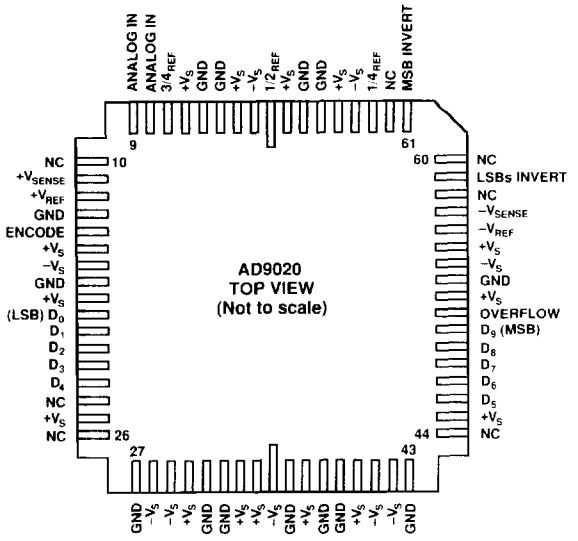
V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Device	Temperature Range	Description	Package Option*
AD9020JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9020KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9020SZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020SE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020TZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020TE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020/PCB	0 to +70°C	Evaluation Board	

*E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.



AD9020 Pin Designations

AD9020 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$1/2_{REF}$	Midpoint of internal reference ladder.
2, 16, 28, 29, 35, 41, 42, 54, 64	$-V_S$	Negative supply voltage; nominally −5.0 V ±5%.
3, 6, 15, 18, 25, 30, 33, 34, 37, 40, 45, 52, 55, 65, 68	$+V_S$	Positive supply voltage; nominally +5 V ±5%.
4, 5, 13, 17, 27, 31, 32 36, 38, 39, 43, 53, 66, 67	GROUND	All ground pins should be connected together and to low-impedance ground plane.
7	$3/4_{REF}$	Three-quarter point of internal reference ladder.
8, 9	ANALOG IN	Analog input; nominally between ±1.75 V.
11	$+V_{SENSE}$	Voltage sense line to most positive point on internal resistor ladder. Normally +1.75 V.
12	$+V_{REF}$	Voltage force connection for top of internal reference ladder. Normally driven to provide +1.75 V at $+V_{SENSE}$.
14	ENCODE	TTL-compatible convert command used to begin digitizing process.
19–23, 46–50	D_0–D_9	TTL-compatible digital output data.
51	OVERFLOW	TTL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
56	$-V_{REF}$	Voltage force connection for bottom of internal reference ladder. Normally driven to provide −1.75 V at $-V_{SENSE}$.
57	$-V_{SENSE}$	Voltage sense line to most negative point on internal resistor ladder. Normally −1.75 V.
59	LSBs INVERT	Normally grounded. When connected to $+V_S$, lower order bits (D_0–D_8) are inverted.
61	MSB INVERT	Normally grounded. When connected to $+V_S$, most significant bit (MSB; D_9) is inverted.
63	$1/4_{REF}$	One-quarter point of internal reference ladder.