BURR-BROWN®

ADC87/883B SERIES

ADC87/883B ADC87V/883B ADC87U/883B
ADC87 ADC87V ADC87U

REVISION D
JANUARY, 1989

12-Bit, –55°C to +125°C MILITARY ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HI-REL MANUFACTURE
- ACCURATE:
  ±1/2 LSB max Linearity Error
  ±0.1% FSR max Full-Scale Absolute Accuracy
  ±15ppm max Gain Drift
- 10μs MAX CONVERSION TIME
- –55°C TO +125°C OPERATION
- COMPLETE:
  Internal Reference
  Internal Buffer
  Internal Clock
- MIL-STD-883B SCREENING

DESCRIPTION

The ADC87/883B Series is a high performance, analog-to-digital converter. It features ±1/2LSB linearity, ±0.1% full-scale accuracy, ±15ppm drift, 10μs conversion time, –55°C to +125°C operation and optional MIL-STD-883 screening.

The ADC87 uses successive approximation. It resolves the most significant bit first, then the second bit, then the third, etc. Successive approximation is the most popular high performance design because it is fast and accurate.

The ADC87 is a hybrid microcircuit. It is complete with an internal reference, an input buffer amplifier and an internal clock. The converter may be short cycled to provide faster conversion to less resolution. Five analog input ranges—±2.5V, ±5V, ±10V, 0V to +10V, and 0V to +20V—are available, and the digital output data is available in parallel and serial format. All digital outputs and inputs are TTL-compatible. Standard power supply voltages (±15VDC and +5VDC) are required.

Three electrical performance grades are available. The premium grade and the "V" grade operate from –55°C to +125°C and are designed for military, aerospace, and demanding industrial applications. The "U" grade is specified from –25°C to +85°C and from –55°C to +125°C. Applications include test equipment, shipboard, and ground support equipment where operation is normally between –25°C and +85°C and full temperature range operation must be assured.

The ADC87/883B Series is manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions, which assures inherent quality and provides for long product life. The ADC87 is hermetically sealed in a ceramic, side-brazed, dual-in-line package.

Two product assurance levels are available: Standard, and /883B. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The /883B product assurance level, /883B suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883B, Method 5008 and 10% PDA. Quality assurance further processes /883B devices by performing Group A and B inspections on each inspection lot and Group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

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DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
ANALOG-TO-DIGITAL CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a precision, 12-bit, integrated circuit analog-to-digital converter.

1.2 Part Number. The complete part number is shown below.

ADC87	—	/883B
Basic Model Number	Grade (see 1.2.1)	Hi-Rel Product Designator (see 1.2.2)

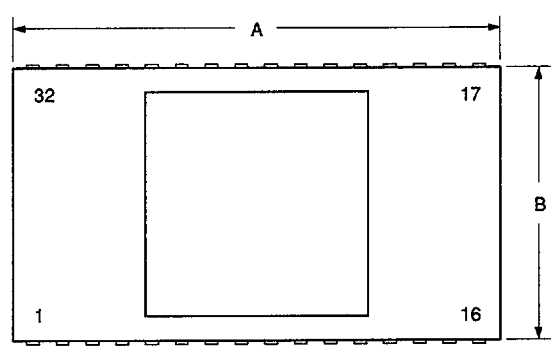
1.2.1 Device Type. The device is a single, 12-bit, analog-to-digital converter. There are two electrical performance grades. The premium grade has no grade designation in the part number, and features specifications and tests from –55°C to +125°C. The "V" grade has a "V" grade designation in the part number and features specifications and tests from –55°C to +125°C. The "U" grade has a "U" grade designation in the part number and features specifications and tests from –25°C to +85°C, and specifications from –55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device Class. The device class is similar to the hybrid class (Class B) product assurance level as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level available as follows:

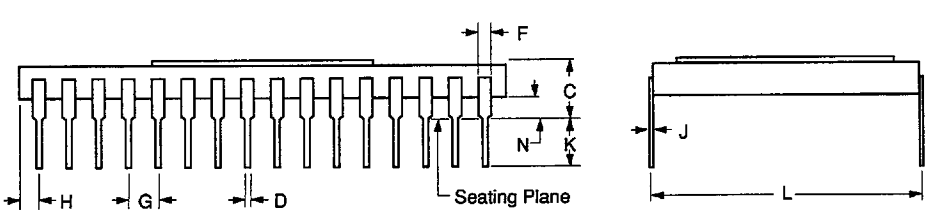
Hi-Rel Product Designator	Requirements
/883B	Standard model plus 100% MIL-STD-883 Class B screening, with 10% PDA, plus Quality Conformance Inspection (QCI) consisting of Groups A and B performed in each inspection lot, plus Groups C and D performed as required by MIL-STD-883.
none	Standard model including 100% electrical testing.

1.2.3 Case Outline. The case outline is as defined in MIL-M-38510, Appendix C and is shown in Figure 1. The case is ceramic and nonconductive.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.580	1.620	40.13	41.15
B	.880	.900	22.35	22.86
C	.138	.198	3.51	5.03
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.125	.185	3.18	4.70
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



1.2.4 Absolute Maximum Ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	+7VDC
Analog Inputs (pins 24 and 25)	±25VDC
Buffer Input	±18VDC
Digital Inputs	+5.5VDC
Storage temperature range	– 65°C to +150°C
Lead temperature (soldering, 60s)	+300°C
Junction temperature	T_J = +175°C
Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC
	V_{DD}: +4.75VDC to +5.25VDC
Case temperature range	–55°C to +125°C

1.2.6 Power and Thermal Characteristics.

Package	Case Outline	Maximum Allowable Power Dissipation	Maximum θ_{J-C}	Maximum θ_{C-A}	Maximum θ_{J-A}
32-lead ceramic side-braze	Figure 1	1500mW at T_A = 125°	7°C/W	25°C/W	32°C/W

2. APPLICABLE DOCUMENTS

2.1 Government Specification and Standard. The following documents form a part of this specification to the extent specified herein.

SPECIFICATION
MILITARY
MIL-M-38510 — Microcircuits, general specification for.

STANDARD
MILITARY
MIL-STD-883 — Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail Specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.2 Design, Construction, and Physical Dimensions.

3.2.1 Package, Metals, and Other Materials. The packages, metal surfaces, and other materials are in accordance with MIL-M-38510, except that organic and polymeric materials may be used for substrates and die attach. The exterior metal surfaces are corrosion resistant. The other materials are non-nutrient to fungus as specified in MIL-M-38510.

3.2.2 Design Documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal Conductors and Internal Wires. The internal conductors and internal lead wires are in accordance with MIL-STD-38510.

3.2.4 Lead Material and Finish. The lead material is kovar (type A). The lead finish is gold plate with nickel underplating. The lead material and finish are in accordance with MIL-M-38510 and are solderable in accordance with MIL-STD-883, Method 2003.

3.2.5 Glassivation. All dice utilized are glassivated.

3.2.6 Die Thickness. The die thickness is in accordance with MIL-M-38510.

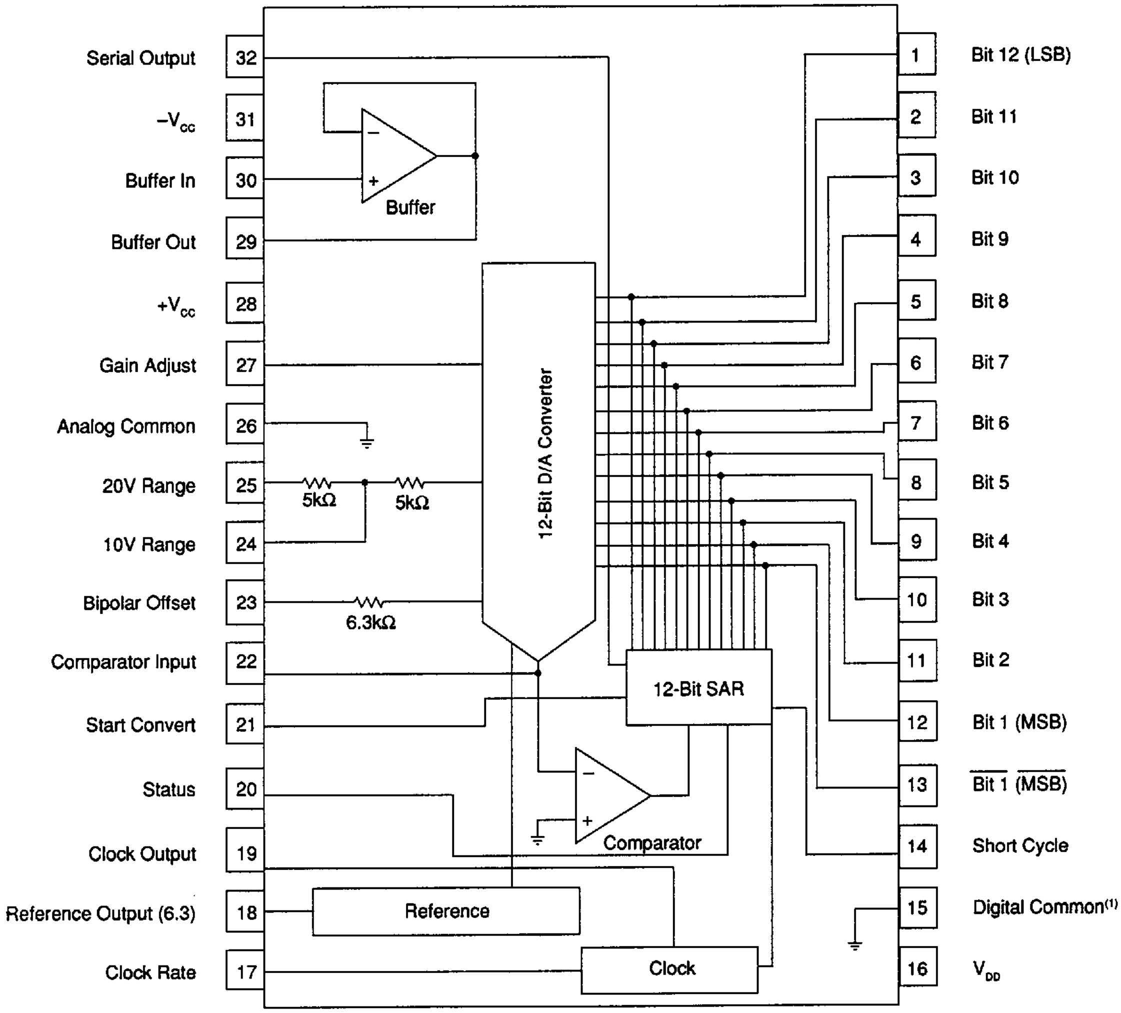
3.2.7 Physical Dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein and are shown in Figure 1.

3.2.8 Circuit Diagram and Terminal Connections. The simplified circuit diagram and terminal connections are shown in Figure 2.

3.3 Electrical Performance Characteristics. The electrical performance characteristics are specified in Table I and apply over the full operating ambient temperature range of –55°C to +125°C unless otherwise specified.

3.3.1 Input Range. The analog input range is as specified in Table V when externally connected as shown therein.

3.3.2 Output Code. Coding is complementary binary. The digital output codes corresponding to analog input voltages are shown in Table VI.



NOTE: (1) Pin 15 is connected to the case.

FIGURE 2. Circuit Diagram and Terminal Connections (Bottom View).

3.3.3 Transfer Function. An A/D converter represents an analog input voltage in a digital output format. The converter resolves the analog input into 12 bits of resolution, or 2^{12}, or 4096 voltage segments. For each voltage segment there is a unique digital output code.

The ideal transfer curve, as shown in Figure 3, is a "stair-case" connecting the extremes of the analog input range. Minus full scale (–FS) corresponds to digital 1111 1111 1111, the first transition occurs at –FS + 1/2LSB, each bit is 1LSB wide, and +FS – 1LSB corresponds to 0000 0000 0000. An ideal straight line connects each end point and the center of each bit. A best fit is parallel to the ideal straight line and biased to minimize linearity errors. Note that the coding is complementary.

The "basic" converter is unipolar in design; that is, 0VDC analog input produces one digital extreme and plus full-scale VDC produces the other digital extreme. There are two unipolar input ranges. For bipolar operation, a bias (bipolar offset) is introduced into the input such that 0VDC analog input produces midscale digital output. This allows plus and minus analog inputs (see Figure 3). There are three bipolar input ranges.

The errors from the best fit transfer function are specified in Table I. Linearity and Differential Linearity are the most meaningful ADC87 accuracy indicators, as they are not externally adjustable. They are factory laser-trimmed. Zero error and gain error are laser-trimmed and may be externally nulled if necessary for the application. The inherent quantization uncertainty due to resolving or quantizing the analog input into bits is ±1/2LSB.

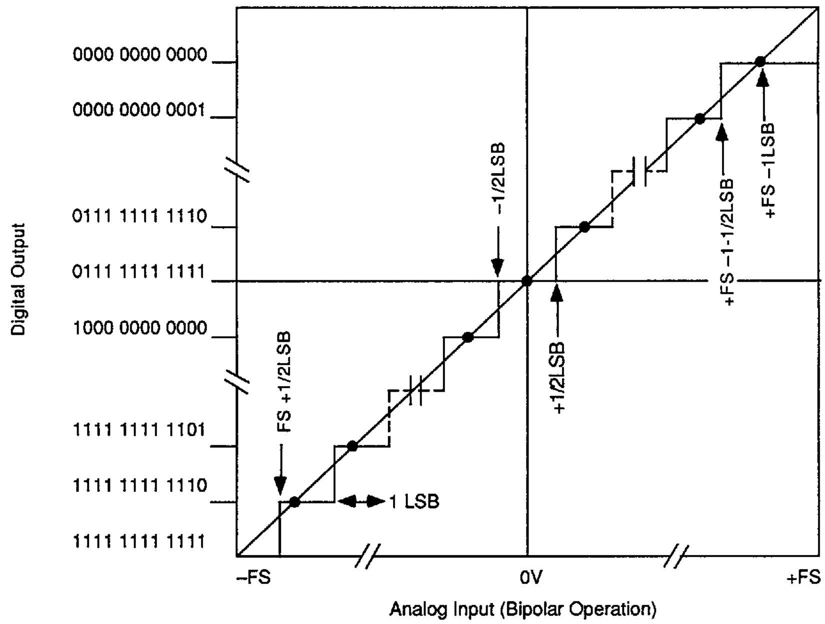


FIGURE 3. Ideal A/D Converter Transfer Function.

3.3.4 Timing Considerations. The timing diagram is shown in Figure 4. A start convert, positive going pulse, initiates a conversion. The most significant bit (MSB) is determined during the second clock pulse, and each successive bit is determined during the next 11 clock pulses. When conversion is complete, Status output drops to Logic 0. Digital output data is available in parallel or serial format. Serial output data may be strobed out bit-by-bit, during the clock period after the bit is determined.

3.3.5 Zero error and gain error adjustment. Zero error and gain error may be externally nulled using the circuits shown in Figure 6. See Applications Information, paragraph 7.4.

3.3.6 Required external connections. For specified accuracy and speed, connect Clock Rate, pin 17, to 0VDC, pin 15. For a 12-bit conversion cycle, connect Short Cycle, pin 14 to Logic 1, pin 16. See Applications Information, paragraph 7, for additional information.

3.4 Electrical Test Requirements. Electrical test requirements are as specified in Table II. The subgroups of Table III, which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum:

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code(1)
d. Manufacturer's identification (BURR-BROWN BB).
e. Manufacturer's designating symbol (CEBS).
f. Country of origin.
g. Electrostatic sensitivity identifier (Δ).
h. Compliance identifier "C."

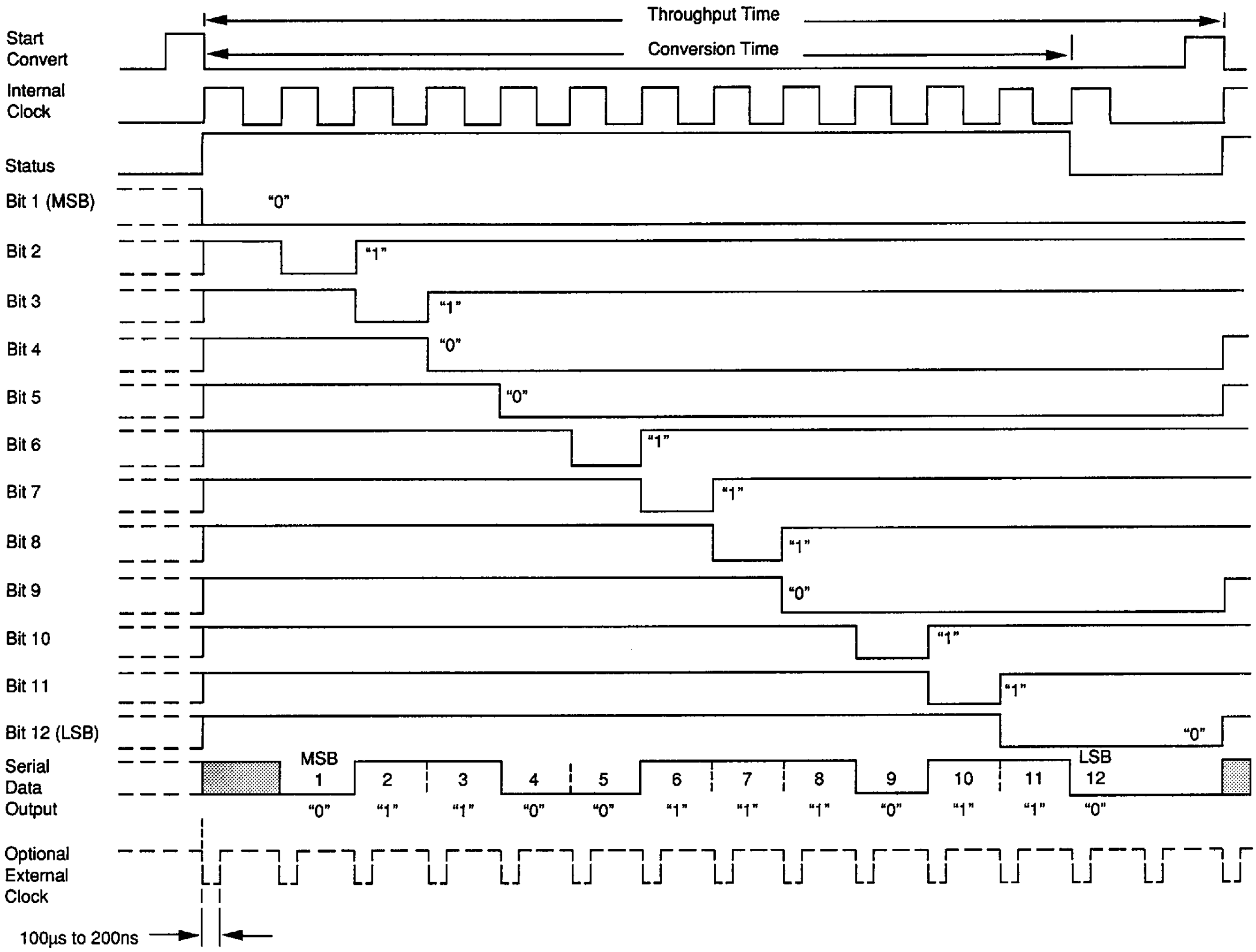
3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework Provisions. Rework provisions, including rebonding for the "/883B" product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for the "/883B" product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot.

3.8 Product and Process Change. Burr-Brown will not implement any major change to the design, materials, construction, or manufacturing process that may affect the performance, quality, or interchangeability of the microcircuit without full or partial requalification.

(1) A 4-digit code, indicating year and week of seal, and a 4- or 5-digit lot identifier are marked on each microcircuit.



NOTES: (1) Start Convert must be at least 50ns wide and must remain low during conversion. Conversion is initiated by the Start Convert trailing edge. Once a conversion has begun, a second start pulse will not reset the converter. (2) Parallel data will be valid 140ns after status goes low and remains valid until after another conversion is initiated. (3) Serial data will be valid 140ns after an internal clock rising edge and 200ns after an external clock falling edge. (4) When using an external clock, conversion is initiated by the falling edge of the first clock pulse following status going low. Ther converter will continuously convert.

FIGURE 4. Timing Diagram.

3.9 Screening. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, Method 5008, Class B, and as specified herein. All microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality Conformance Inspection. Quality Conformance Inspection (QCI) for the "/883B" product designation is in accordance with MIL-STD-883, and as specified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE I. Electrical Performance Characteristics.

(T_A = –55°C to +125°C, Supply Voltages ±15VDC and +5VDC, unless otherwise specified.)

		ADC87/883B ADC87			ADC87V/883B ADC87V			ADC87U/883B ADC87U			
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION		12			*			*			Bits
ANALOG INPUTS											
Input Voltage Ranges											
Unipolar			0 to +5, 0 to +10			*			*		V
Bipolar			±2.5, ±5, ±10			*			*		V
Direct Input Impedance											
0V to +5V, ±2.5V			2.5			*			*		kΩ
0V to +10V, ±5V			5			*			*		kΩ
±10V			10			*			*		kΩ
Buffer Amplifier											
Gain Accuracy			±0.01			*			*		%
Input Impedance	T_A = +25°C		10^{12}			*			*		Ω
Input Bias Current	T_A = +25°C		80			*			*		nA
Offset Voltage	T_A = +25°C		1	5		*			*		mV
Settling Time	10V step to ±0.01% FSR		3			*			*		µs
DIGITAL INPUTS											
Start Convert Command[1]											
Positive Pulse Width		50			*			*			ns
Logic Loading				1			*			*	TTL Load[2]
Short Cycle Logic Loading				1			*			*	TTL Load
Logic Levels (all digital inputs)											
Logic "1"		2			*			*			V
Logic "0"				0.8			*			*	V
DIGITAL OUTPUTS											
Parallel Data Coding(3)											
Unipolar Ranges			CSB			*			*		
Bipolar Ranges			COB, CTC			*			*		
Output Drive		2			*			*			TTL Loads
Serial Data Coding (NRZ)[3]			CSB, COB				*				
Output Drive		2			*			*			TTL Loads
Status Bit Coding					Logic 1 During Conversion						
Output Drive		2			*			*			TTL Loads
Internal Clock Output Drive		2			*			*			TTL Loads
Logic Levels (all outputs)											
Logic "1"		2.4			*			*			V
Logic "0"				0.4			*			*	V
TRANSFER CHARACTERISTICS**											
Zero Error, Bipolar[4] (Bipolar Major Transition Error)	+25°C		±0.02	±0.05		*	±0.1		*	±0.1	%FSR[5]
	–25°C to +85°C								±0.05	±0.15	%FSR
	–55°C to +125°C		±0.05	±0.01			±0.2			±0.3	%FSR
Full Scale Absolute Accuracy Error[4]	+25°C		±0.05	±0.1		*	*		*	±0.15	%FSR
Bipolar[6]	–25°C to +85°C								±0.1	±0.25	%FSR
Gain Error[4]	+25°C		±0.05	±0.1		*	*		*	*	%
	Drift[7]		±10	±15		*	*		*	*	ppm/°C
Zero Error, Unipolar[4]	+25°C		±0.10	±0.15		*	*		*	+0.2	%FSR
	–25° to +85°C					*	*		±0.15	±0.3	%FSR
	–55°C to +125°C		±0.15	±0.2		*	*			±0.6	%FSR
Full Scale Absolute Accuracy Error	+25°C		±0.1	±0.2		*	*		*	*±0.25	%FSR
Unipolar[4]	–25°C to +85°C								±0.2	±0.4	%FSR
	–55°C to +125°C		±0.2	±0.3		*	*			±0.9	%FSR
Linearity Error	+25°C		±1/4	±1/2		*	*		*	*	LSB(8)
	–25°C to +85°C								±1/2	±1	LSB
	–55°C to +125°C		±1/2	±1		*	*			±4	LSB
	Drift		±2			*			*		ppm of FSR/°C
Inherent Quantization Uncertainty			±1/2			*			*		LSB
Differential Linearity Error	+25°C		±1/4	±1/2		*	*		*	*	LSB
	–25°C to +85°C									±1	LSB
	–55°C to +125°C		±1							±3	LSB
	Drift		±2			*			*		ppm of FSR/°C
No Missing Codes		–55		+125							°C
Monotonicity		–55		+125	*		*	–25		+85	°C
Zero Adjustment Range		0.3	0.4		*	*		*	*		%FSR
Gain Adjustment Range		0.5	0.55		*	*		*	*		%FSR

TABLE I. Electrical Performance Characteristics. (Cont)

(T_A = –55°C to +125°C, Supply Voltages ±15VDC and +5VDC, unless otherwise specified.)

		ADC87/883B ADC87			ADC87V/883B ADC87V			ADC87U/883B ADC87U			
CHARACTERISTICS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DYNAMIC CHARACTERISTICS**											
Conversion Time(9)				10			*			*	µs
Internal Clock Frequency(9)			1.3		*	*		*	*		MHz
REFERENCE											
Internal Reference											
Voltage		6.0	+6.3	6.6	*	*	*	*	*	*	V
Drift	–55°C to +125°C		±5			*					ppm/°C
	–25°C to +85°C									±5	ppm/°C
External Current				200			*			*	µA
POWER SUPPLY											
Power Supply Range											
±15V Supply		±14.5	±15	±15.5	*	*	*	*	*	*	V
+5V Supply		+4.75	+5	+5.25	*	*	*	*	*	*	V
Quiescent Current											
+15V			35	45		*	*		*	*	mA
–15V			35	45		*	*		*	*	mA
+5V			40	50		*	*		*	*	mA
Power Consumption	Quiescent		1300	1500		*	*		*	*	mW
Power Supply Rejection											
+15VDC			±0.002			*			*		$\%FSR/\%V_{CC}$
–15VDC			±0.002			*			*		$\%FSR/\%V_{CC}$
+5VDC			±0.001			*			*		$\%FSR/\%V_{CC}$
THERMAL CHARACTERISTICS											
Operating Temperature Range	Ambient	–55		+125	*		*	*		*	°C
Storage Temperature Range	Ambient	–65		+150	*		*	*		*	°C
Thermal Impedance											
Case to Ambient, θ_{CA}			20			*			*		°C/W
Junction to Case, θ_{JC}			5			*			*		°C

*Specifications the same as for ADC87/883B.
**Transfer and dynamic characteristics are specified without the optional buffer amplifiers.
NOTES: (1) Trailing edge (Logic "1" to Logic "0") initiates conversion. (2) A TTL Load is defined as 40µA max at VIN = 2.4VDC (Logic "1") and –1.6mA max at VIN = 0.4VDC (Logic "0"). (3) CSB = Complementary Straight Binary; COB = Complementary Offset Binary; CTC = Complementary Two's Complement. Serial and parallel output data is in Nonreturn to Zero (NRZ) format. See Output Coding and Timing Diagram. (4) Externally adjustable to zero. This specification is without external adjustment. (5) FSR = Full Scale Range. The ±10V analog input range is a 20V FSR. The ±5V or 0 to 10V input range is a 10V FSR. (6) Applies to +Full Scale and to –Full Scale. (7) Gain drift is defined as the absolute value of the change from +25°C to the hot temperature, plus the absolute value of the change from +25°C to the cold temperature, and that quantity is divided by the temperature span. This is a 3-point drift. The hot temperature change is usually greater than the cold temperature change. (8) ±1LSB = ±0.024% FSR. (9) Conversion time is defined as the width of the status pulse. It is specified using the internal clock, with Clock Rate, pin 17, connected to 0VDC and Short Cycle, pin 14, connected to Logic "1."

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III.)

Models	**ADC87/883B**	**ADC87**		
MIL-STD-883 Test Requirements (Hybrid Class)	**ADC87V/883B**	**ADC87V**	**ADC87U/883B**	**ADC87U**
		Subgroups	**(see Table III.)**	
Interim electrical parameters (preburn-in) (Method 5008)	1, 4, 7	1, 4, 7	1, 4, 7	1, 4, 7
Final electrical test parameters (Method 5008)	1*, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7	1*, 2U, 3U, 4,7	1, 2U, 3U, 4,7
Group A test requirements (Method 5008)	1, 2, 3, 4, 5, 6, 7	—	1, 2U, 3U, 4, 7	—
Group C end point electrical parameters (Method 5008)	1	—	1	—

*PDA applies to subgroup 1 (see 4.3d).

TABLE III. Group A Inspection.

			ADC87/883B ADC87		ADC87V/883B ADC87V		ADC87U/883B ADC87U		
SUBGROUP	PARAMETERS	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
1	Zero error, –FS bipolar[2]	±10V range[3]		±10		±20		±14	mV
T_A = +25°C	Full scale error, –FS bipolar[2]	±10V range[3]		±20	*			±30	mV
	Full scale error, +FS bipolar[2]	±10V range[3]		±20		*		±30	mV
	Gain Error[2]	±10V range		±1/2		*		*	mV
	No missing codes		Pass		*		*		Pass/fail
	Internal reference voltage		±6.0	+6.6	*	*	*	*	V
	Zero error, unipolar[2]	0V to +10V range[3]		±20		*		*	mV
	Full scale error, unipolar[2]	0V to +10V range[3]		±20		*		*	mV
	Gain error, unipolar[2]	0V to +10V range		±10		*		*	mV
	Quiescent Current	No load, all bits Logic "1"							
	$+V_{CC}$			45		*		*	mA
	$-V_{CC}$			45		*		*	mA
	V_{DD}			50		*		*	mA
2	Zero error, bipolar	±10V range[3]		±20		±40			mV
T_A = +125°C	Full scale error, –FS bipolar[2]	±10V range[3]		±40		*			mV
	Full scale error, +FS bipolar[2]	±10V range[3]		±40		*			mV
	Gain drift	See subgroup 3							
	Linearity Error			±1		*			LSB
	Differential Linearity Error			±1					LSB
	No missing codes		Pass		*		Pass		Pass/fail
2U	Zero error, bipolar	±10V range[3]						±30	mV
T_A = +85°C	Full scale error, –FS bipolar[2]	±10V range[3]						±50	mV
	Full scale error, +FS bipolar[2]	±10V range[3]						±50	mV
	Gain drift	See subgroup 3U							
	Linearity Error							±1	LSB
	Differential Linearity Error							±1	LSB
	No missing codes						Pass		Pass/fail
3	Zero error, bipolar	±10V range[3]		±20		±40			mV
T_A = –55°C	Full scale error, –FS bipolar[2]	±10V range[3]		±40		*			mV
	Full scale error, +FS bipolar[2]	±10V range[3]		±40		*			mV
	Gain drift	[5]		±54					mV
	Linearity Error			±1		*			LSB
	Differential Linearity Error			±1		*			LSB
	No missing codes		Pass		*		Pass		Pass/fail
3U	Zero error, bipolar	±10V range[3]						±30	mV
T_A = –25°C	Full scale error, –FS bipolar[2]	±10V range[3]						±50	mV
	Full scale error, +FS bipolar[2]	±10V range[3]						±50	mV
	Gain drift	[6]						±33	mV
	Linearity Error							±1	LSB
	Differential Linearity Error							±1	LSB
	No missing codes						Pass		Pass/fail
4 T_A = +125°C	Conversion time			10		*		11	µs
5 T_A = +25°C	Conversion time			10		*		11	µs
6 T_A = –55°C	Conversion time			10		*		11	µs
7	Linearity Error			±1/2		*		*	LSB
	Differential Linearity Error[4]			±1/2		*		*	LSB
T_A = +25°C	Power consumption	Quiescent		1500		*		*	mW
	Zero adjustment range	±10V range	±60		*		*		mV
	Gain adjustment range	±10V	±100		*		*		mV
	MSB inverted output		Pass		*		*		Pass/fail
	Serial Output		Pass		*		*		Pass/fail

*Specifications the same as ADC87/883B.

NOTES: (1) $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, no load, without the optional buffer amplifier, unless otherwise specified. The internal clock is used. Clock Rate, pin 17, is connected to 0VDC. Short Cycle, pin 14, is connected to Logic "1." (2) Without external adjustment. (3) For the ±10V range: bipolar +FS is ideally at +9.995117VDC; bipolar zero is ideally at 0.000VDC; bipolar –FS is ideally at –10.000VDC. For the 0 to 10V range: unipolar +FS is ideally at +9.997559VDC; unipolar zero is ideally at 0.000VDC. Refer to Figure 3 and Table V. (4) Monotonicity is assured by differential linearity ≤±1LSB. (5) The absolute value of the gain change from +25°C to +125°C is added to the absolute value of the gain change from +25°C to –55°C. This provides a 3-point drift. (6) The absolute value of the gain change from +25°C to +85°C is added to the absolute value of the gain change from +25°C to –25°C. This provides a 3-point drift.

TABLE IV. Analog Input Range Selection Connections.

Input Range	DIRECT INPUT Input Signal to Pin	DIRECT INPUT Input Impedance	DIRECT INPUT Pin Connections	BUFFERED INPUT Input Signal to Pin	BUFFERED INPUT Input Impedance	BUFFERED INPUT Required External Pin Connections
±2.5V	24	2.5kΩ	30 to 26 29 open 23 to 22 22 to 25	30	50MΩ	29 to 24 23 to 22 22 to 25
±5V	24	5kΩ	30 to 26 29 open 23 to 22	30	50MΩ	29 to 24 23 to 22
±10V	25	10kΩ	30 to 26 29 open 23 to 22	30	50MΩ	29 to 25 23 to 22
0V to +5V	24	2.5kΩ	30 to 26 29 open 23 to 26 22 to 25	30	50MΩ	29 to 24 23 to 26 22 to 25
0V to +10V	24	5kΩ	30 to 26 29 open 23 to 26	30	50MΩ	29 to 24 23 to 26

TABLE V. Ideal Analog Input Voltage vs Digital Output Code.

	DIGITAL OUTPUT CODE			
	MSB LSB	MSB LSB	MSB LSB	
Input Range	1111 1111 1111	0111 1111 1111	0000 0000 0000	1LSB
±2.5V	–2.500V	0V	+2.498779V	1.2207mV
±5V	–5.000V	0V	+4.997559V	2.4414mV
±10V	–10.000V	0V	+9.995117V	4.8828mV
0 to +5V	0V	+2.500V	+4.998779V	1.2207mV
0 to +10V	0V	+5.000V	+9.997559V	2.4414mV

NOTE: Analog voltages are the center of the bit range. Transitions occur 1/2LSB before and 1/2LSB after the bit center.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and Inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, Method 5008, Class B, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for Groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4 herein).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening for the "/883B" Hi-Rel product designation is in accordance with MIL-STD-883, Method 5008, Class B, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, Method 2001) is test condition A, Y_1 axis only.

b. Interim and final electrical test parameters are specified in Table II. The interim electrical parameters test before burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, Method 1015) conditions:

(1) Test condition B
(2) Test circuit is Figure 5 herein
(3) T_A = +125°C minimum
(4) Test duration is 160 hours minimum.

d. Percent Defective Allowable (PDA). The PDA, for "/883B" product designation only, is ten percent and includes both parametric and catastrophic failures. It is based on failures from Group A, Subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, Method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed before burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests are omitted, all screening failures shall be included in the PDA. The verified failures of Group A, Subgroup 1 after burn-in are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

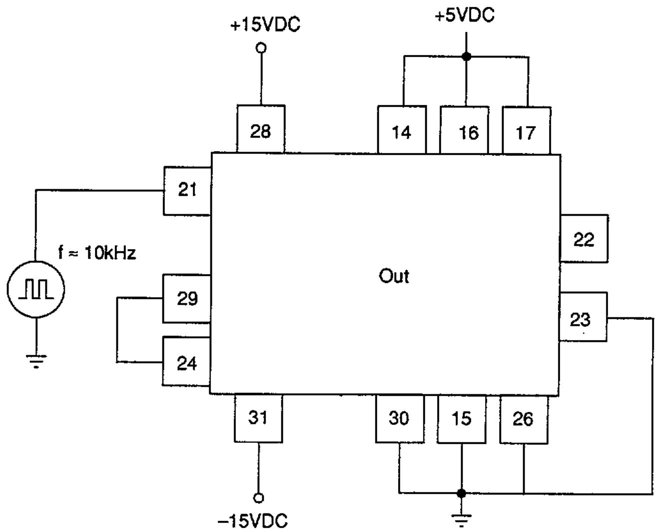


FIGURE 5. Test Circuit—Burn-in and Operating Life Test.

4.4 Quality Conformance Inspection. Groups A and B inspections of MIL-STD-883, Method 5008, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, Method 5008, Class B are performed as required by MIL-STD-883. A report of the most recent Group C and D inspections is available from Burr-Brown.

4.4.1 Group A Inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, Method 5008, and as specified in Table II herein.

4.4.2 Group B Inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, Method 5008, Class B.

4.4.3 Group C Inspection. Group C inspection consists of the subgroups and LTPD values shown in MIL-STD-883, Method 5008, and as follows:

a. Operating life test (MIL-STD-883, Method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

4.4.4 Group D Inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, Method 5008.

4.4.5 Inspection of Packaging. Inspection of packaging shall be in accordance with MIL-M-38510.

4.5 Methods of Examination and Test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced Test Methods of MIL-STD-883.

4.5.1 Voltage and Current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PACKAGING

5.1 Packaging Requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended Use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is required or desirable.

6.3. Ordering Data. The contract or purchase order should specify the following:
a. Complete part number (see paragraph 1.2).
b. Requirements for Certificate of Compliance, if desired.

6.4 Definitions.

Full Scale Absolute Accuracy Error. Full scale accuracy is the difference between the ideal and the actual, unadjusted, analog input voltage at the full scale points. It applies to unipolar plus full scale, bipolar minus full scale, and bipolar plus full scale. Absolute accuracy includes zero, gain, linearity, and noise errors and , when specified over temperature, includes the drifts of these errors. It is measured at the first or last transition, as appropriate. The error is expressed in LSBs or percent of FSR.

Bipolar Zero Error. Bipolar zero error is the difference between the ideal and the actual analog input voltage for the digital output code 0111 1111 1111. It is measured at the 1000 0000 0000 to 0111 1111 1111 transition which ideally occurs at 0VDC +1/2LSB.

Gain Error. Gain error is the difference between the ideal and the actual analog input voltage span. It applies to both unipolar and bipolar input ranges. It is measured between the first transition which is ideally FSR-2LSB.

Gain error in some literature describes what is defined herein to be unipolar full scale error and bipolar plus full scale error.

Offset Error. This term is not used with the ADC87. Offset error in some literature describes what is defined herein to be unipolar zero error and/or bipolar minus full scale error.

Linearity Error. Linearity error is the difference between the ideal and the actual bit transition when zero error and gain error equal zero.

Differential Linearity Error. Differential linearity error is the difference between the ideal and the actual bit step width. Zero differential linearity error means each bit step width is 1LSB. A maximum differential linearity error of ±1/2LSB means a bit step width may be between 1/2LSB and 3/2LSB.

Monotonicity. Monotonicity is the condition where the digital output code remains the same or increases for an increasing analog input signal.

Quantization Uncertainty. Quantization uncertainty is the inherent uncertainty of being able to determine the analog voltage which produces a digital code. Because the analog input voltage is divided or quantized into a finite number of bits, each digital code represents an analog voltage span equal to 1LSB. Quantization uncertainty is ±1/2. Its magnitude may be reduced only by using a higher resolution converter.

6.5 Microcircuit group assignment. These microcircuits are Technology Group I as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic Sensitivity. Caution—these microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Layout. To produce clean, noise-free, accurate conversions, high frequency layout techniques should be used. Wide, low inductance conductor patterns, short and direct external component leads, power supply decoupling, and a ground plane are recommended. Long runs should be avoided. Coupling and runs, which might cause input-to-output coupling, should be avoided. High impedance points should be given special consideration. The input to the buffer, the comparator input (particularly sensitive) and the external adjustment pins are sensitive. Shielding by Analog Common or ±15VDC supply patterns may be helpful.

7.2 Grounding. A ground plane under the ADC87 is recommended.

Analog Common (pin 26) and Digital Common (pin 15) must be connected together and to the analog system ground. Preferably, connect both commons directly to the ground plane under the ADC87. If these commons must be run separately, use wide conductor patterns and connect a 0.01µF ceramic capacitor from each power supply to the ground plane. Locate the capacitors close to the converter.

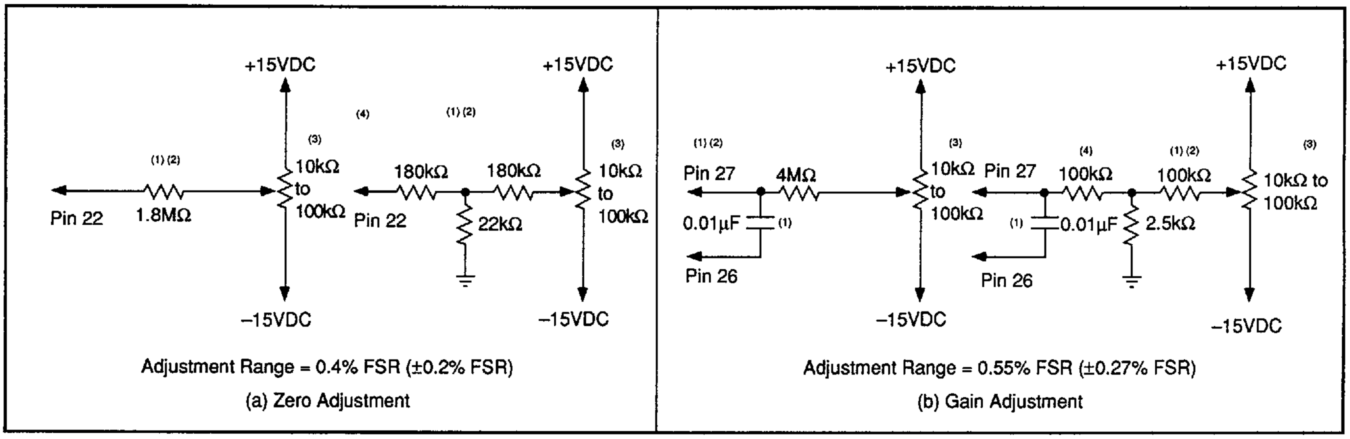
7.3 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1µF tantalum capacitor and a 0.01µF ceramic capacitor from each power supply to the ground plane. Locate the capacitors close to the converter.

7.4 Optional External Zero and Gain Adjustments. The ADC87 zero error and gain error are factory laser-trimmed to position the staircase transfer function within Table I specifications. Optionally, two adjustments null zero error and gain error (see Figure 6).

Zero adjustment moves the entire staircase left to right. For unipolar ranges, –FS, 0VDC, is nulled. For bipolar ranges, midscale, 0VDC, is nulled. (Alternately, bipolar –FS may be nulled.)

Gain adjustment adjusts the span of the staircase. Adjustment effectively rotates the staircase about –FS. For unipolar and bipolar ranges, zero adjustment should be made first, then +FS error is nulled.

Adjustments should be made after a 10 minute warm-up. Fixed, selected resistors may be substituted for the potentiometers after the adjustments have been determined, if desired. If adjustments are not used, pin 22 (zero adjust) should only be connected as required for analog input range selection and pin 27 (gain adjust) should be either grounded (recommended) or open.



NOTES: (1) Locate as close as possible to the converter to minimize noise pickup. (2) 5% carbon composition or better. (3) Use multiburn potentiometers with 100ppm/°C TCR or less to minimize drift with temperature. (4) An attenuator network may be substituted for the series resistor for lower impedance and lower noise susceptibility.

FIGURE 6. Optional External Zero and Gain Circuit Adjustment Circuits.

7.4.1 Zero Adjustment Procedure. For the selected unipolar range, apply the analog input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition ideally occurs, 0VDC + 1/2LSB. While continuously converting, adjust the zero potentiometer until the transition "flickers."

For the selected bipolar range, apply the analog input voltage at which the 1000 0000 0000 to 0111 1111 1111 transition ideally occurs, 0VDC – 1/2LSB. While continuously converting, adjust the zero potentiometer until the transition "flickers."

7.4.2 Gain Adjustment Procedure. Make zero adjustment first. For all input ranges, apply the analog input voltage at which the 0000 0000 0001 to 0000 0000 0000 transition ideally occurs, +FS –3/2LSB. While continuously converting, adjust the gain potentiometer until the transition "flickers."

For the selected bipolar range, repeat zero and gain adjustments as they are interactive.

7.5 Start Convert and Status. To start a conversion, a positive pulse with a minimum pulse width of 50ns must be applied to the Start Convert terminal, pin 21. The trailing edge (falling edge) resets the converter, starts the internal clock and initiates a conversion. The Start Convert input must remain Logic 0 during conversion, as the internal clock is stopped by Logic 1 and the output will be erroneous. Another Start Convert pulse during a conversion does not reset and restart a conversion; it may momentarily stop the internal clock and produce an erroneous output.

Status Output, pin 20, is Logic 1 during conversion. When a conversion is complete, Status drops to Logic 0 and the internal clock is turned off. Refer to the Timing Diagram, Figure 4.

7.6 Internal Clock and Clock Rate. The ADC87 is specified and tested using the internal clock. The internal clock is factory adjusted to 1.3MHz with Clock Rate, pin 17, connected to 0VDC (Digital Common). Under these conditions, the ADC87 will meet all the conversion speed and accuracy specifications.

The internal clock frequency may be increased or decreased by applying a positive or negative voltage to Clock Rate, pin 17 (see Figure 7). The circuits shown in Figure 8 may be used. Increasing the clock frequency decreases the conversion time; however, linearity errors increase as shown in Figures 9 and 10. Decreasing the clock frequency is accomplished by using a negative voltage or using an external clock (see paragraph 7.8).

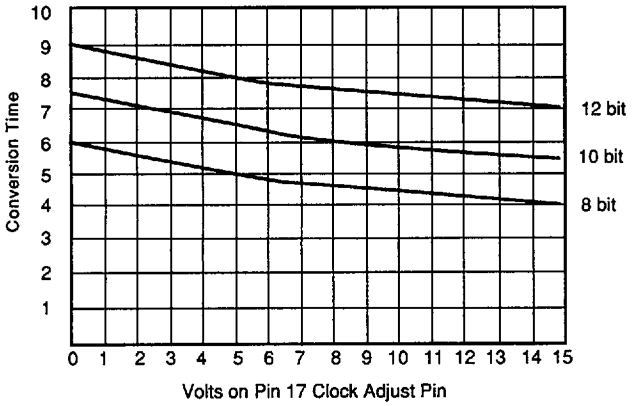
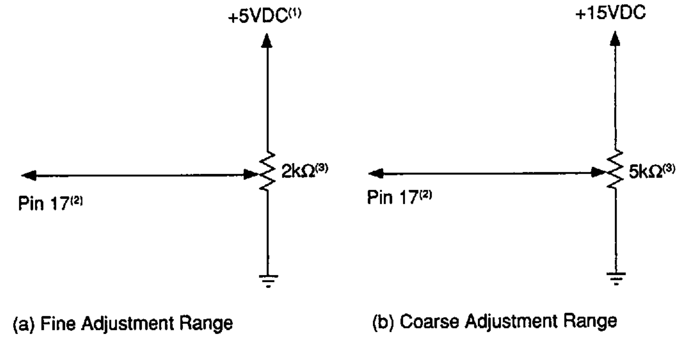


FIGURE 7. Clock Rate Control Voltage.



NOTES: (1) Use negative supply to decrease the clock frequency. (2) Pin 17 is not connected to 0VDC when using clock rate adjustment potentiometer. (3) Multiturn potentiometer with 100ppm/°C TCR or less.

FIGURE 8. Clock Rate Adjustment, Optional.

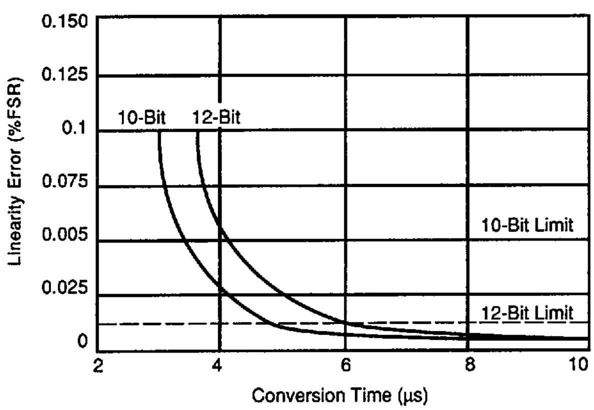


FIGURE 9. Linearity vs Conversion Time.

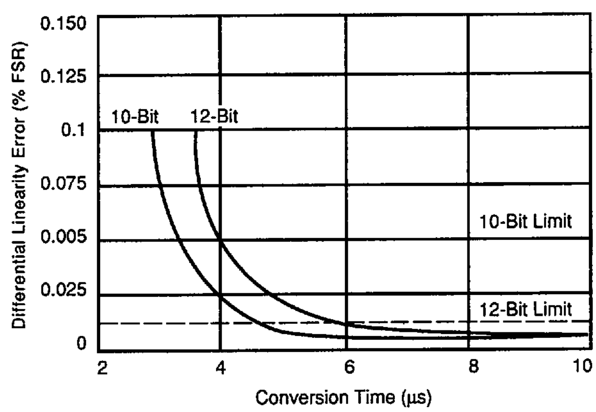


FIGURE 10. Differential Linearity vs Conversion Time.

7.7 Short Cycle. The ADC87 conversion cycle may be stopped before converting all 12 bits. This provides faster conversions to less resolution. For conversions to n bits, connect the n + 1 bit output to Short Cycle, pin 14. The remaining bits are truncated.

Table VI shows a complete cycle and a short cycle to 10 and 8 bits. For 10 bits the internal clock frequency has been increased to provide the minimum conversion time. See Clock Rate, paragraph 7.7.

TABLE VI. Short Cycle Connections.

RESOLUTION (bits)	12	10	8
Connect Pin 17 to(1)	15	16	28
Connect Pin 14 to	16	2	4
Maximum Conversion Speed (µs)(2)	10	6	4
Maximum Nonlinearity at 25°C (% of FSR)	0.012(3)	0.048(4)	0.20(4)

NOTES: (1) Connect only if clock rate control is not used. (2) Maximum conversion speeds to maintain ±1/2LSB nonlinearity error. (3) 12-bit models only. (4) 10- or 12-bit models.