HB526A25672EA Series

131,072-word × 72-bit × 2-bank Synchronous Dynamic RAM Module

HITACHI

ADE-203-614 (Z)
Preliminary
Rev. 0.0
Jul. 5, 1996

Description

The HB526A25672EA belongs to 8byte DIMM family. The HB526A25672EA is a 128k × 72 × 2 banks Synchronous Dynamic RAM Module, mounted 5 pieces of 4-Mbit SDRAM (HM5241605CTT) sealed in TSOP package, 1 piece of 20-bit register (SN74ALVCH16721) sealed inTSSOP package, and 1 piece of 12-bit PLL clock driver (CDC2586PAH) sealed in TQFP package. An outline of the HB526A25672EA is 200-pin Dual tabs socket type package. The HB526A25672EA provides common data inputs and outputs. Decoupling capacitors are mounted beside TSOP on the module board.

Features

- 200-pin socket type package (Dual read out)
  - Outline: 153.70 mm (Length) × 38.10 mm (Height) × 3.80 mm (Thickness)
  - Lead pitch: 1.27 mm
- 3.3V power supply
- Clock frequency: 80 MHz / 66 MHz / 57 MHz
- LVTTL interface
- Data bus width: × 72 (ECC) bit
- Single pulsed $\overline{RAS}$
- 2 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 1/2/4/8/full page (256)
- Programmable burst sequence
  - Sequential/interleave
- Full page burst length capability
  - Sequential burst
  - Burst stop capability
- Programmable $\overline{CAS}$ latency: 2/3/4
- PLL and register buffered except DQ

Preliminary:The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regrding specification.

Hitachi semiconductor

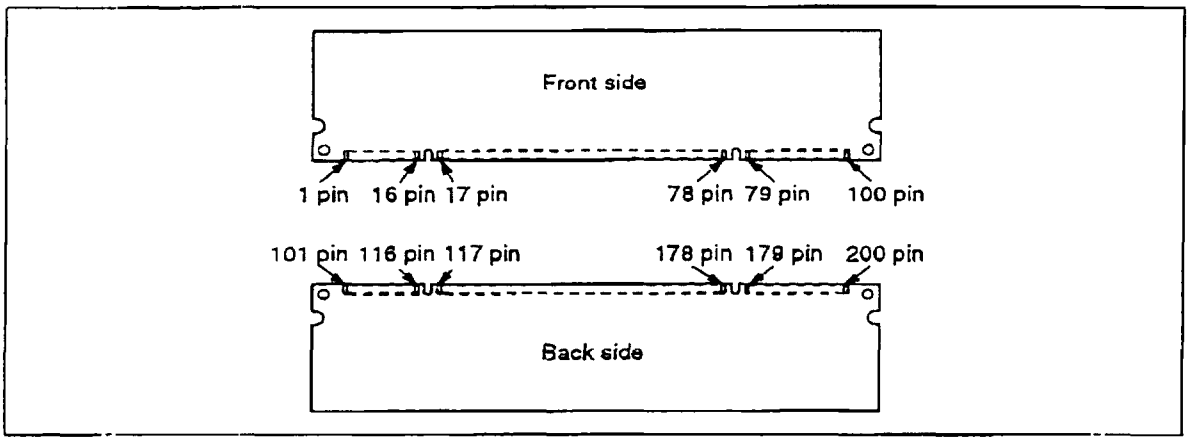
HB526A25672EA Series

- 1024 refresh cycles:16 ms
- 2 variations of refresh
  - — Auto refresh
  - — Self refresh

Ordering Information

Type No.	Frequency	Package	Contact pad
HB526A25672EA-12	80 MHz	200-pin DIMM (dual read out socket type)	Gold
HB526A25672EA-15	66 MHz		
HB526A25672EA-17	57 MHz		

Pin Arrangement



Pin Arrangement (cont.)

Front side						Back side					
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{DD}	35	V_{SS}	69	DQ25	101	NC	135	DQ39	169	DQ22
2	NC	36	DQ41	70	DQ24	102	NC	136	DQ38	170	V_{DD}
3	NC	37	DQ40	71	V_{SS}	103	V_{SS}	137	V_{SS}	171	DQ21
4	NC	38	V_{DD}	72	DQ19	104	NC	138	DQ37	172	DQ20
5	NC	39	A4	73	DQ18	105	NC	139	DQ36	173	V_{SS}
6	ID1	40	A5	74	V_{DD}	106	NC	140	V_{DD}	174	NC
7	ID2	41	V_{SS}	75	DQ17	107	ID3	141	A6	175	NC
8	V_{SS}	42	A8	76	DQ16	108	DQ71	142	A7	176	V_{DD}
9	DQ67	43	NC	77	V_{SS}	109	DQ70	143	V_{SS}	177	NC
10	DQ66	44	V_{DD}	78	NC	110	V_{SS}	144	A9 (BS)	178	V_{SS}
11	V_{DD}	45	NC	79	NC	111	DQ69	145	NC	179	V_{SS}
12	DQ65	46	CKE0	80	V_{DD}	112	DQ68	146	V_{DD}	180	NC
13	DQ64	47	V_{SS}	81	DQ15	113	V_{DD}	147	DQM	181	NC
14	V_{SS}	48	$\overline{CAS}$	82	DQ14	114	NC	148	$\overline{WE}$	182	V_{DD}
15	DQ63	49	NS	83	V_{SS}	115	V_{SS}	149	V_{SS}	183	DQ11
16	DQ62	50	V_{DD}	84	DQ13	116	NC	150	NC	184	DQ10
17	NC	51	V_{SS}	85	DQ12	117	DQ59	151	CK0	185	V_{SS}
18	DQ61	52	$\overline{RAS}$	86	V_{DD}	118	DQ58	152	V_{DD}	186	DQ9
19	DQ60	53	V_{SS}	87	DQ7	119	V_{SS}	153	NC	187	DQ8
20	V_{DD}	54	NC	88	DQ6	120	DQ57	154	$\overline{S0}$	188	V_{DD}
21	NC	55	NC	89	V_{SS}	121	DQ56	155	V_{SS}	189	DQ3
22	NC	56	V_{DD}	90	DQ5	122	V_{DD}	156	NC	190	DQ2
23	V_{SS}	57	A0	91	DQ4	123	DQ55	157	NC	191	V_{SS}
24	NC	58	A1	92	V_{DD}	124	DQ54	158	V_{DD}	192	DQ1
25	NC	59	V_{SS}	93	$\overline{PDE}$	125	V_{SS}	159	A2	193	DQ0
26	V_{DD}	60	DQ35	94	PD1	126	DQ53	160	A3	194	PD5
27	DQ51	61	DQ34	95	PD2	127	DQ52	161	V_{SS}	195	PD6
28	DQ50	62	V_{DD}	96	PD3	128	V_{DD}	162	DQ31	196	PD7
29	V_{SS}	63	DQ33	97	PD4	129	DQ47	163	DQ30	197	PD8
30	DQ49	64	DQ32	98	NC	130	DQ46	164	V_{DD}	198	V_{DD}
31	DQ48	65	V_{SS}	99	NC	131	V_{SS}	165	DQ29	199	NC
32	V_{DD}	66	DQ27	100	V_{SS}	132	DQ45	166	DQ28	200	NC
33	DQ43	67	DQ26			133	DQ44	167	V_{SS}		
34	DQ42	68	V_{DD}			134	V_{DD}	168	DQ23		

Pin Description

Pin name	Function
A0 to A9	Address input — Row address A0 to A8 — Column address A0 to A7 — Bank select address A9 (BS)
DQ0 to DQ71	Data-input/output
$\overline{S0}$	Chip select
$\overline{RAS}$	Row address asserted bank enable
$\overline{CAS}$	Column address asserted
$\overline{WE}$	Write enable
DQM	Input/output mask
CK0	Clock input
CKE0	Clock enable
PD1 to PD8	Presence detect
$\overline{PDE}$	Presence detect enable
ID1, ID2, ID3	ID bit
V_{DD}	Power supply
V_{SS}	Ground
NC	No connection

PD Matrix*1

Pin name	Pin NO.	Function described	PDE = Low -12	PDE = Low -15	PDE = Low -17	PDE = High All	Comments
PD1	94	Module configuration and SDRAM organization	TBD*2	TBD*2	TBD*2	High-Z	
PD2	95		TBD*2	TBD*2	TBD*2	High-Z	
PD3	96		TBD*2	TBD*2	TBD*2	High-Z	
PD4	97		TBD*2	TBD*2	TBD*2	High-Z	
PD5	194	Speed (t_{CYC})	0	1	TBD*2	High-Z	
PD6	195		1	1	TBD*2	High-Z	
PD7	196	Interface	1	1	1	High-Z	Buffered
PD8	197	Write mode	1	1	1	High-Z	word

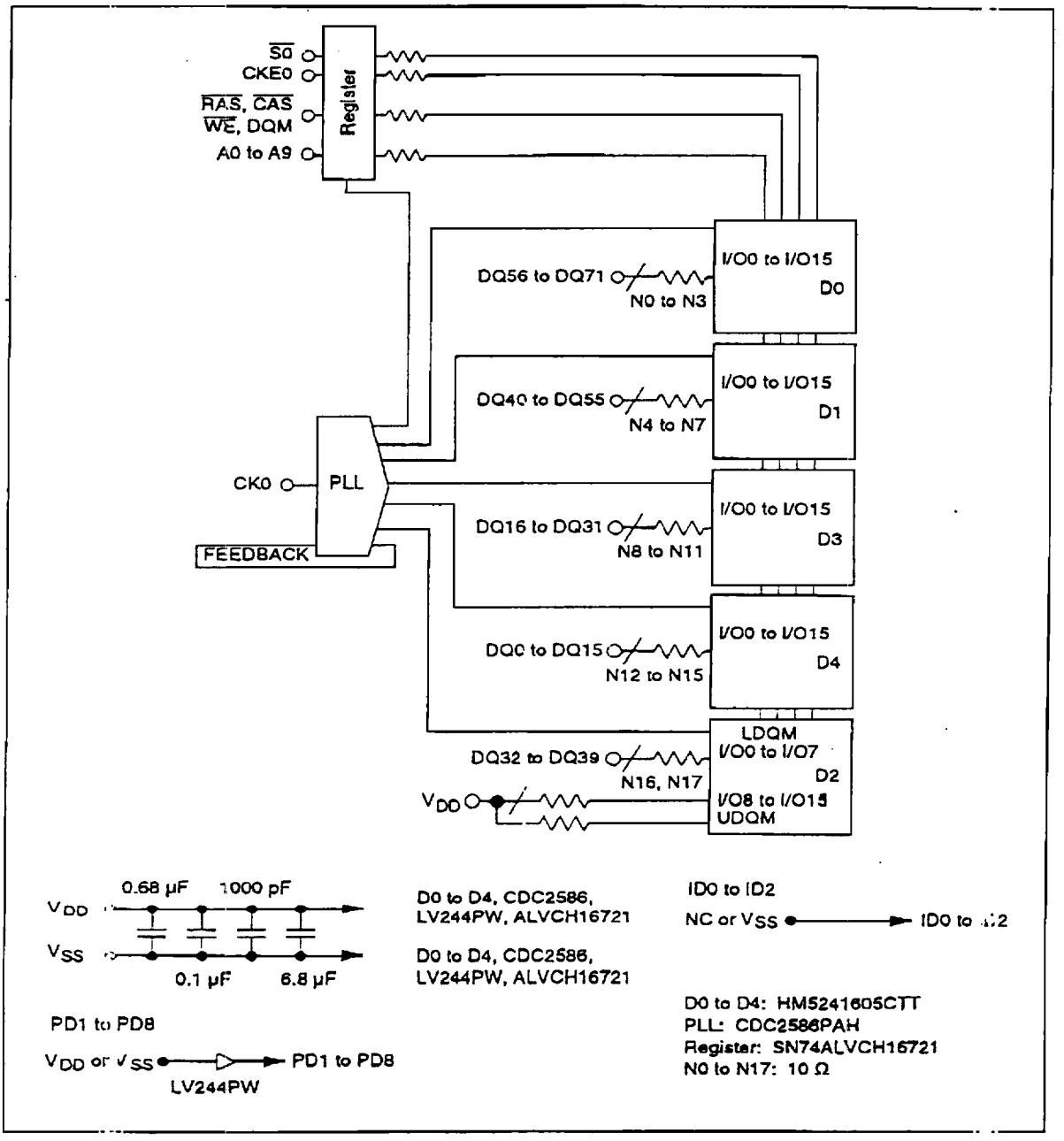
Notes: 1. 0: driven Low, 1: driven High
2. Depend on customer requirement

ID Matrix*1

Pin name	Pin NO.	Function described	ID	Comments
ID1	6	Command interval	1	1 clock
ID2	7	Read precharge timing	1	Early $\overline{RAS}$
ID3	107	Power level	0	Normal

Note: 0: GND, 1: NC

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on any pin relative to V_{SS}	V_T	−0.5 to V_{DD} + 0.5	V	1, 2
Supply voltage relative to V_{SS}	V_{DD}	−0.5 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	8	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	−55 to +125	°C	

Notes: 1. V_{IH} (max) = 5.5 V for pulse width ≤ 5 ns.
2. Respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{DD}	3.0	3.3	3.6	V	1
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.0	—	4.6	V	1, 2
Input low voltage	V_{IL}	−0.3	—	0.8	V	1, 3

Notes: 1. All voltage referred to V_{SS}
2. V_{IH} (max) = 5.5 V for pulse width ≤ 5 ns
3. V_{IL} (min) = −1.0 V for pulse width ≤ 5 ns

DC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB526A25672EA								
		-12		-15		-17				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	770	—	720	—	670	mA	Burst length = 1 t_{RC} = min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	—	155	—	155	—	155	mA	CKE0 = V_{IH}, t_{CK} = min	5
		—	11	—	11	—	11	mA	CKE0 = V_{IL} CK0 = V_{IL} or V_{IH} Fixed	6
		—	490	—	460	—	445	mA	CKE0 = V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	175	—	175	—	175	mA	CKE0 = V_{IH}, t_{CK} = min. DQ = High-Z	1, 2
		—	495	—	465	—	450	mA	CKE0 = V_{IH}, NOP command t_{CK} = min, DQ = High-Z	1, 2, 3
Burst operating current										
($\overline{CAS}$ Latency = 2)	I_{CC4}	—	620	—	620	—	595	mA	t_{CK} = min, BL = 4	1, 2, 4
($\overline{CAS}$ Latency = 3)	I_{CC4}	—	795	—	795	—	770	mA		
($\overline{CAS}$ Latency = 4)	I_{CC4}	—	895	—	820	—	770	mA		
Refresh current	I_{CC5}	—	720	—	645	—	620	mA	t_{RC} = min	
Self refresh current	I_{CC6}	—	305	—	305	—	305	mA	$V_{IH} \geq V_{DD} - 0.2$ $V_{IL} \leq 0.2$ V	7
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	$0 \leq Vin \leq V_{DD}$	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	$0 \leq Vout \leq V_{DD}$ DQ = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CK0 cycles.
4. Input signal transition is once per one CK0 cycle.
5. After power down mode, CK0 operating current.
6. After power down mode, no CK0 operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Max	Unit	Notes
Input capacitance (Address)	C_{IN}	14	pF	1, 3
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CK0, CKE0)	C_{IN}	14	pF	1, 3
Input capacitance ($\overline{S0}$)	C_{IN}	14	pF	1, 3
Input capacitance (DQM)	C_{IN}	14	pF	1, 3
Input/Output capacitance (DQ0 to DQ63)	$C_{I/O}$	27	pF	1, 2, 3

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB526A25672EA							
		-12		-15		-17			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
System clock cycle time ($\overline{CAS}$ Latency = 2)	t_{CK}	30	—	30	—	35	—	ns	1
($\overline{CAS}$ Latency = 3)	t_{CK}	15	—	15	—	17.5	—		
($\overline{CAS}$ Latency = 4)	t_{CK}	12.5	—	15	—	17.5	—		
CK0 high pulse width	t_{CKH}	0.45 × t_{CK}	—	0.45 × t_{CK}	—	0.45 × t_{CK}	—	ns	1
CK0 low pulse width	t_{CKL}	0.45 × t_{CK}	—	0.45 × t_{CK}	—	0.45 × t_{CK}	—	ns	1
Access time from CK0 ($\overline{CAS}$ Latency = 2)	t_{AC}	—	26.6	—	30.6	—	34.6	ns	1, 2
($\overline{CAS}$ Latency = 3)	t_{AC}	—	13.6	—	15.6	—	17.1		
($\overline{CAS}$ Latency = 4)	t_{AC}	—	11.6	—	13.6	—	16.1		
Data-out hold time ($\overline{CAS}$ Latency = 2)	t_{OH}	3.4	—	3.4	—	3.4	—	ns	1, 2
($\overline{CAS}$ Latency = 3, 4)	t_{OH}	2.4	—	2.4	—	2.4	—		
CK0 to Data-out low impedance	t_{LZ}	–0.6	—	–0.6	—	–0.6	—	ns	1, 2
CK0 to Data-out high impedance ($\overline{CAS}$ Latency = 2)	t_{HZ}	—	12.6	—	15.6	—	17.6	ns	1, 3
($\overline{CAS}$ Latency = 3, 4)	t_{HZ}	—	9.6	—	10.6	—	12.6		
Data-in setup time	t_{DS}	4.1	—	4.6	—	4.6	—	ns	1
Data in hold time	t_{DH}	2.1	—	2.6	—	2.6	—	ns	1
Address setup time	t_{AS}	3.7	—	3.7	—	3.7	—	ns	1
Address hold time	t_{AH}	0.6	—	0.6	—	0.6	—	ns	1
CKE0 setup time	t_{CES}	3.7	—	3.7	—	3.7	—	ns	1, 4

AC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (cont)

		HB526A25672EA							
		-12		-15		-17			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
CKE0 setup time for power down exit	t_{CESP}	3.7 + 1t_{CK}	—	3.7 + 1t_{CK}	—	3.7 + 1t_{CK}	—	ns	1, 5
CKE0 hold time	t_{CEH}	0.6	—	0.6	—	0.6	—	ns	1
CKE0 hold time for CKE0 function exit	t_{CEHP}	3.7 + 1t_{CK}	—	3.7 + 1t_{CK}	—	3.7 + 1t_{CK}	—	ns	1, 6
Command ($\overline{S0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	3.7	—	3.7	—	3.7	—	ns	1
Command ($\overline{S0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	0.6	—	0.6	—	0.6	—	ns	1
Ref/Active to Ref/Active command period	t_{RC}	110	—	110	—	120	—	ns	1
Active to precharge command period	t_{RAS}	70	10000	70	10000	75	10000	ns	1
Active to precharge on full page mode	t_{RASC}	—	80000	—	80000	—	80000	ns	1
Active command to column command (same bank)	t_{RCD}	30	—	30	—	35	—	ns	1
Precharge to active command period	t_{RP}	30	—	34	—	34	—	ns	1
The last data-in the precharge lead time	t_{RWL}	25	—	30	—	35	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	25	—	30	—	35	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.40 V.

2. Access time is measured at 1.40 V. Load condition is C_L = 50 pF with current source.

3. t_{HZ} (max) defines the time at which the outputs achives ± 200 mV. Load condition is C_L = 5 pF with current source.

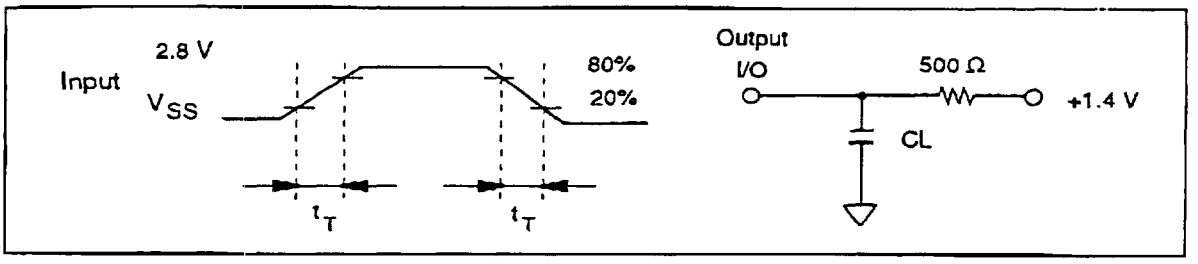
4. t_{CES} define CKE0 setup time to CK0 rising edge except power down exit command and active clock suspend exit command.

5. t_{CESP} define CKE0 setup time to CK0 rising edge for power down exit command and active clock suspend exit command.

6. t_{CEHP} define CLK rising edge to CKE0 hold time for self refresh exit command, power down exit command and active clock suspend exit command.

Test Conditions

- Input and output timing reference levels: 1.4 V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter	Symbol	HB526A25672EA -12		-15		-17		Note
Frequency (MHz)		80	40	66	33	57	28.5	
t_{CK} (ns)		12.5	25	15	30	17.5	35	
Active command to column command (same bank)	t_{RCD}	3	2	2	1	2	1	1
Active command to active command (same bank)	t_{RC}	9	5	8	5	7	4	= [t_{RAS} + t_{RP}] 1
Active command to precharge command (same bank)	t_{RAS}	6	3	5	3	5	3	1
Precharge command to active command (same bank)	t_{RP}	3	2	3	2	2	1	1
Last data input to precharge command (same bank)	t_{RWL}	2	1	2	1	2	1	1
Active command to active command (different bank)	t_{RRD}	2	1	2	1	2	1	1
Last data in to active command (Auto precharge, same bank)	t_{APW}	5	3	5	3	4	2	= [t_{RWL} + t_{RP}]
Self refresh exit to command input	t_{SEC}	9	5	8	4	7	4	= [t_{RC}]
Precharge command to high impedance ($\overline{CAS}$ latency = 4)	t_{HZP}	4	4	4	4	4	4	
($\overline{CAS}$ latency = 3)	t_{HZP}	—	3	3	3	3	3	
($\overline{CAS}$ latency = 2)	t_{HZP}	—	—	—	2	—	2	
Last data out to active command (auto precharge) (same bank) ($\overline{CAS}$ latency = 4)	t_{APR}	2	1	2	1	1	0	
($\overline{CAS}$ latency = 3)	t_{APR}	2	1	2	1	—	1	
($\overline{CAS}$ latency = 2)	t_{APR}	—	—	—	2	—	1	= [t_{RP}] − 1

Relationship Between Frequency and Minimum Latency (cont)

Parameter	Symbol	HB526A25672EA -12		-15		-17		Note
Frequency (MHz)		80	40	66	33	57	28.5	
t_{CK} (ns)		12.5	25	15	30	17.5	35	
Last data out to precharge (early precharge) ($\overline{CAS}$ latency = 4)	l_{EP}	–2	–2	–2	–2	–2	–2	
($\overline{CAS}$ latency = 3)	l_{EP}	–1	–1	–1	–1	–1	–1	
($\overline{CAS}$ latency = 2)	l_{EP}	—	—	—	0	—	0	
Column command to column command	l_{CCD}	1	1	1	1	1	1	
Write command to data in latency	l_{WCD}	1	1	1	1	1	1	
DQM to data in	l_{DID}	1	1	1	1	1	1	
DQM to data out	l_{DOD}	3	3	3	3	3	3	
CKE0 to CK0 disable	l_{CLE}	1	1	1	1	1	1	
Register set to active command	t_{RSA}	2	1	2	1	2	1	
$\overline{S0}$ to command disable	l_{COD}	0	0	0	0	0	0	
Power down exit to command input	l_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold ($\overline{CAS}$ latency = 4)	l_{BDR}	3	3	3	3	3	3	
($\overline{CAS}$ latency = 3)	l_{BDR}	2	2	2	2	2	2	
($\overline{CAS}$ latency = 2)	l_{BDR}	—	—	—	1	—	1	
Burst stop to output high impedance ($\overline{CAS}$ latency = 4)	l_{BDH}	4	4	4	4	4	4	
($\overline{CAS}$ latency = 3)	l_{BDH}	3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)	l_{BDH}	2	2	2	2	2	2	
Burst stop to write data ignore	l_{BDW}	2	2	2	2	2	2	

Note: 1. t_{RCD} to t_{RAD} are recommended value.

Pin Functions

CK0 (input pin): CK0 is the master clock input to this pin. The other input signals are referred at CK0 rising edge.

$\overline{S0}$ (input pin): When $\overline{S0}$ is Low, the command input cycle becomes valid. When $\overline{S0}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins): Although these pin names are the same as those of conventional DRAM modules, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A8 (input pins): Row address (AX0 to AX8) is determined by A0 to A8 level at the bank active command cycle CK0 rising edge. Column address (AY0 to AY7) is determined by A0 to A7 level at the read or write command cycle CK0 rising edge. And this column address becomes burst access start address. A8 defines the precharge mode. When A8 = High at the precharge command cycle, both banks are precharged. But when A8 = Low at the precharge command cycle, only the bank that is selected by A9 (BS) is precharged.

A9 (input pin): A9 is a bank select signal (BS). The memory array of the HB526A25672EA is divided into bank 0 and bank 1, both which contain 512 row × 256 column × 72 bits. If A9 is Low, bank 0 is selected, and if A9 is High, bank 1 is selected.

CKE0 (input pin): This pin determines whether or not the next CK0 is valid. If CKE0 is High, the next CK0 rising edge is valid. If CKE0 is Low, the next CK0 rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQM (input pins): Read operation: If DQM is High, the output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z.

Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.

DQ0 to DQ71 (DQ pins): Data is input to and output from these pins. These pins are the same as those of a conventional DRAM module.

V_{DD} (power supply pins): 3.3 V is applied.

V_{SS} (power supply pins): Ground is connected.

Command Operation

Command Truth Table

The synchronous DRAM module recognizes the following commands sepcified by the $\overline{S0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE0 n - 1	CKE0 n	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A9	A8	A0 to A7
Ignore command	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop in full page	BST	H	×	L	H	H	L	×	×	×
Column address and read command	READ	H	×	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	×	L	H	L	H	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	×	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	×	H	×
Refresh	REF/SELF	H	V	L	L	L	H	×	×	×
Mode register set	MRS	H	×	L	L	L	L	V	V	V

Note: H: V_{IH}. L: V_{IL}. x: V_{IH} or V_{IL}. V: Valid address input

Ignore command [DESL]: When this command is set ($\overline{S0}$ is High), the synchronous DRAM module ignore command input at the clock. However, the internal status is held.

No operation [NOP]: This command is not an execution command. However, the internal operations continue.

Burst stop in full-page [BST]: This command stops a full-page burst operation (burst length = full-page (256)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for a full-page of data (256), it automatically returns to the start address, and input/output is performed repeatedly.

Column address strobe and read command [READ]: This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY7) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READ A]: This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4, or 8. When the burst length is full-page (256), this command is illegal.

Column address strobe and write command [WRIT]: This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7) and the bank select address (A9) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7) and the bank select address (A9).

Write with auto-precharge [WRIT A]: This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4, or 8, or after a single write operation. When the burst length is full-page (256), this command is illegal.

Row address strobe and bank activate [ACTV]: This command activates the bank that is selected by A9 (BS) and determines the row address (AX0 to AX8). When A9 is Low, bank 0 is activated. When A9 is High, bank 1 is activated.

Precharge selected bank [PRE]: This command starts precharge operation for the bank selected by A9. If A9 is Low, bank 0 is selected. If A9 is High, bank 1 is selected.

Precharge all banks [PALL]: This command starts a precharge operation for all banks.

Refresh [REF/SELF]: This command starts the refresh operation. There are two types of refresh oepration, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE0 truth table section.

Mode register set [MRS]: Synchronous DRAM module has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A9) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE0 n - 1	n	DQM
Write enable/output enable	ENB	H	×	L
Write inhibit/output disable	MASK	H	×	H

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
I_{DDO} is needed.

The HB526A25672EA series can mask input/output data by means of DQM. During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output. During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the HB526A25672EA operating instructions.

CKE0 Truth Table

Current state	Function		CKE0 n-1	CKE0 n	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry		H	L	H	×	×	×	×
Any	Clock suspend		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	Auto refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Idle	Power down entry		H	L	L	H	H	H	×
			H	L	H	×	×	×	×
Self-refres	Self refresh exit	SELFX	L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Power down	Power down exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.

Clock suspend mode entry: The synchronous DRAM module enters clock suspend mode from active mode by setting CKE0 to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

ACTIVE clock suspend: This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

READ suspend and READ A suspend: The data being output is held (and continues to be output).

WRITE suspend and WRIT A suspend: In this mode, external signals are not accepted. However, the internal state is held.

Clock suspend: During clock suspend mode, keep the CKE0 to Low.

Clock suspend mode exit: The synchronous DRAM module exits from clock suspend mode by setting CKE0 to High during the clock suspend state.

IDLE: In this state, all banks are not selected, and completed precharge operation.

Auto refresh command [REF]: When this command is input from the IDLE state, the synchronous DRAM module starts auto refresh operation. (The auto refresh is the same as the CBR refresh of conventional DRAM module.) During the auto refresh operation, refresh address and bank select address are generated inside the synchronous DRAM module. For every auto refresh cycle, the internal address counter is updated. Accordingly, 1024 times are required to refresh the entire memory. Before exicuting the auto refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto refresh, no precharge command is required after auto refresh.

Self refresh entry [SELF]: When this command is input during the IDLE state, the synchronous DRAM module starts self refresh operation. After the execution of this command, self refresh continues while CKE0 is Low. Since self refresh is performed internally and automatically, external refresh operations are unnecessary.

Power down mode entry: When this command is executed during the IDLE state, the synchronous DRAM module enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

Self refresh exit: When this command is executed during self refresh mode, the synchronous DRAM module can exit from self refresh mode. After exiting from self refresh mode, the synchronous DRAM module enters the IDLE state.

Power down exit: When this command is executed at the power down mode, the synchronous DRAM module can exit from power down mode. After exiting from power down mode, the synchronous DRAM module enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM module.

Current state	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	×	×	×	×	DESL	Enter IDLE after t_{RP}
	L	H	H	H	×	NOP	Enter IDLE after t_{RP}
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A8	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	ILLEGA
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A8	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set

Current state	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Row active	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A8	READ/READ A	Begin read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[*3]
	L	L	H	L	BA, A8	PRE, PALL	Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop to full page
	L	H	L	H	BA, CA, A8	READ/READ A	Continue burst read to $\overline{CAS}$ latency and new read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[*3]
	L	L	H	L	BA, A8	PRE, PALL	Term burst read and Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[*3]
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Current state	$\overline{S0}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop on full page
	L	H	L	H	BA, CA, A8	READ/READ A	Term burst and new read
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	Term burst and new write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[*3]
	L	L	H	L	BA, A8	PRE, PALL	Term burst write and precharge[*2]
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank[*3]
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh (auto refresh)	H	×	×	×	×	DESL	Enter IDLE after t_{RC}
	L	H	H	H	×	NOP	Enter IDLE after t_{RC}
	L	H	H	L	×	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A8	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A8	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A8	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{RWL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOR] or [BST]: When these commands are executed, the synchronous DRAM module enters the IDLE state after t_{RP} has elapsed from the completion of precharge.

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM module enters refresh mode (auto refresh or self refresh).

To [MRS]: The synchronous DRAM module enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read oepration starts. (However, an interval of t_{RCD} is requried.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM module to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is requried.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM module enters precharge mode.

From [READ with AUTO PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM module then enters precharge mode.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM module then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

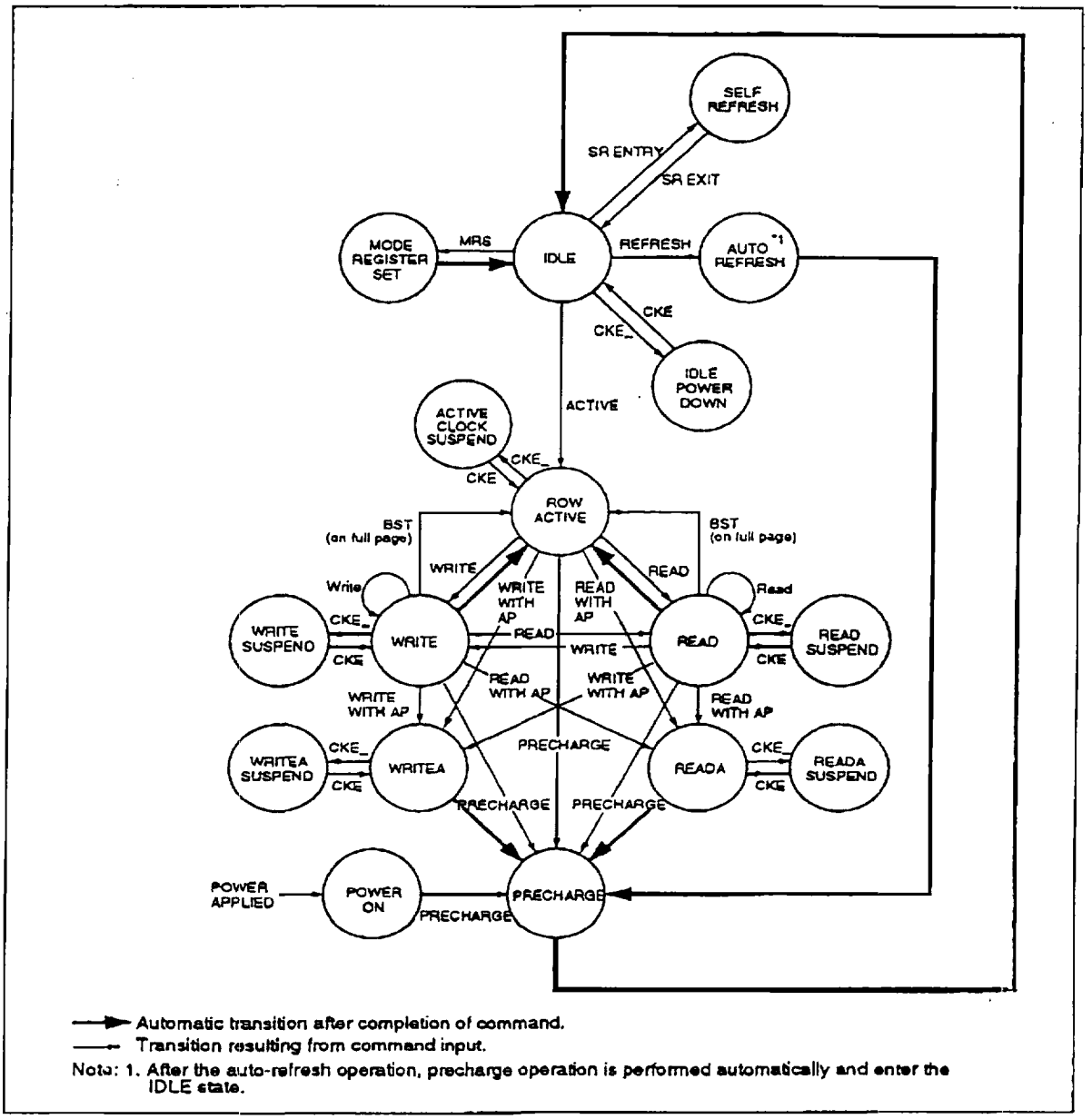
To [DESL], [NOP]: These commands continue write operations until the burst is completed, and the synchronous DRAM module enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM module automatically enters the IDLE state.

Simplified State Diagram



Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A9) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

A9 and A8: (OPCODE): The synchronous DRAM module has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

Burst read and BURST WRITE: Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

Burst read and SINGLE WRITE: Data is only written to the column address specified during the write cycle, regardless of the burst length.

A7: Keep this bit Low at the mode register set cycle.

A6, A5, A4: (LMODE): These pins specify the $\overline{CAS}$ latency.

A3: (BT): A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

A2, A1, A0: (BL): These pins specify the burst length.

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE		0	LMODE			BT	BL		

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	R
0	0	1	2
0	1	0	3
0	1	1	4
1	×	×	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

A9	A8	Write mode
0	0	Burst read and burst write
0	1	R
1	0	Burst read and SINGLE WRITE
1	1	R

F.P. = Full Page (256)
R is Reserved (inhibit)
x = 0 or 1

Burst Sequence

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0.

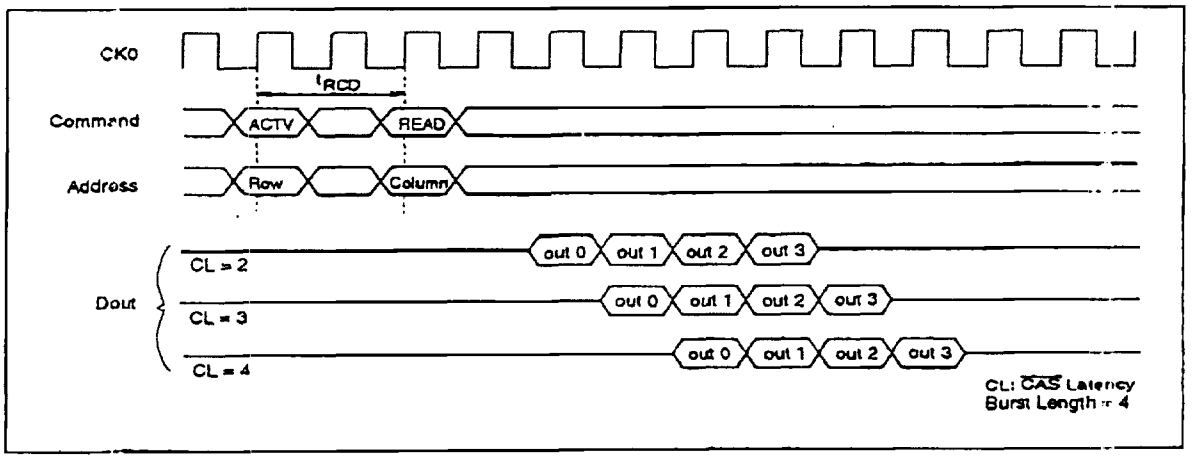
Operation of HB526A25672EA Series

Read/Write Operations

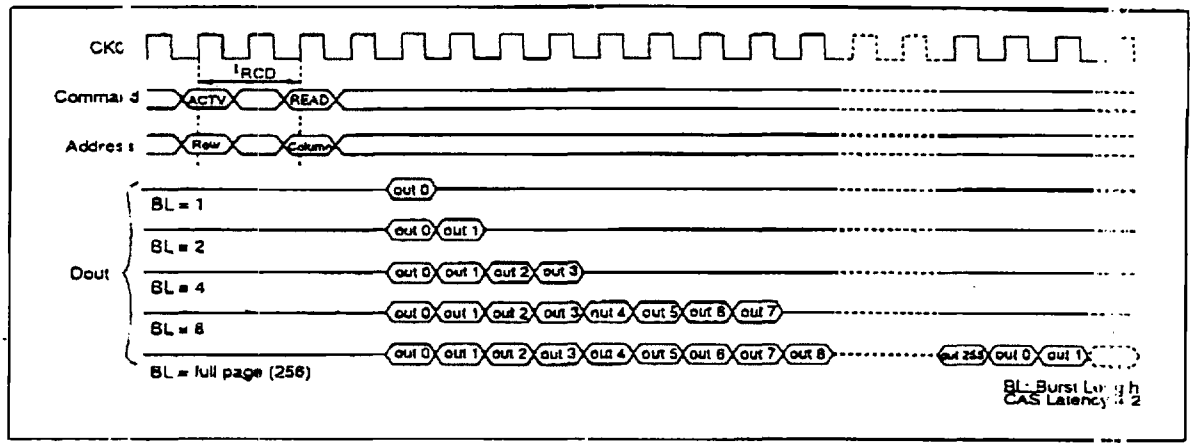
Bank active: Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Either bank 0 or bank 1 is activated according to the status of the A9 pin, and the row address (AX0 to AX8) is activated by the A0 to A8 pins at the bank active command cycle. An interval of t_{RCD} is requried between the bank active command input and the following read/write command input.

Read operation: A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CAS}$ Latency-1) cycle after read command set. HB526A25672EA series can perform a burst read operation. The burst length can be set to 1, 2, 4, 8 or full-page (256). The start address for a burst read is specified by the column address (AY0 to AY7) and the bank select address (A9) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the $\overline{CAS}$ Latency. The $\overline{CAS}$ Latency can be set to 2, 3 or 4. When the burst length is 1, 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output. When the burst length is full-page (256), data is repeatedly output until the burst stop command is input. The $\overline{CAS}$ latency and burst length must be specified at the mode register.

$\overline{CAS}$ Latency



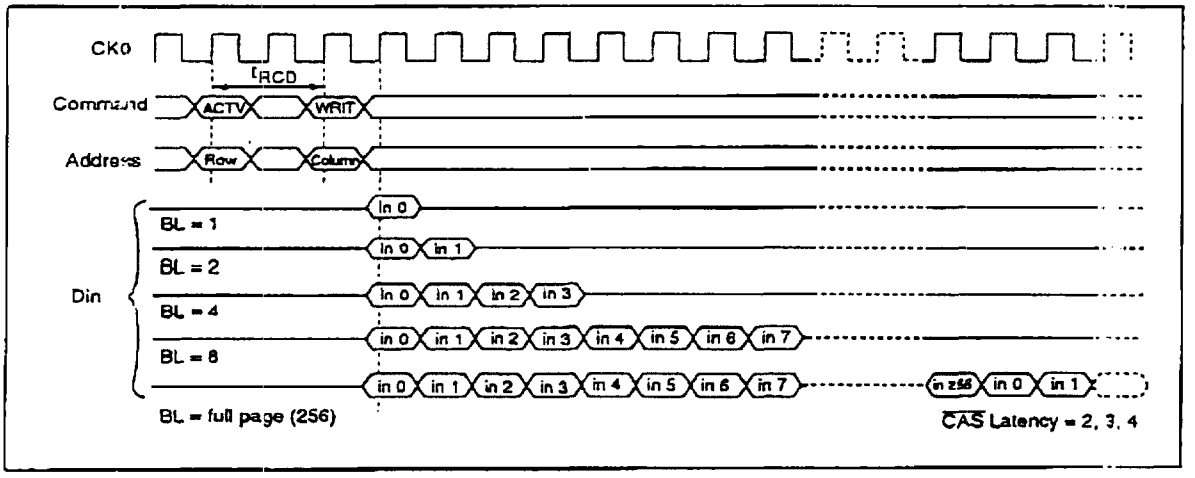
Burst Length



Write operation: Burst write or single write mode is selected by the OPCODE (A9, A8) of the mode register.

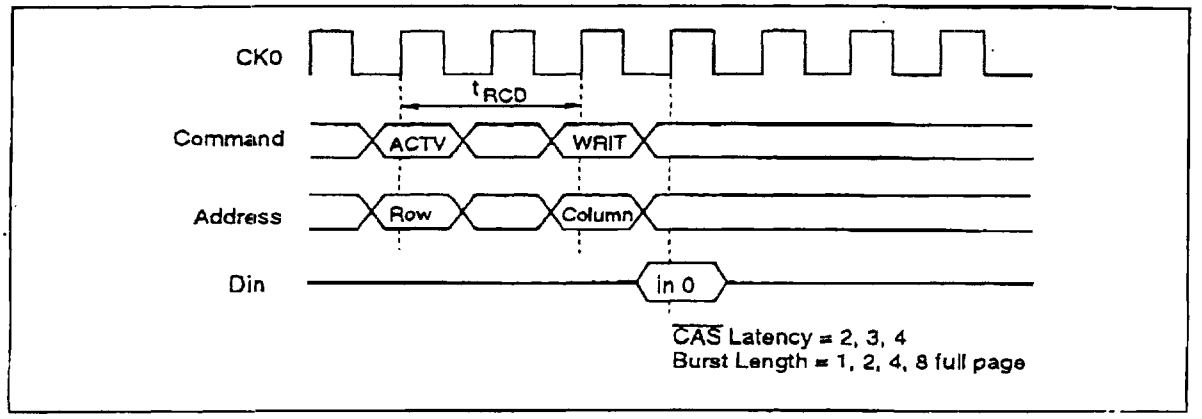
Burst write

A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4, 8, and full-page, like burst read operations. The write start address is specified by the column address (AY0 to AY7) and the bank select address (A9) at the write command set cycle.



Single write

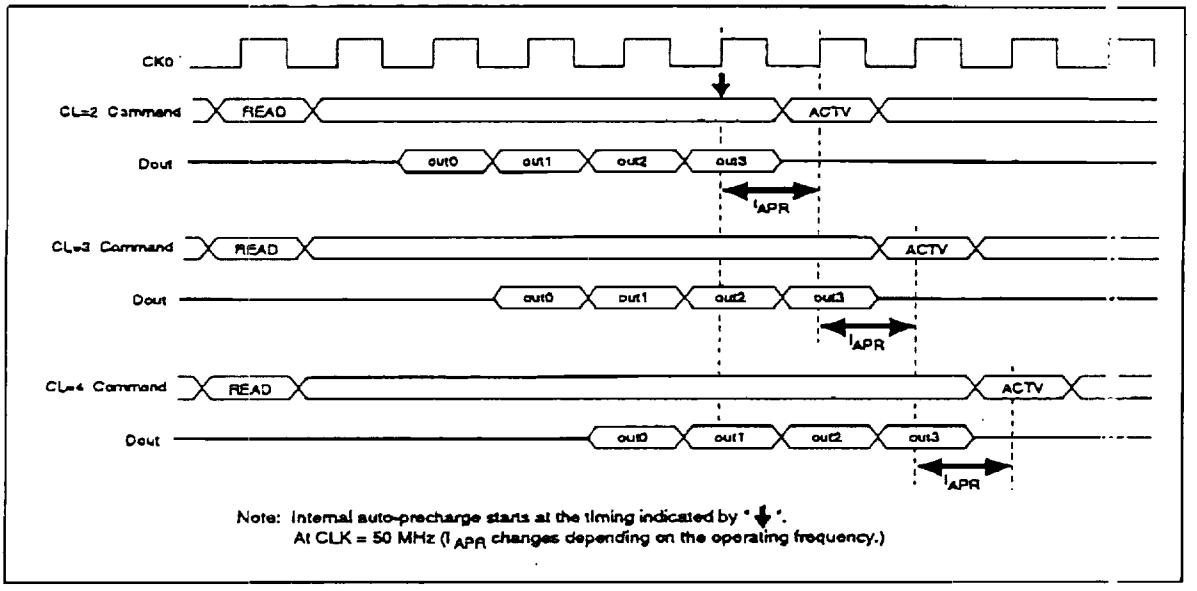
A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is olny written to the column address (AY0 to AY7) and the bank select address (A9) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0).



Auto Precharge

Read with auto precharge: In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by I_{APR} is required before execution of the next command.

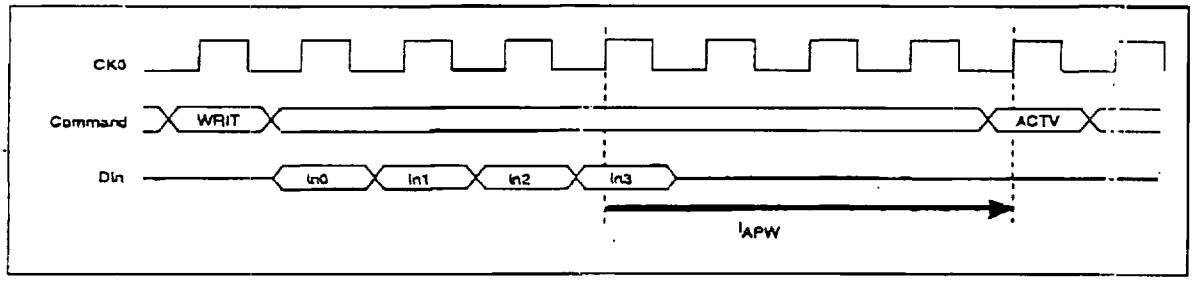
$\overline{CAS}$ latency	Precharge start cycle
4	2 cycle before the final data is output
3	1 cycle before the final data is output
2	same cycle as the final data is output



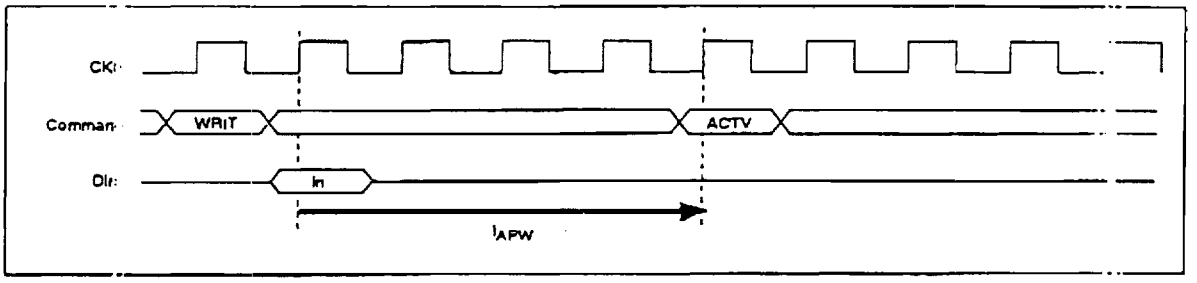
Note: Internal auto-precharge starts at the timing indicated by "↓".
At CLK = 50 MHz (I_{APR} changes depending on the operating frequency.)

Write with auto precharge: In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of t_{APW} is requried between the final valid data input and input of the next command.

Burst Write (Burst Length = 4)



Single Write

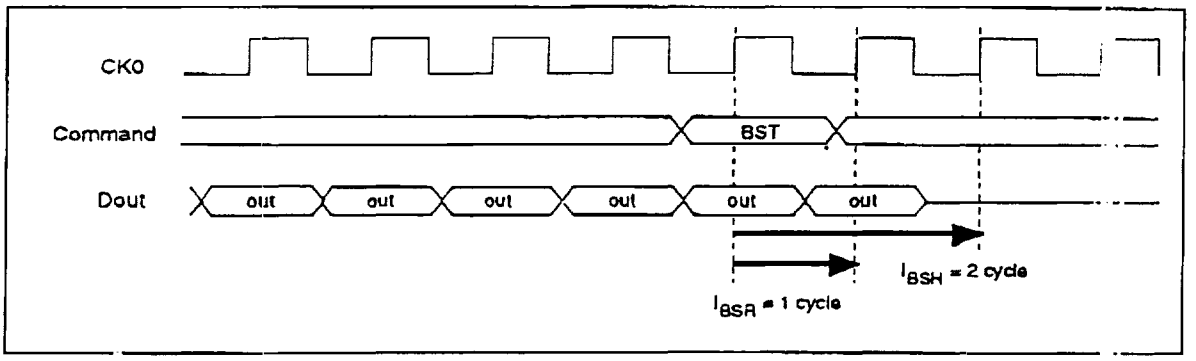


Full-page Burst Stop

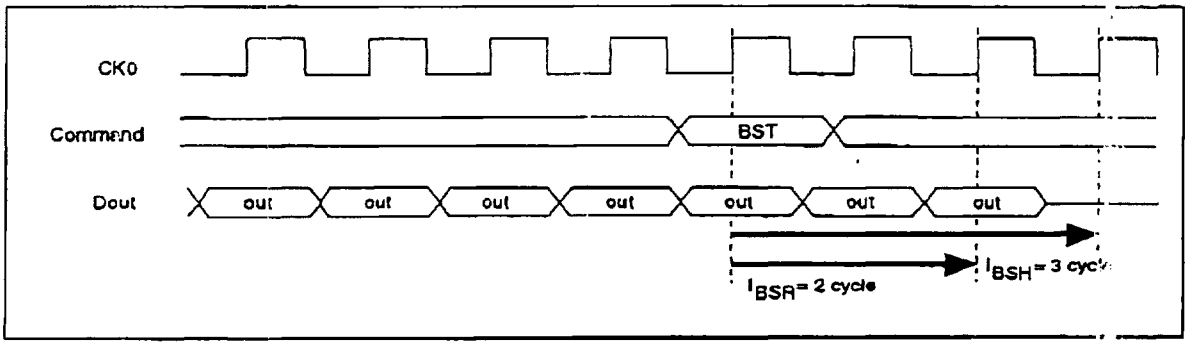
Burst stop command during burst read: The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read. The timing from command input to the last data changes depending on the $\overline{CAS}$ latency setting. In addition, the BST command is valid only during full-page burst mode, and is invalid with burst lengths 1, 2, 4 and 8.

$\overline{CAS}$ latency	BST to valid data	BST to high impedance
2	1	2
3	2	3
4	3	4

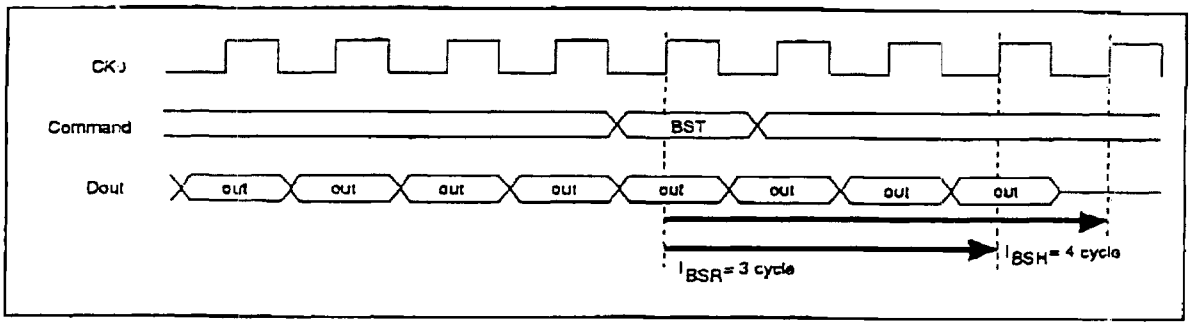
$\overline{CAS}$ Latency = 2, Burst Length = full page



$\overline{CAS}$ Latency = 3, Burst Length = full page

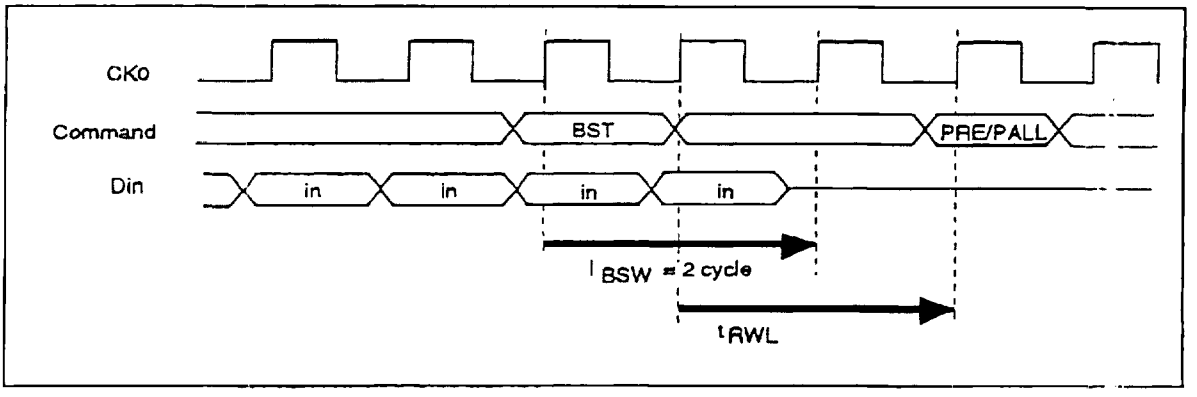


$\overline{\text{CAS}}$ Latency = 4, Burst Length = full page



Burst stop command at burst write: The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same cycle as the BST command and in subsequent cycles. In addition, the BST command is only valid during full-page burst mode, and is invalid with burst lengths of 1, 2, 4 and 8. And an interval of t_{RWL} is requried between the BST command and the next precharge command.

Burst Length = full page

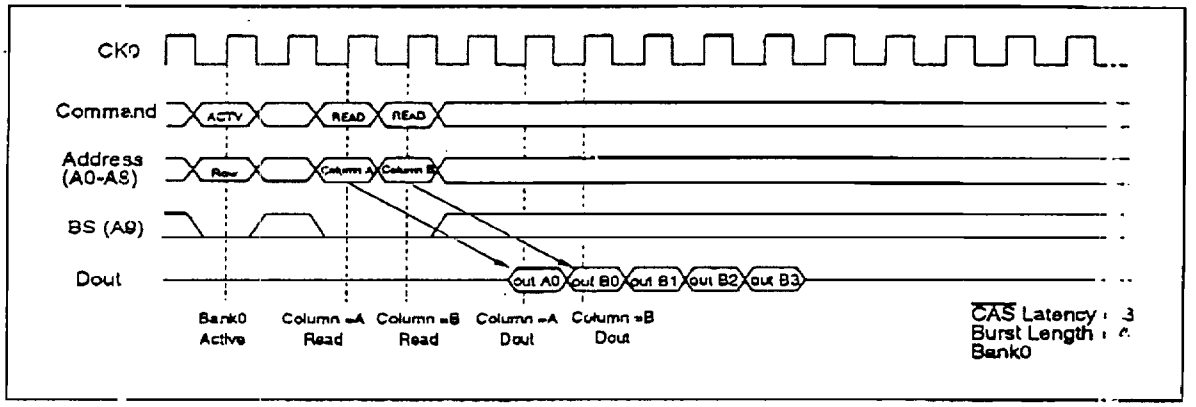


Command Intervals

Read command to Read command interval:

Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

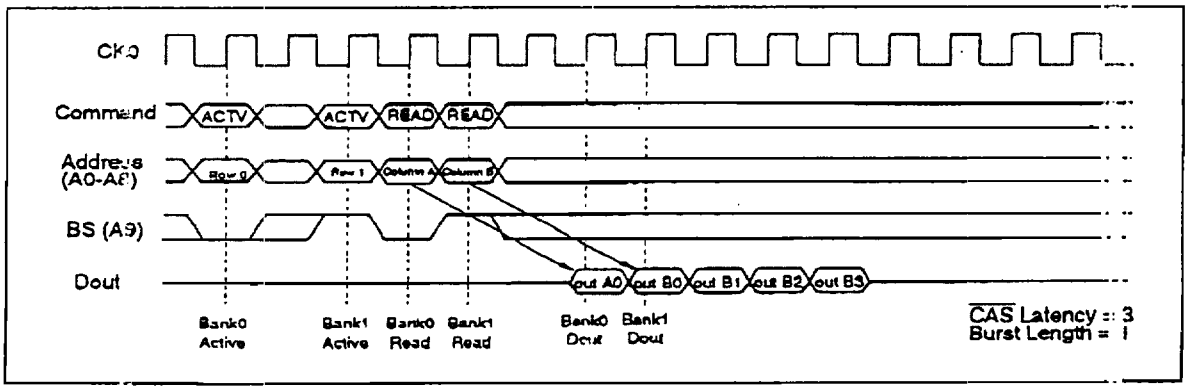
READ to READ Command Interval (same ROW address in same bank)



Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

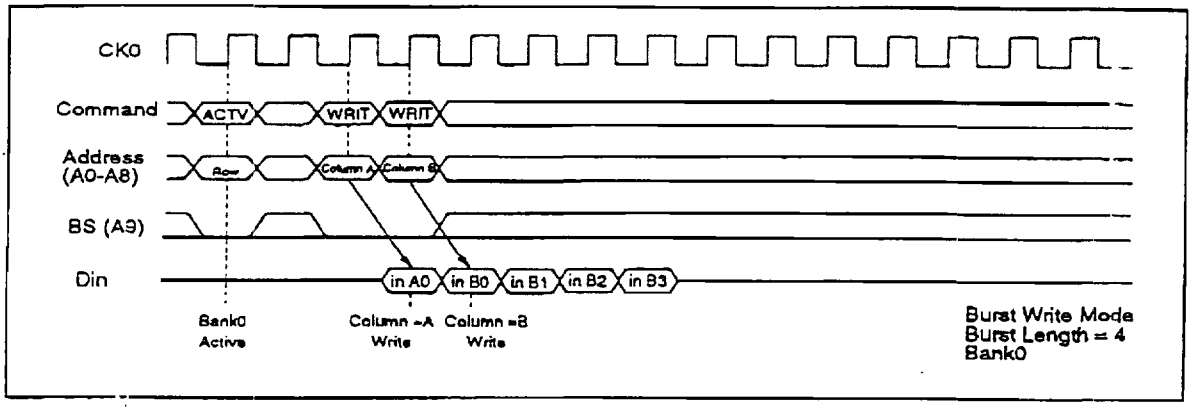
READ to READ Command Interval (different bank)



Write command to Write command interval:

Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle. In the case of burst writes, the second write command has priority.

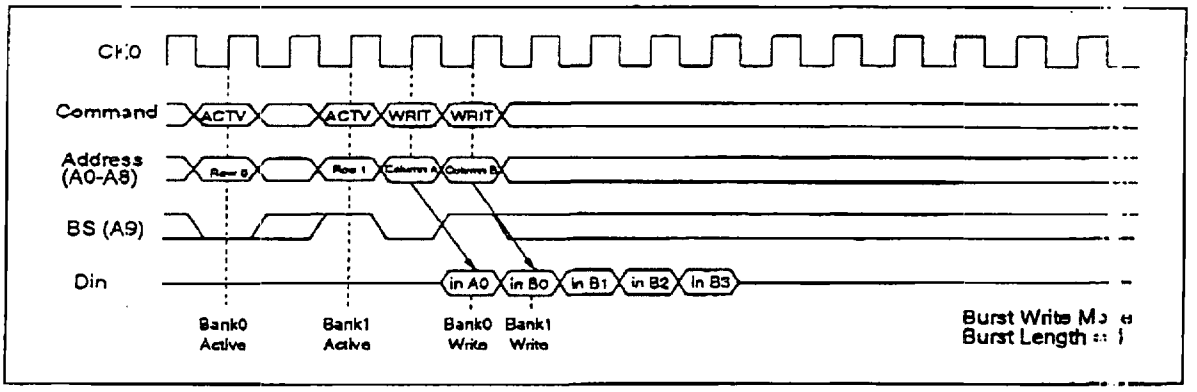
WRITE toWRITE Command Interval (same ROW address in same bank)



Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst writes, the second write command has priority.

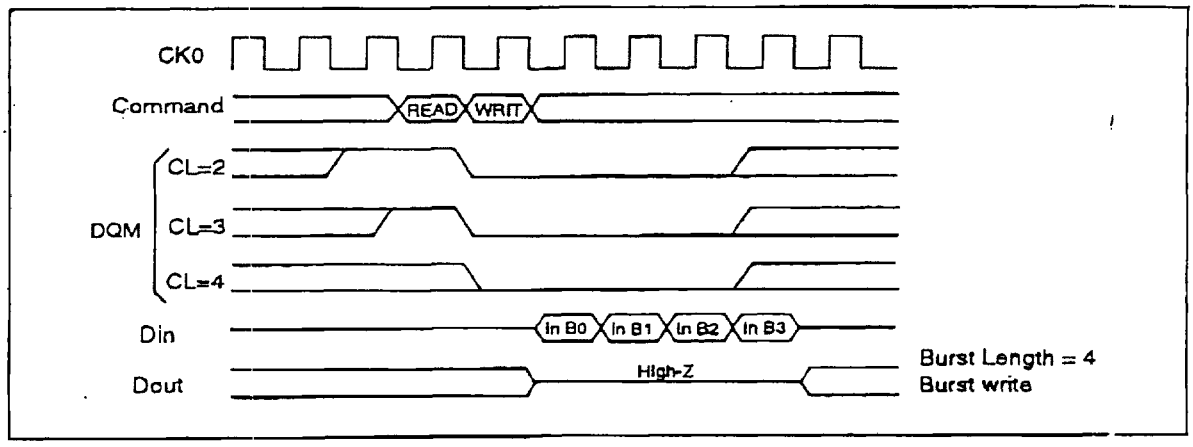
WRITE to WRITE Command Interval (different bank)



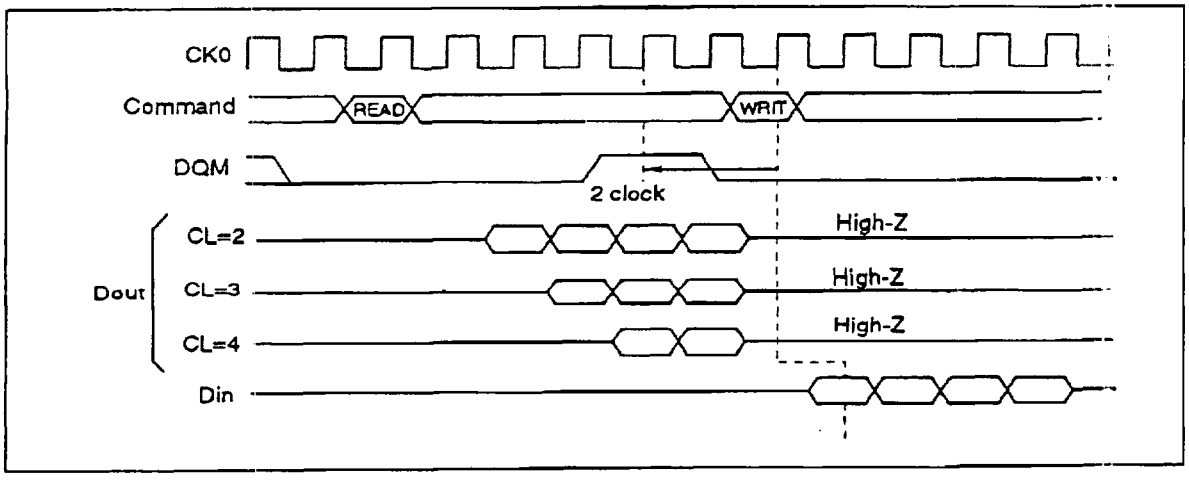
Read command to Write command interval:

Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle. However, DQM must be set High so that the output buffer becomes High-Z before data input.

READ to WRITE Command Interval (1)



READ to WRITE Command Interval (2)



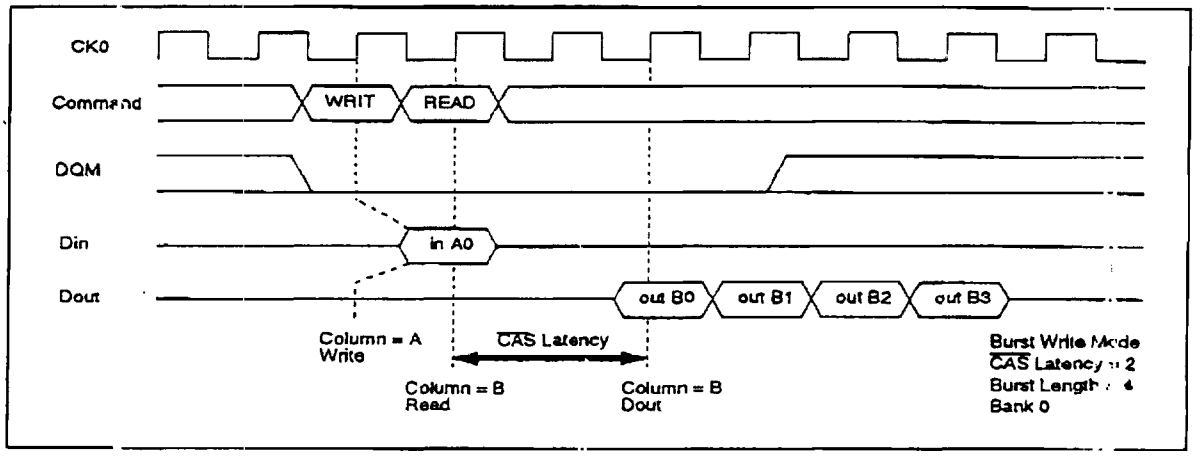
Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command or a bank-active command.

Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

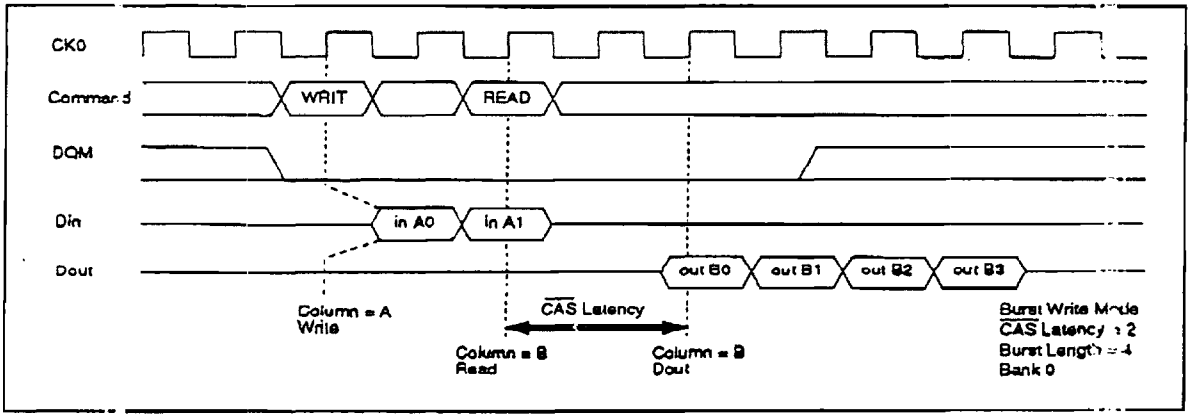
Write command to Read command interval:

Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the write command can be performed after an interval of no less than 1 cycle. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



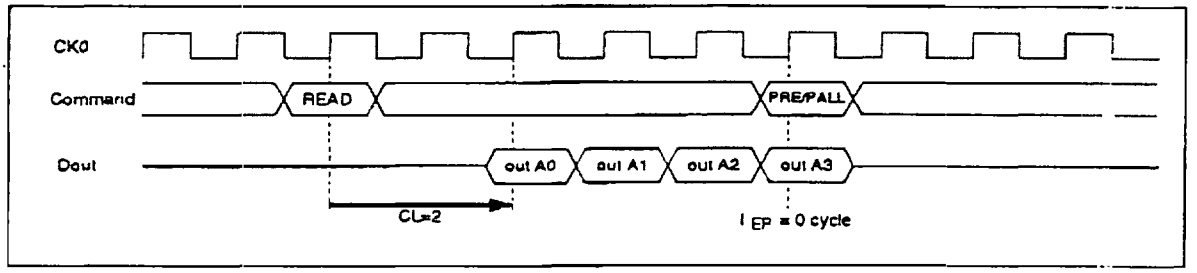
Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed (as in the case of the same bank and the same address).

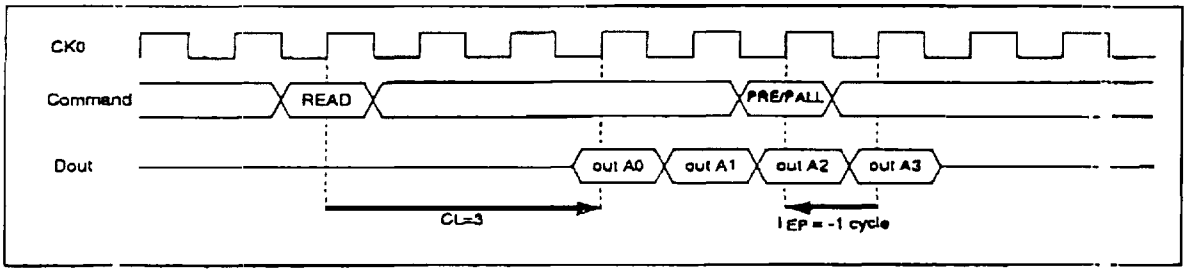
Read command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by I_{HZP}, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the cycles defined by I_{EP} must be assured as an interval from the final data output to precharge command execution.

READ to PRECHARGE Command Interval (same bank): To output all data

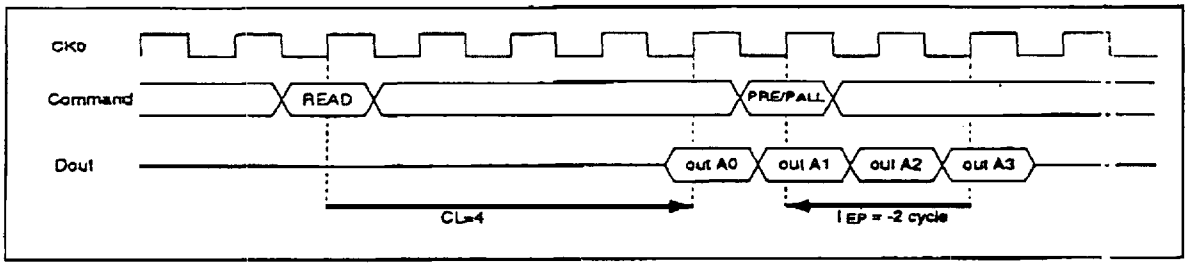
$\overline{CAS}$ Latency = 2, Burst Length = 4



$\overline{CAS}$ Latency = 3, Burst Length = 4

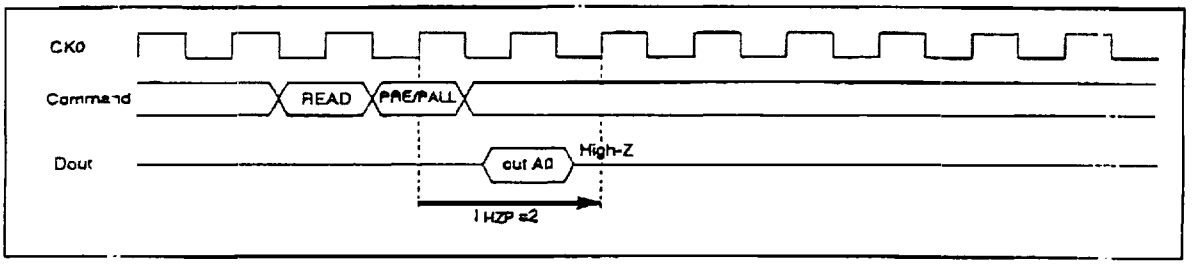


$\overline{CAS}$ Latency = 4, Burst Length = 4

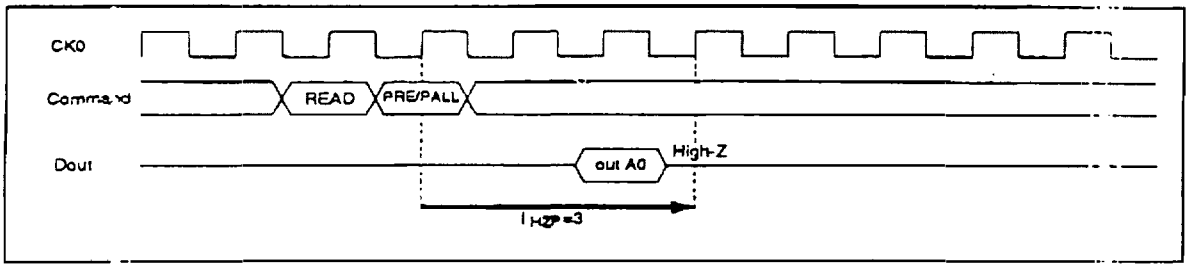


READ to PRECHARGE Command Interval (same bank): To stop output data

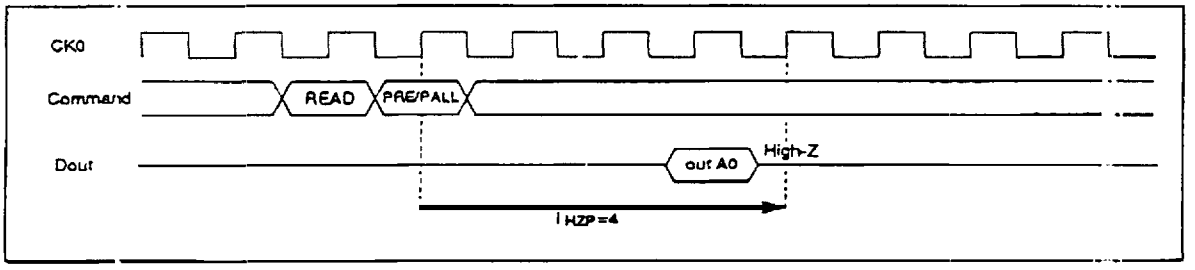
$\overline{CAS}$ Latency = 2, Burst Length = 1, 2, 4, 8



$\overline{CAS}$ Latency = 3, Burst Length = 1, 2, 4, 8



$\overline{AS}$ Latency = 4, Burst Length = 1, 2, 4, 8

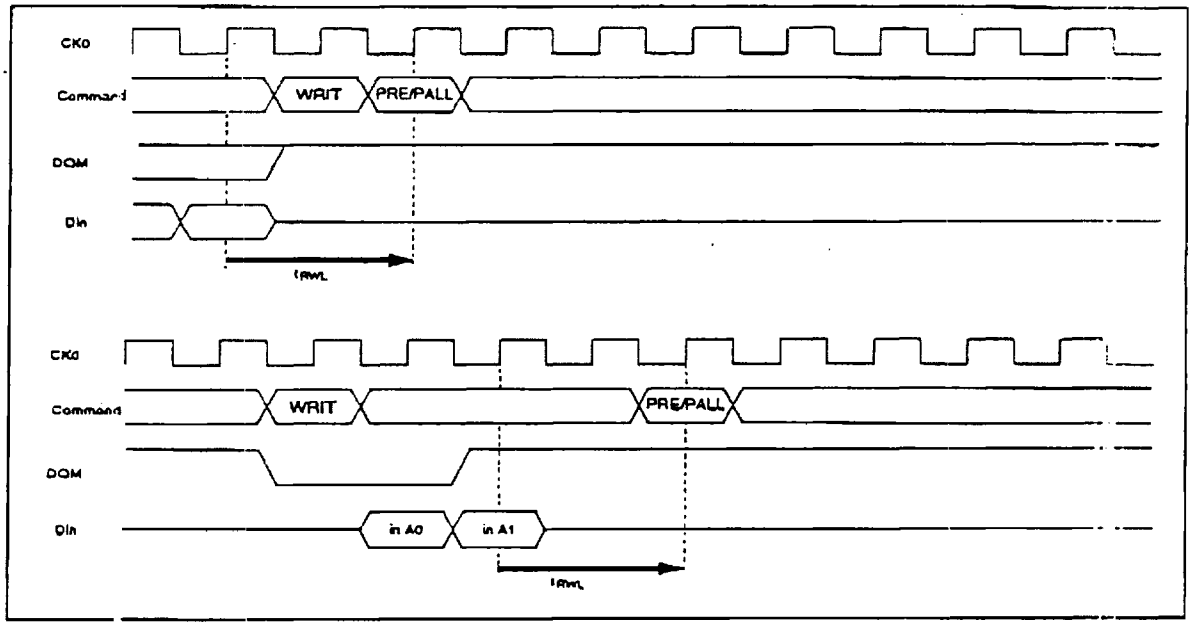


Write command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle.

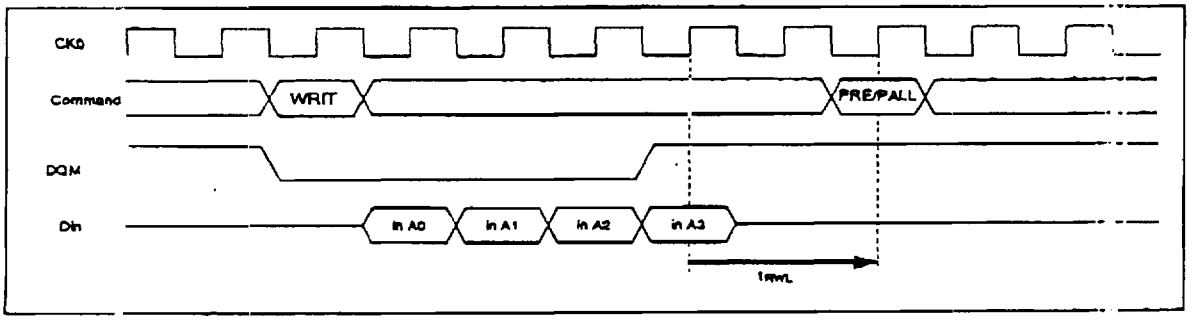
WRITE to PRECHARGE Command Interval (same bank): However, if the burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the cycle defined by t_{RWL}.

WRITE to PRECHARGE Command Interval (same bank)

Burst Length = 4 (To stop write operation)



Burst Length = 4 (To write all data)

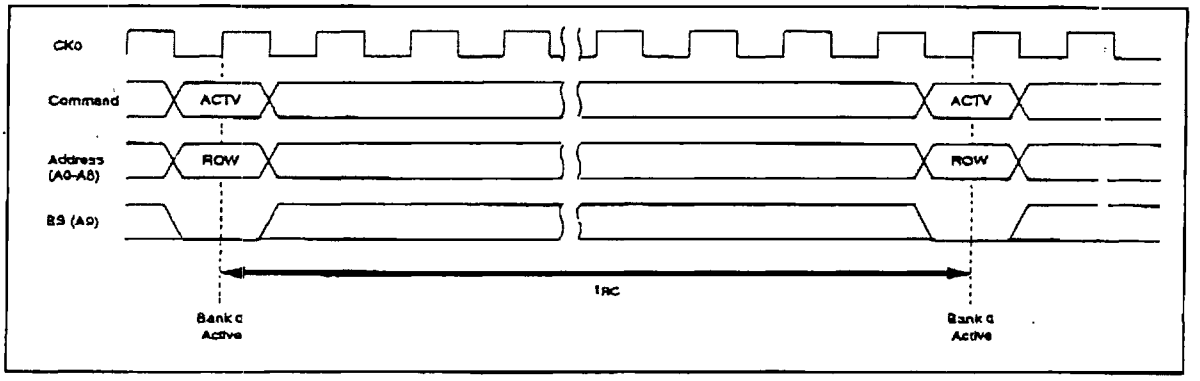


Bank active command interval:

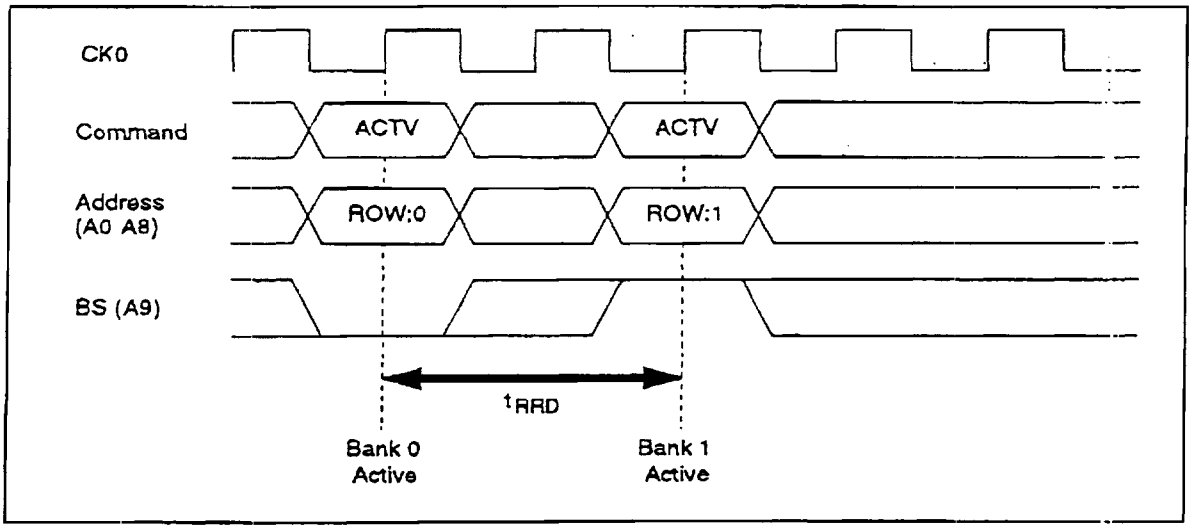
Same bank: The interval between the two bank-active commands must be no less than t_{RC}.

In the case of different bank-active commands: The interval between the two bank-active commands must be no less than t_{RRD}.

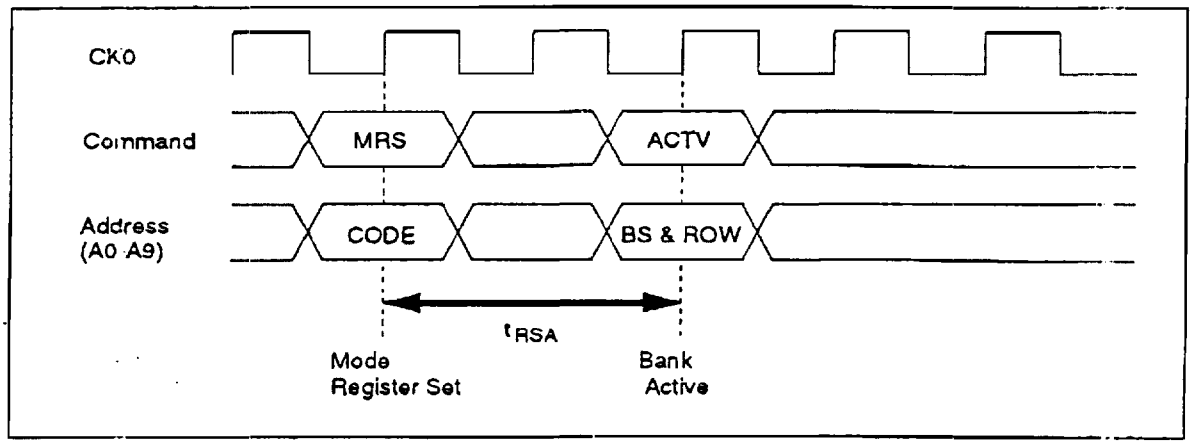
Bank active to bank active for same bank



Bank active to bank active for different bank



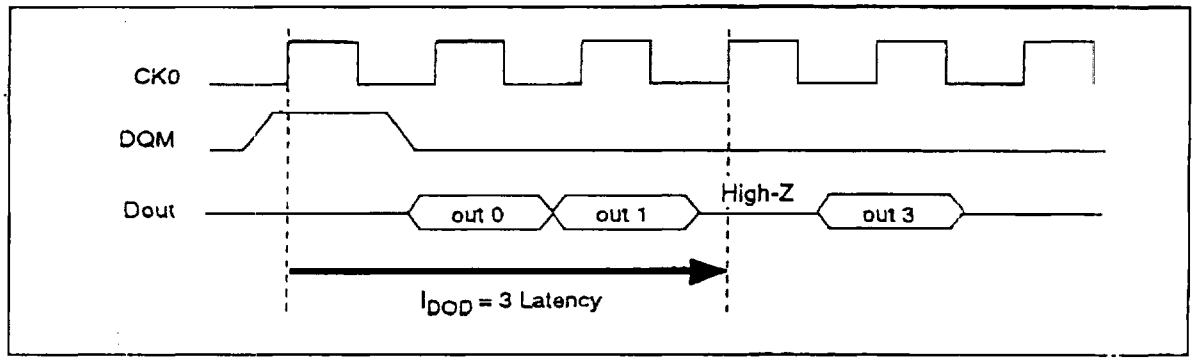
Mode register set to Bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



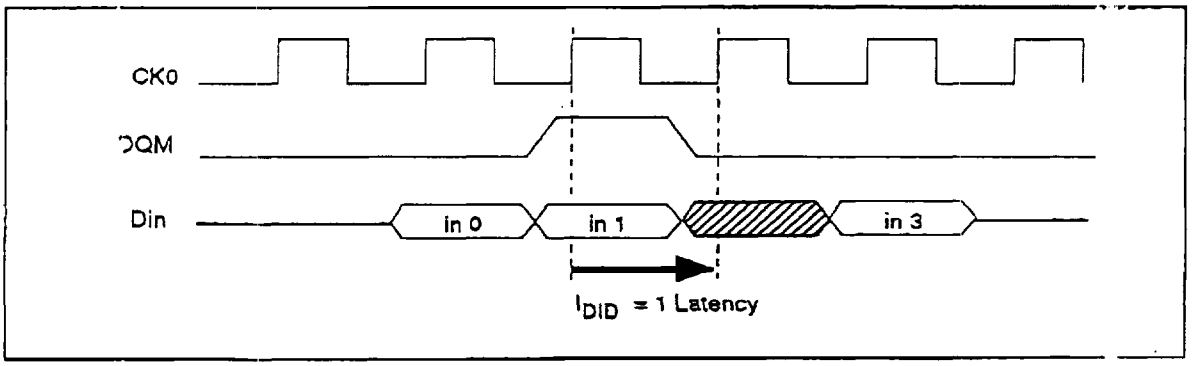
DQM Control

The DQM mask the lower and upper bytes of the DQ data, respectively. The timing of DQM is different during reading and writing.

Reading: When data is read, the output buffer can be controlled by DQM. By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is 3.



Writing: Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is 1.



Refresh

Auto-refresh: All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the interval counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 1024 cycles/16ms. (1024 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh: After executing a self-refresh command, the self-refresh operation continues while CKE0 is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. After the self-refresh, since it is impossible to determine the address of the last ROW to be refreshed, an auto-refresh should immediately be performed for all addresses (1024 cycles).

Others

Power-down mode: The synchronous DRAM module enters power-down mode when CKE0 goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE0 is held Low. In addition, by setting CKE0 to High, the synchronous DRAM module exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

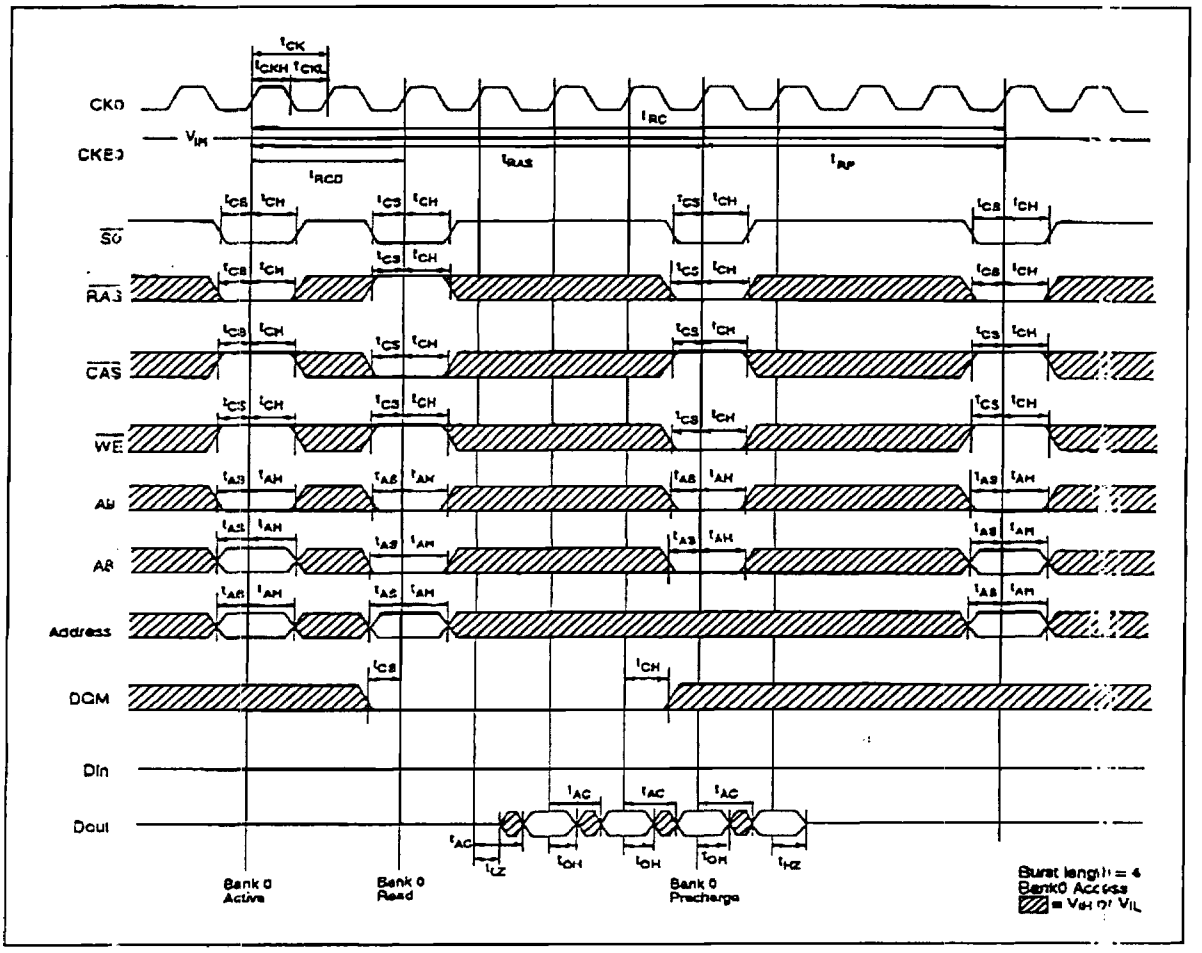
Clock suspend mode: By driving CKE0 to Low during a bank-active or read/write operation, the synchronous DRAM module enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE0 is driven High, the synchronous DRAM module terminates clock suspend mode, and command input is enabled from th enext cycle. For details, refer to the "CKE0 Truth Table".

Power-up sequence: During power-up sequence, the DQM and the CKE0 must be set to High. When 200 µs has past after power on, all banks must be precharged using the precharge command. After t_{RP} delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

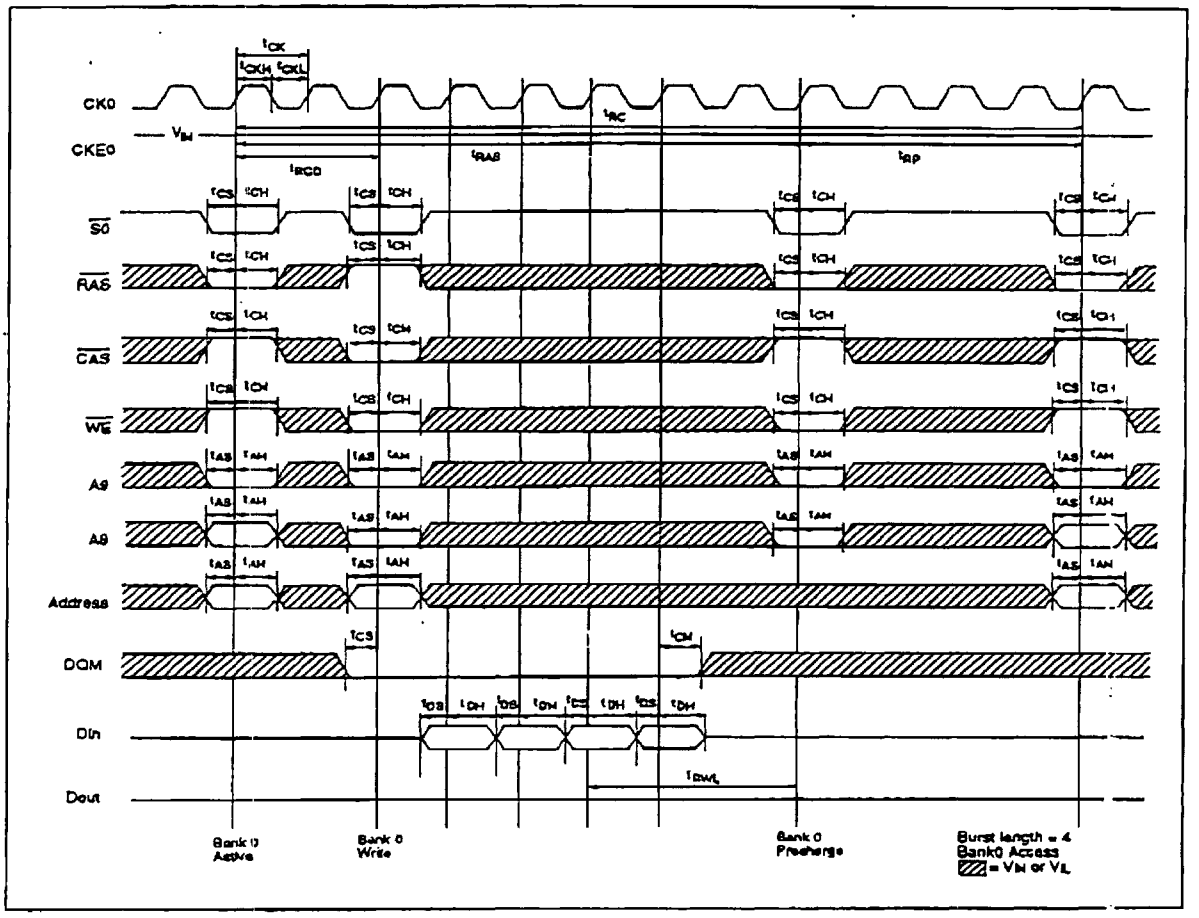
Stabilization time: The PLL requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power on. PLL needs dammy cycle for 50 µs after power on.

Timing Waveforms

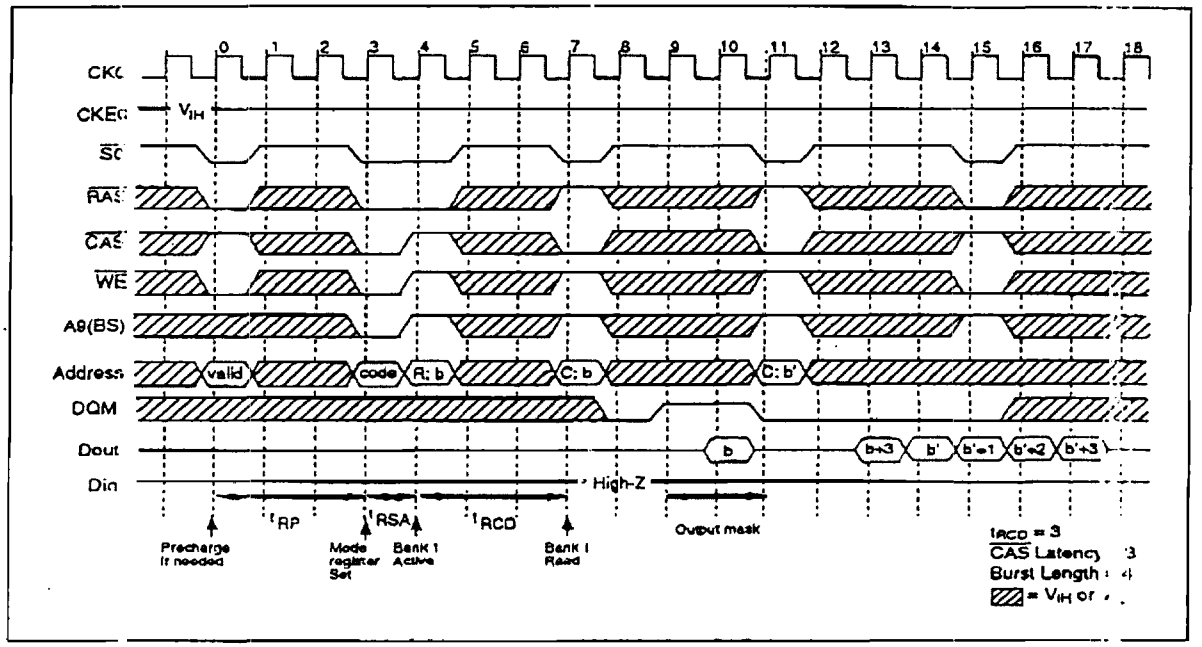
Read Cycle



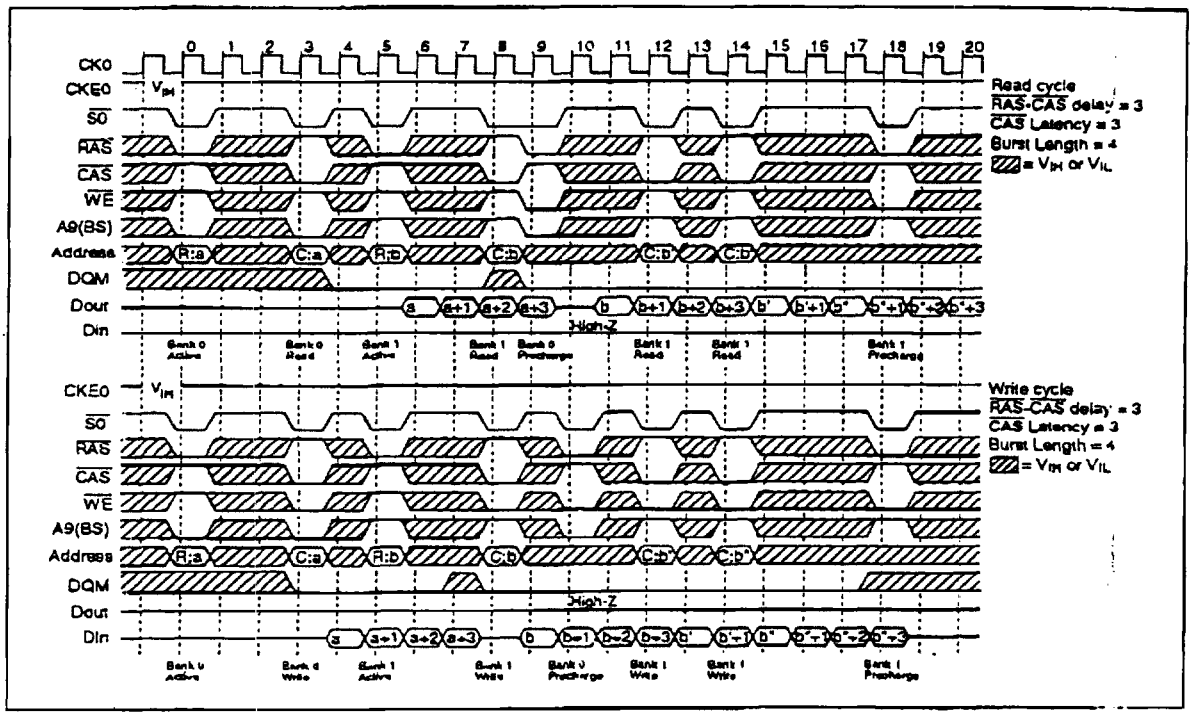
Write Cycle


CK0
CKE0
S0
RAS
CAS
WE
A9
A9
Address
DQM
Din
Dout
Bank 0 Active
Bank 0 Write
Bank 0 Precharge
Burst length = 4
Bank0 Access
= VIH or VIL

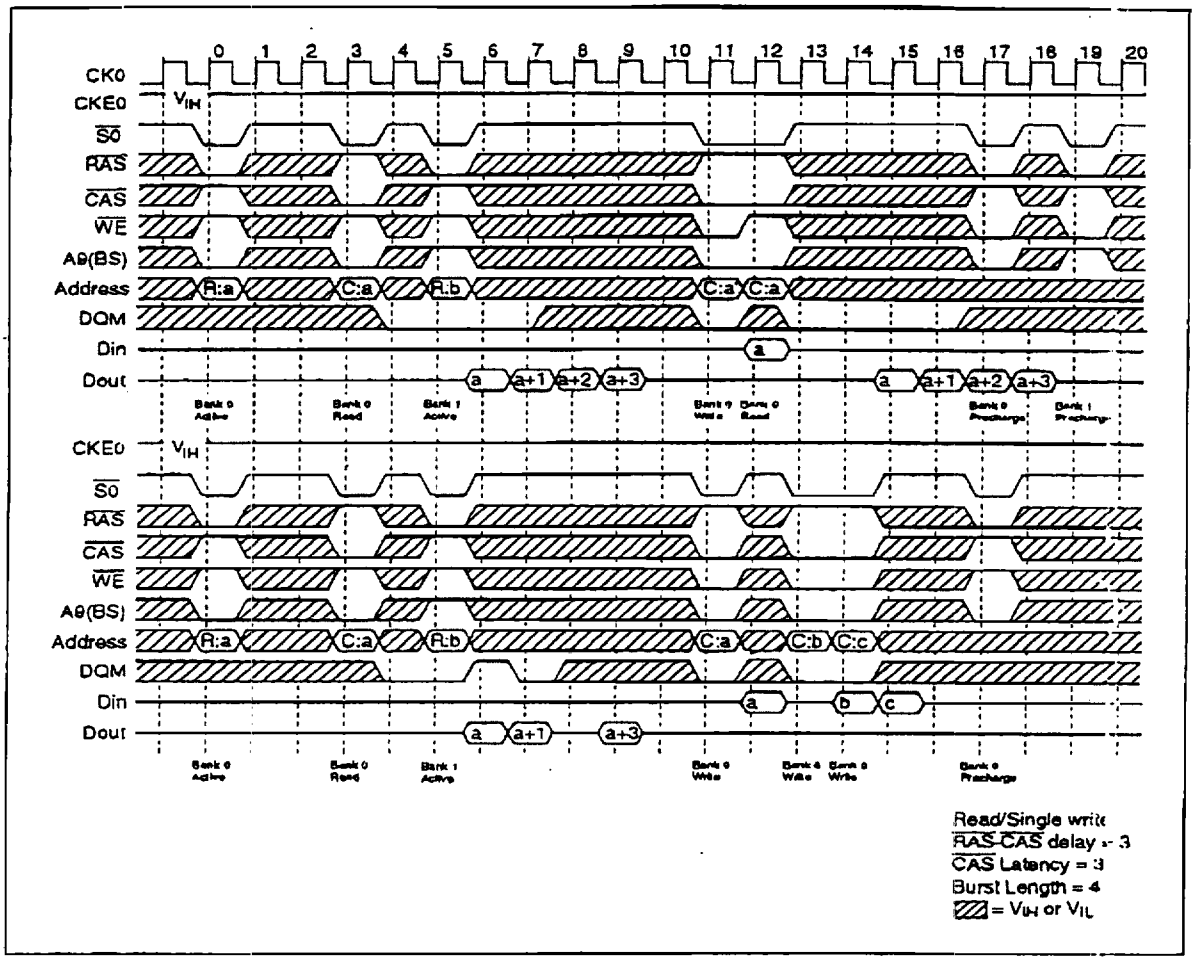
Mode Register Set Cycle



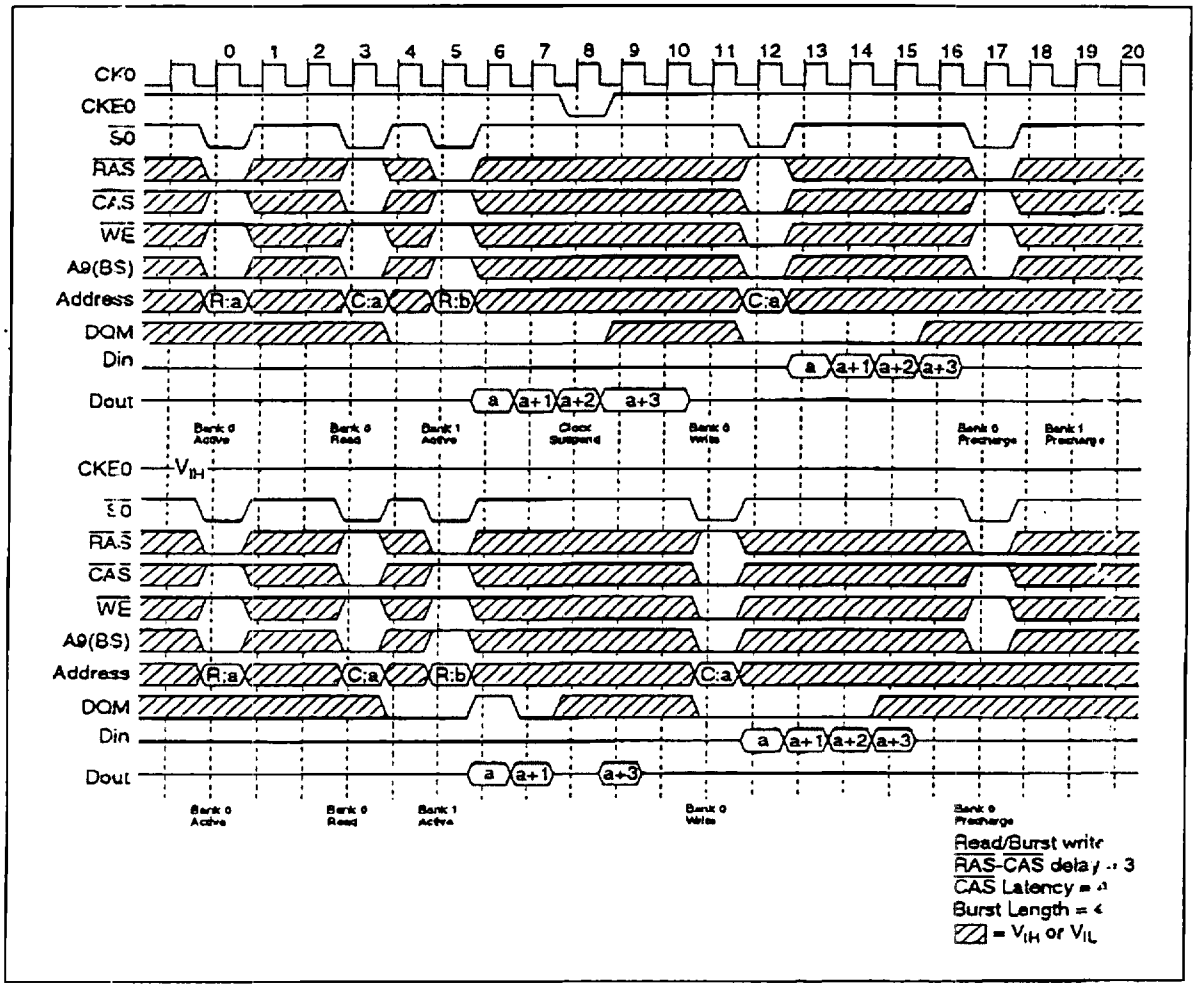
Read Cycle/Write Cycle



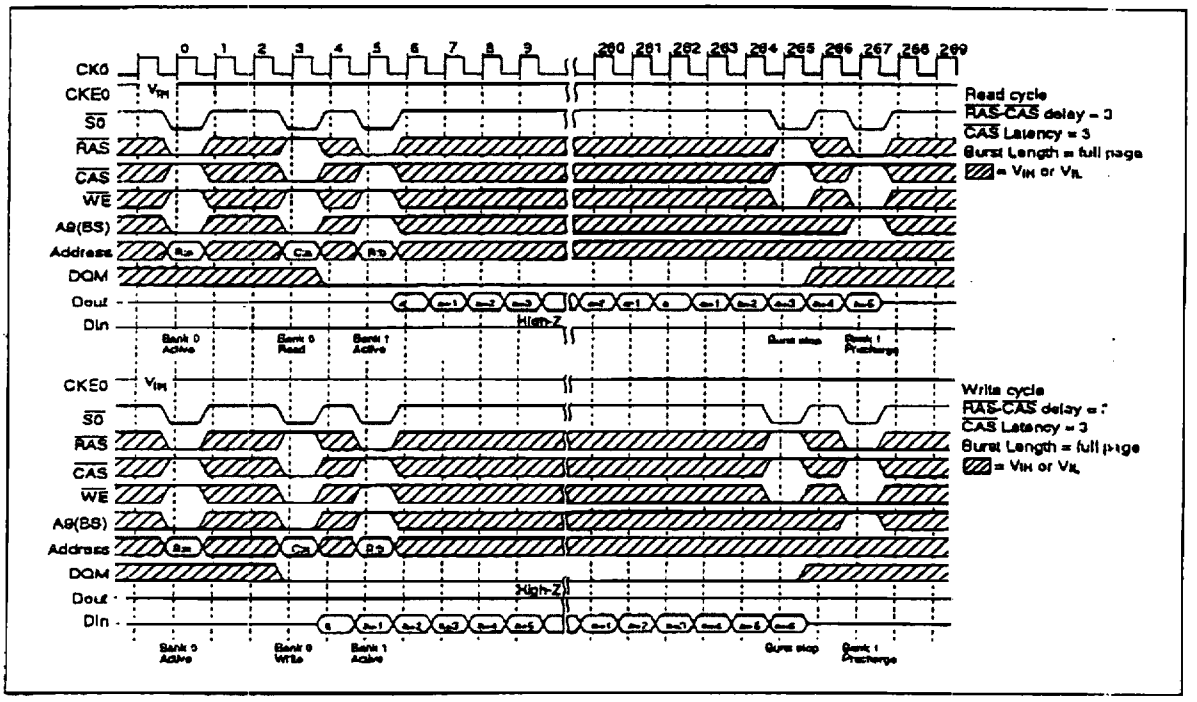
Read/Single Write Cycle



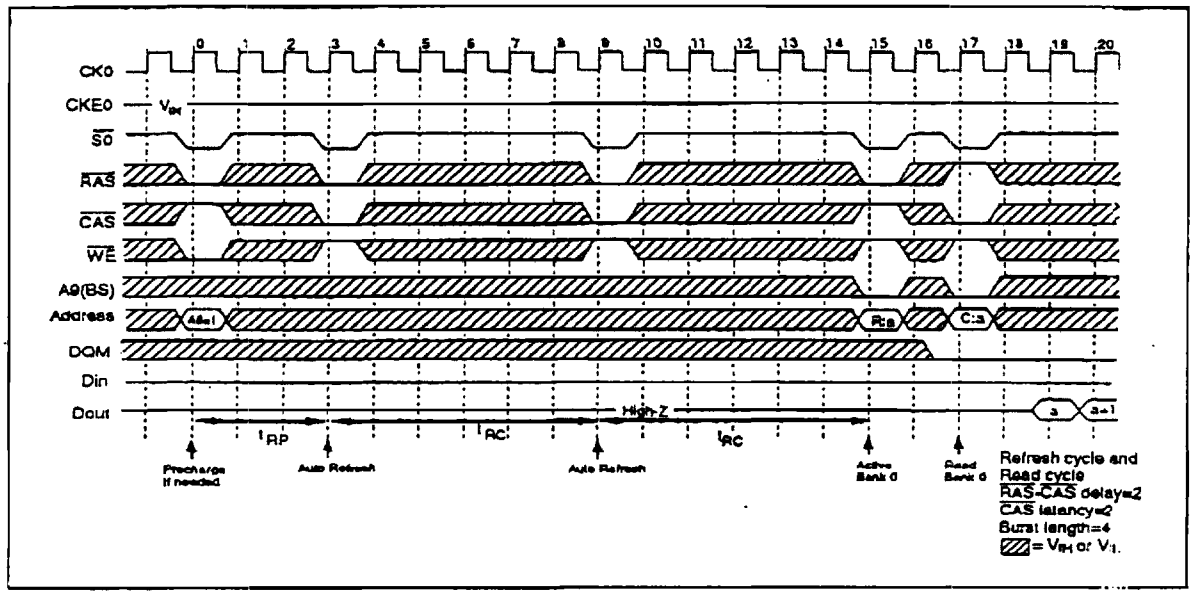
Read/Burst Write Cycle



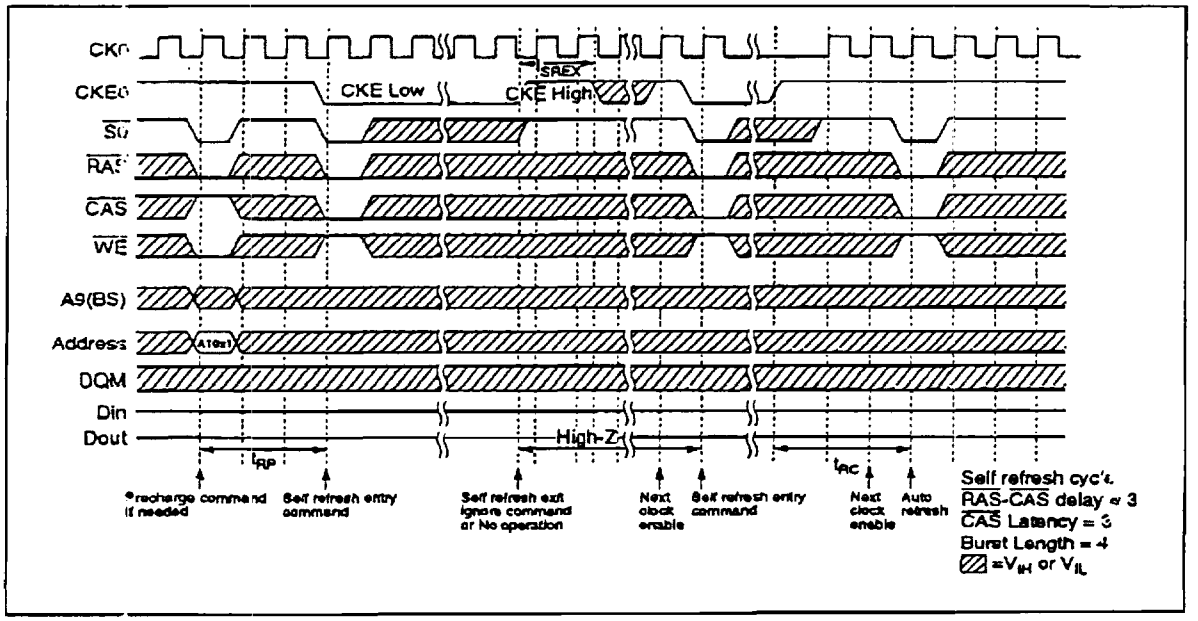
Full Page Read/Write Cycle



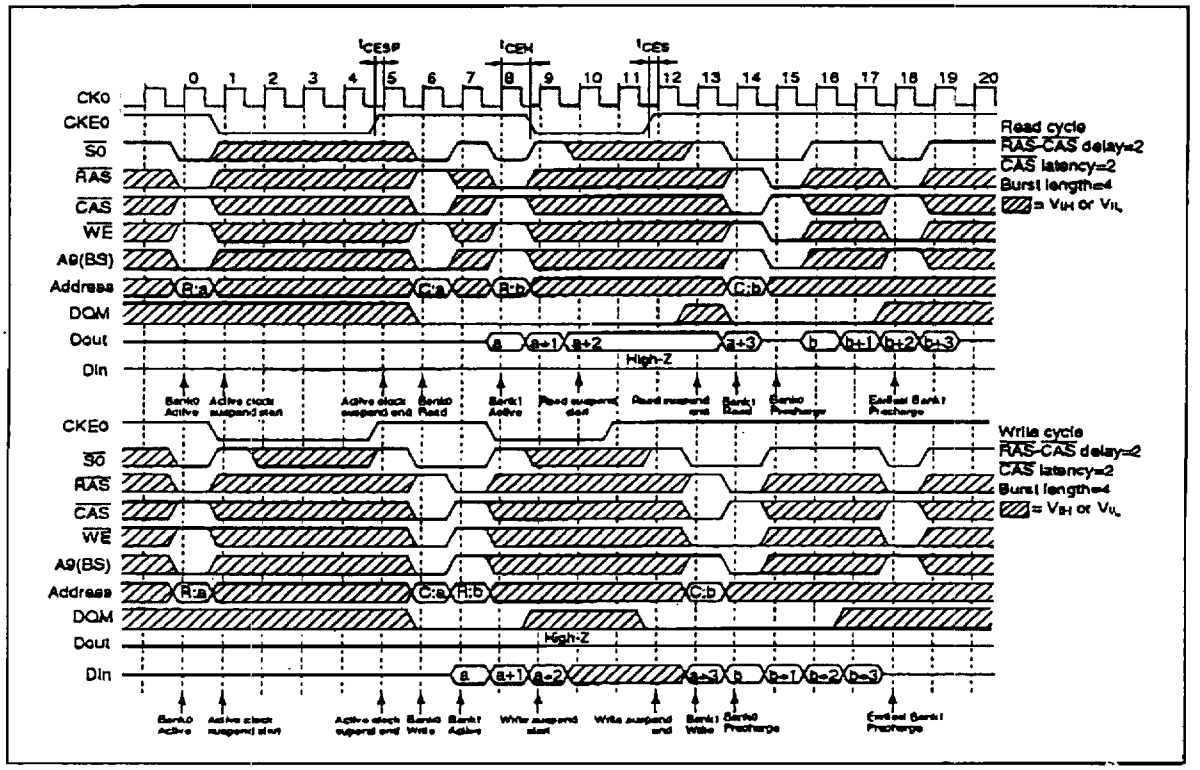
Auto Refresh Cycle



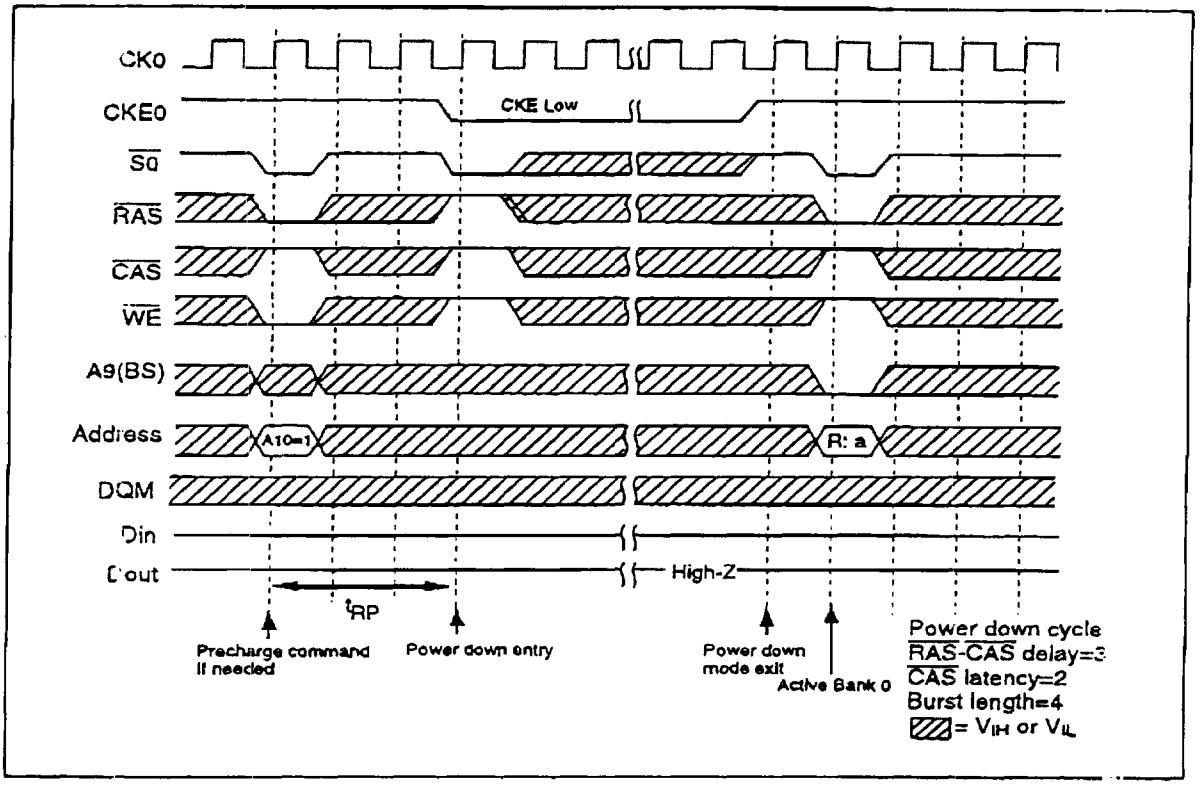
Self Refresh Cycle



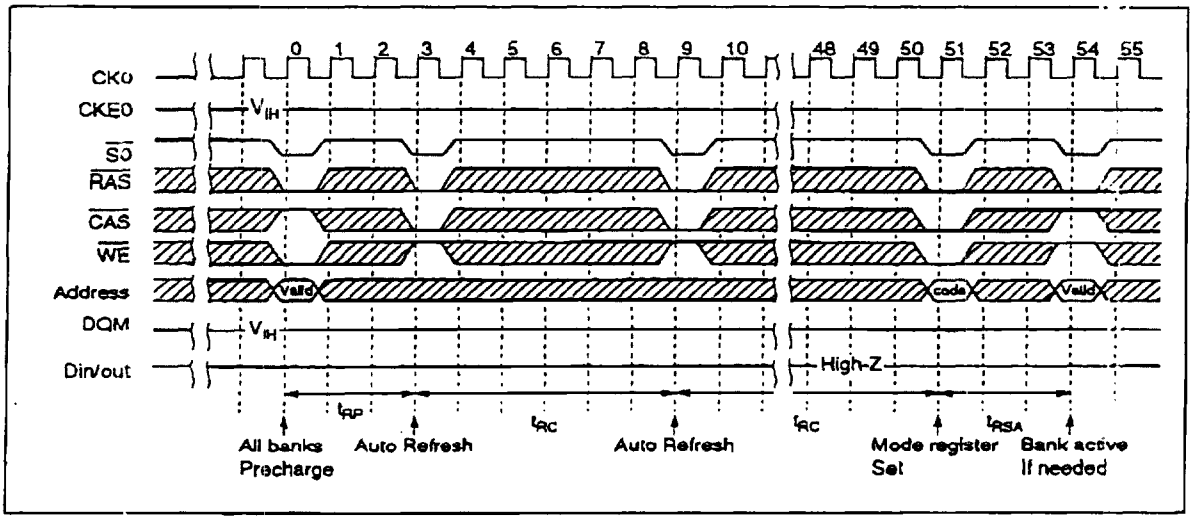
Clock Suspend Mode



Power Down Mode

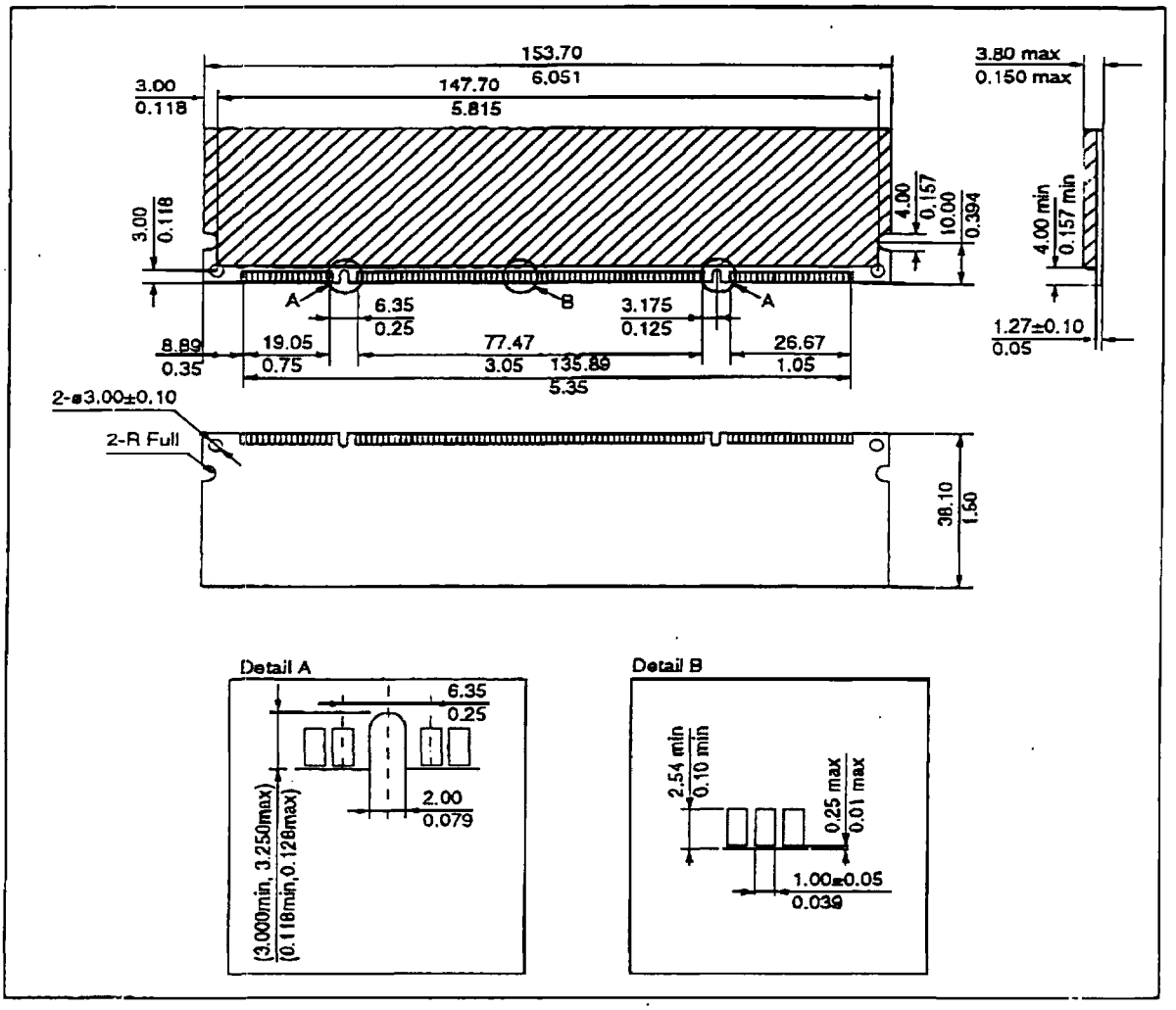


Power Up Sequence



Physical Outline

Unit: mm / inch



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