CMOS Floating-Point Arithmetic Unit and Multiplier

32/34 Bits

The TMC3200, an arithmetic unit, adds and subtracts floating-point numbers expressed in IEEE 32-bit single-precision format or extended-range 34-bit format. Conversions between floating-point and 24-bit two's-complement integer fixed-point representations are provided. Also, an internal accumulate path enhances performance in high-speed systems. The TMC3201, the multiplier compatible with the TMC3200, generates a product of two normalized floating-point numbers. These devices meet the floating-point format and operations described in Version 10.0 of IEEE Standard 754. The TMC3200 and TMC3201 are built using TRW's OMICRON-C™ one-micron CMOS process.

All data and instruction inputs to the TMC3200 and TMC3201 are registered. The input operands of the TMC3200 are selected from the input bus, zero or the accumulate path. Each input operand enters on a half-width bus on two consecutive rising edges of the clock. Controls are provided to determine the operand selection, the arithmetic operation, the data format and the rounding mode. Renormalizing, rounding and limiting functions are provided on both the TMC3200 and TMC3201 to ensure proper handling of special cases and to correct output data formatting. Results are output as two words on successive clock cycles and emerge through a three-state output port.

Features

- IEEE Standard 754 Version 10.0 32-Bit Or Extended-Range 34-Bit Floating-Point Data Format
- IEEE Default Unbiased Round-To-Nearest And Round-Toward-Zero Modes
- Three-Bus Architecture For High Throughput
- Automatic Limiting For Overflow/Underflow Cases
- Selectable Pipelining
- All Inputs And Outputs Are Registered And TTL Compatible
- Low Power CMOS Construction
- Standard/Extended Temperature Range
- Available In An 88 Pin Grid Array Package

TMC3200

- 10 Megaflop Throughput Rate (100ns Pipelined Cycle Time)
- Internal Accumulator Feedback Path
- Integer Two's-Complement 24-Bit Fixed-Point Data Format Conversions
- Full Conversion Between All Data Formats
- Flexible Data Source Selection
- Direct User-Transparent Handling Of Denormalized Operands
- Input Traps For Infinity And Not-A-Number

TMC3201

- 8 Megaflop Throughput Rate (125ns Pipelined Cycle Time)
- Input Traps For Infinity, Zero, Not-A-Number And Denormalized Numbers

Applications

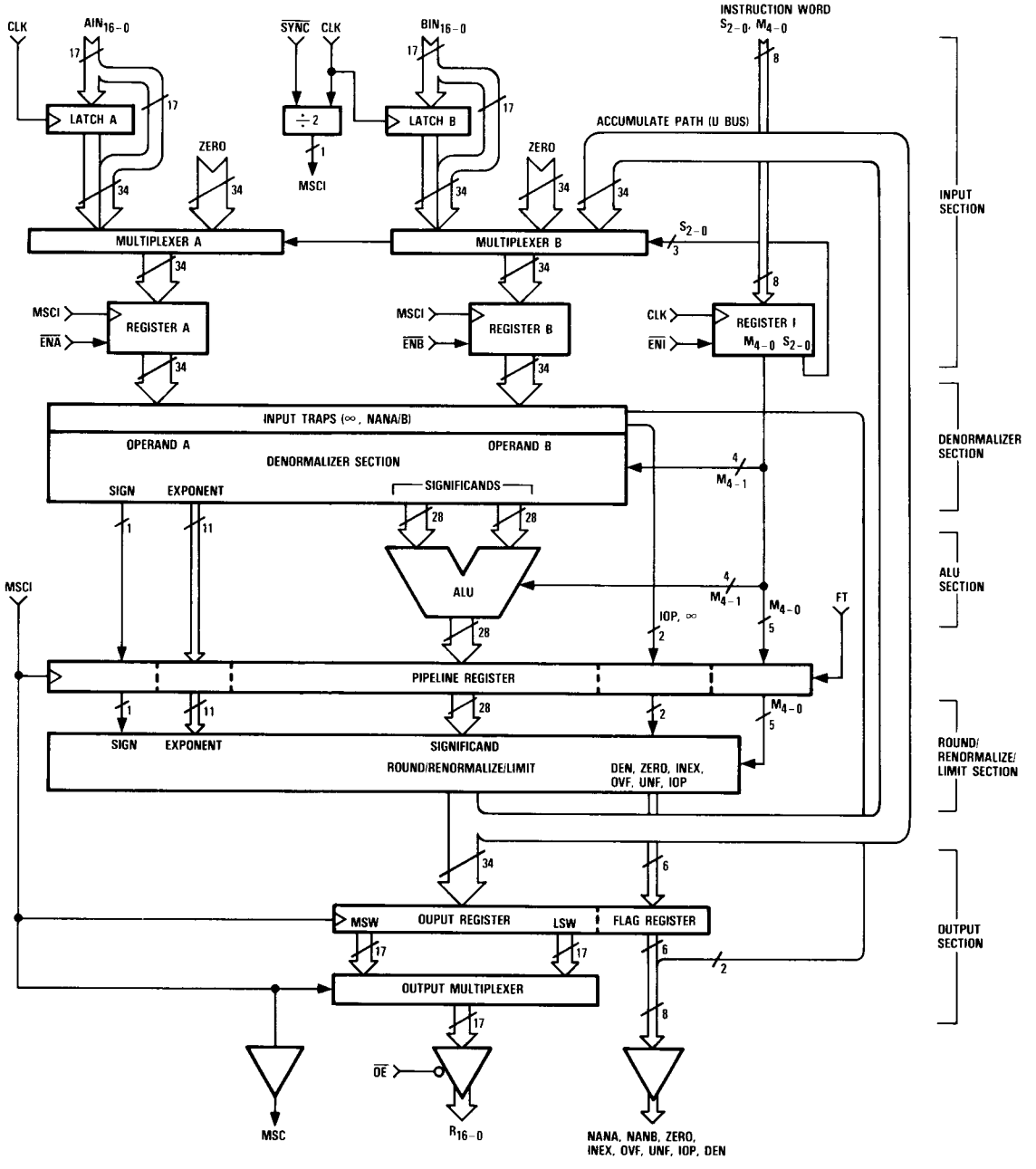
- Matrix Operations And Geometric Transforms
- Arithmetic Element In Microprogrammed Array Processors
- Graphics And Image Processors
- Floating-Point Digital Filters
- Fast Fourier Transforms
- Radar And Sonar Signal Processors
- Solids Modeling

TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

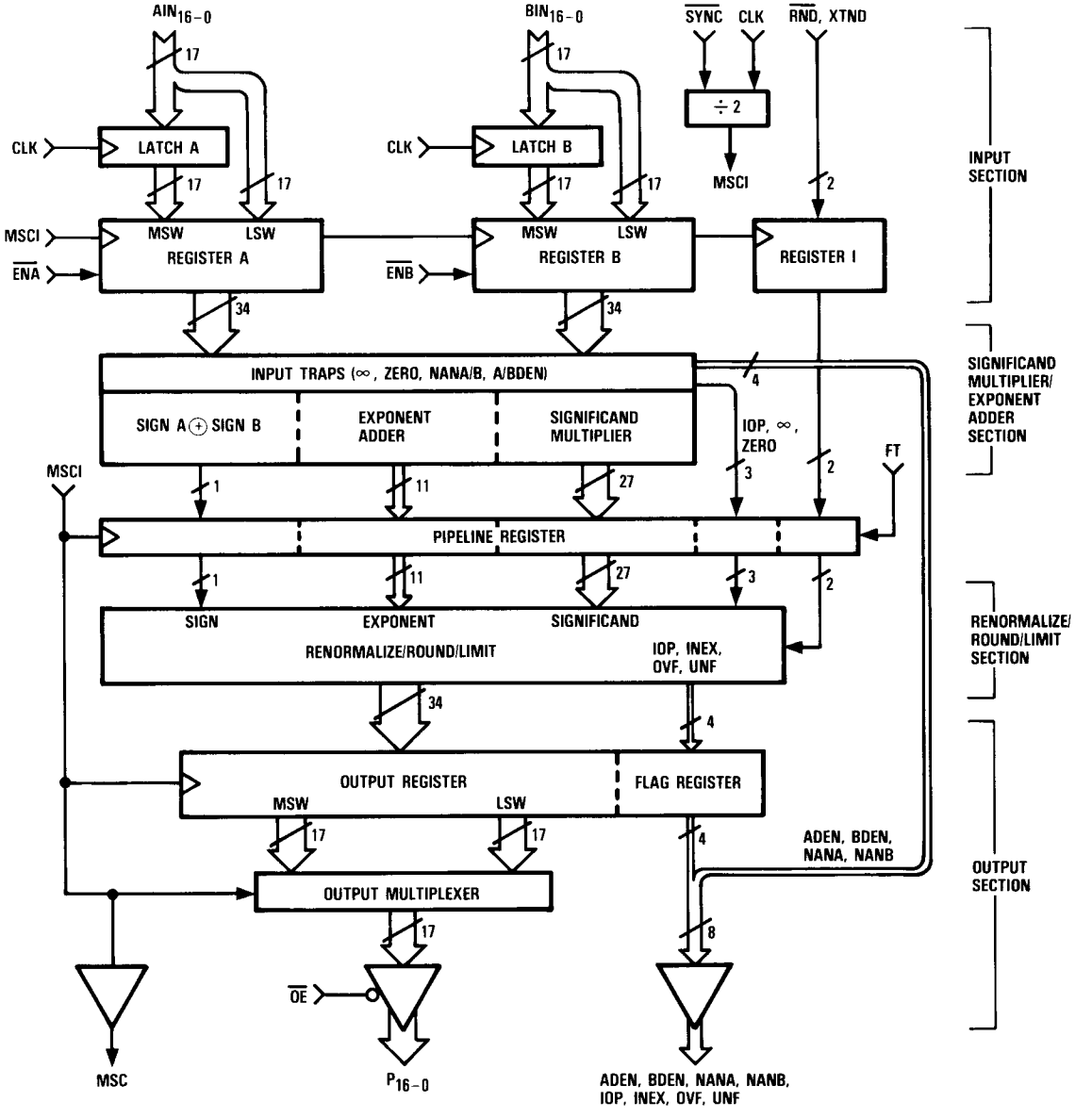
Phone: (619) 457-1000
FAX: (619) 455-6314

40G03660 Rev. C – 11/90
Printed in the U.S.A.

TMC3200 Functional Block Diagram



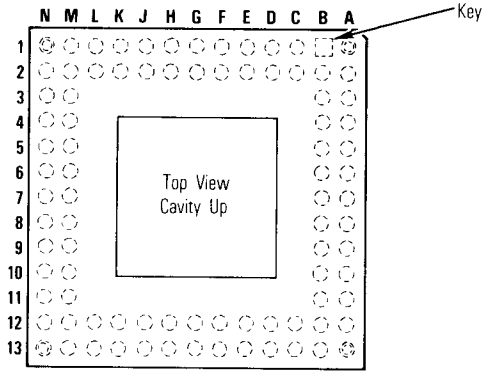
TMC3201 Functional Block Diagram



TMC3200 Pin Assignments

88 Pin Grid Array – G5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B1	AIN_8	N2	V_{DD}	M13	NC	A12	BIN_9
C2	AIN_9	M3	DEN	L12	V_{DD}	B11	BIN_{10}
C1	AIN_{10}	N3	NANA	L13	V_{DD}	A11	BIN_{11}
D2	AIN_{11}	M4	NANB	K12	R_6	B10	BIN_{12}
D1	AIN_{12}	N4	MSC	K13	R_5	A10	BIN_{13}
E2	AIN_{13}	M5	IOP	J12	R_4	B9	BIN_{14}
E1	AIN_{14}	N5	OVF	J13	R_3	A9	BIN_{15}
F2	AIN_{15}	M6	UNF	H12	R_2	B8	BIN_{16}
F1	AIN_{16}	N6	INEX	H13	R_1	A8	$\overline{ENB}$
G1	FT	N7	ZERO	G13	R_0	A7	$\overline{SYNC}$
G2	GND	M7	GND	G12	V_{DD}	B7	V_{DD}
H1	V_{DD}	N8	V_{DD}	F13	GND	A6	GND
H2	S_2	M8	R_{16}	F12	$\overline{OE}$	B6	CLK
J1	S_1	N9	R_{15}	E13	BIN_0	A5	$\overline{ENA}$
J2	S_0	M9	R_{14}	E12	BIN_1	B5	AIN_0
K1	M_2	N10	R_{13}	D13	BIN_2	A4	AIN_1
K2	M_0	M10	R_{12}	D12	BIN_3	B4	AIN_2
L1	M_1	N11	R_{11}	C13	BIN_4	A3	AIN_3
L2	M_4	M11	R_{10}	C12	BIN_5	B3	AIN_4
M1	M_3	N12	R_9	B13	BIN_6	A2	AIN_5
N1	$\overline{ENI}$	N13	R_8	A13	BIN_7	A1	AIN_6
M2	GND	M12	R_7	B12	BIN_8	B2	AIN_7



TMC3200 Functional Description

The TMC3200 consists of five sections: the input multiplexers and registers, the denormalizer, the arithmetic logic unit (ALU) and pipeline register, the round/renormalize/limit block, and the output registers and drivers.

TMC3201 Pin Assignments

88 Pin Grid Array – G5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B1	AIN_8	N2	V_{DD}	M13	NC	A12	BIN_9
C2	AIN_9	M3	GND	L12	V_{DD}	B11	BIN_{10}
C1	AIN_{10}	N3	NANA	L13	V_{DD}	A11	BIN_{11}
D2	AIN_{11}	M4	NANB	K12	P_6	B10	BIN_{12}
D1	AIN_{12}	N4	MSC	K13	P_5	A10	BIN_{13}
E2	AIN_{13}	M5	IOP	J12	P_4	B9	BIN_{14}
E1	AIN_{14}	N5	OVF	J13	P_3	A9	BIN_{15}
F2	AIN_{15}	M6	UNF	H12	P_2	B8	BIN_{16}
F1	AIN_{16}	N6	INEX	H13	P_1	A8	$\overline{ENB}$
G1	FT	N7	V_{DD}	G13	P_0	A7	$\overline{SYNC}$
G2	GND	M7	GND	G12	V_{DD}	B7	V_{DD}
H1	V_{DD}	N8	NC	F13	GND	A6	GND
H2	GND	M8	P_{16}	F12	$\overline{OE}$	B6	CLK
J1	GND	N9	P_{15}	E13	BIN_0	A5	$\overline{ENA}$
J2	V_{DD}	M9	P_{14}	E12	BIN_1	B5	AIN_0
K1	XTND	N10	P_{13}	D13	BIN_2	A4	AIN_1
K2	$\overline{RND}$	M10	P_{12}	D12	BIN_3	B4	AIN_2
L1	GND	N11	P_{11}	C13	BIN_4	A3	AIN_3
L2	V_{DD}	M11	P_{10}	C12	BIN_5	B3	AIN_4
M1	ADEN	N12	P_9	B13	BIN_6	A2	AIN_5
N1	BDEN	N13	P_8	A13	BIN_7	A1	AIN_6
M2	NC	M12	P_7	B12	BIN_8	B2	AIN_7

Input Multiplexers And Registers

The input section accepts the AIN and BIN operands along with the 8-bit instruction word which determines the A and B source multiplexer action, the arithmetic section operation, the rounding mode and data format of the operands. The clock (CLK) is divided by two generating the Most Significant Word Clock (MSCI) which is used internally for I/O multiplexing and is also available as an output, the MSC flag.

The AIN and BIN operands each enter on their respective 17-bit half-width input buses. Input preload registers latch in the data on the input buses on the rising edge of CLK. When the enable controls ($\overline{ENA}$ and $\overline{ENB}$) for the operand registers are LOW and AIN and BIN are selected by MUX A and MUX B, the data present in the preload registers and the data present on the input bus are simultaneously loaded into the operand registers on the rising edge of internal MSCI. The Most Significant Word (MSW) must be present on the rising edge of CLK which generates the falling edge of MSCI, and the Least Significant Word (LSW) must be present on the rising edge of CLK which generates the rising edge of MSCI. The

synchronization control ($\overline{SYNC}$) allows the user to align the MSCI signal with the desired phase of CLK. Initially, $\overline{SYNC}$ must be LOW to align the falling edge of MSCI with the rising edge of CLK and HIGH to align the rising edge of MSCI with CLK. After initial synchronization, alignment of CLK and MSCI will remain set as long as $\overline{SYNC}$ is held HIGH. The pipeline register contents are loaded into the operand register B on the rising edge of MSCI when $\overline{ENB}$ is LOW and the feedback accumulate path is selected.

The 8-bit instruction is loaded into the instruction register on the rising edge of CLK and must be input at the same time as the MSW of the operands with which it is associated. The instruction word must be held through both load cycles (MSW and LSW input) of the data to which it applies. The instruction word is divided into four fields: one to control the operand source multiplexers (S_{2-0}), one to select the data format (M_{2-1}), one to control the arithmetic operation performed (M_{4-3}) and one to control the rounding method (M_0). Operand A can be selected from two possible sources: AIN or zero. The B operand can be selected from three possible sources: BIN, the accumulate path or zero. The input and output data formats may differ and be selected from 32-bit floating-point, 34-bit floating-point or 24-bit integer fixed-point formats. The arithmetic operation performed is selected from A + B, A - B, B - A, -A - B, and CONVB (Convert B to a different data format). The rounding method is either IEEE round-to-nearest (which gives an unbiased error over a sequence of operations) or IEEE round-toward-zero, also known as truncation.

The input traps test AIN and BIN for the special cases of infinity and Not-A-Number (NAN). Internal flags which identify these cases are generated. If NAN is found, the NANA or NANB flag is set immediately and the output will be NAN with the Invalid Operation (IOP) flag. Infinity minus infinity produces a NAN output and sets the IOP flag.

Table 1. Multiplexer A And Multiplexer B Control

S_{2-0}	A Operand	B Operand
000	AIN	BIN
001	AIN	U
010	0	BIN
011	AIN	0
100	Magnitude (AIN)	Magnitude (BIN)
101	Magnitude (AIN)	Magnitude (U)
110	0	Magnitude (BIN)
111	Magnitude (AIN)	0

Note: 1. The Magnitude function turns off the sign bit and applies to floating-point operands only.

Denormalizer

This section prepares the operands by denormalizing (right-shifting) the smaller exponent's significand. This section outputs the larger incoming exponent, the sign and the input trap status flags.

Arithmetic Block

The ALU adds or subtracts the two significands which were output from the denormalizer section. The ALU output, exponent, sign and IOP flag are transferred to the pipeline register on the rising edge of internal MSCI if the Feedthrough (FT) control is LOW. When FT is HIGH, the pipeline register is transparent.

Round/Renormalize/Limit Block

The TMC3200 supports the IEEE default "unbiased round-to-nearest" when M_0 (round) is LOW. When M_0 is HIGH, the device implements "round-toward-zero" which truncates the result. The rounding adder operates on the output generated from the arithmetic section and outputs the result to the renormalizer.

The renormalizer shifts the rounded significand as necessary and adjusts the exponent. The resulting exponent is examined for overflow or underflow of the output data format. The renormalizer is disabled when converting from floating-point to integer and when converting from 34-bit to 32-bit IEEE denormalized "gradual underflow" format.

The limiter replaces overflowing results with a signed infinity (full-scale positive or negative integer in fixed mode). If the output is not in the "gradual underflow" mode, underflowing numbers are replaced with zero. A NAN output is triggered whenever an illegal operation (infinity minus infinity or NAN plus any number) is executed. In all other cases, the limiter will pass the result unchanged. The output from the round/renormalize/limit section is connected to the output register and also may be the input to register B through the accumulate path (U bus), a 34-bit feedback path.

Output Register And Drivers

The output section contains a 34-bit output result register, a 6-bit output flag register, the output multiplexer and the output drivers.

The output registers are clocked by internal MSCI. The contents of the registers are the 34-bit output from the limit section and the output flags. NANA and NANB are set when their particular input operand is NAN and will remain set until

a new legal operand is loaded. The arithmetic section results that are flushed to NANs set the IOP flag but not the NAN flags. The remaining flags become valid with their corresponding results and remain as long as the associated result is in the output register. The flag outputs are always enabled independent of the Output Enable ($\overline{OE}$) control.

The output multiplexer passes either the MSW or LSW of the result to the output drivers. The output multiplexer selects the MSW when MSC is HIGH and the LSW when MSC is LOW. The output drivers are enabled when $\overline{OE}$ is LOW and in the high-impedance state when $\overline{OE}$ is HIGH.

Table 2. Instruction Decoding

Instruction Select M_{4-3}	Mode, Round Select M_{2-0}							
	000	001	010	011	100	101	110	111
00	A+B $F_2 \cdot F_2$ Round	A+B $F_2 \cdot F_2$ Trunc	A+B $F_4 \cdot F_2$ Round	A+B $F_4 \cdot F_2$ Trunc	A+B $F_4 \cdot F_4$ Round	A+B $F_4 \cdot F_4$ Trunc	A+B $F_2 \cdot F_4$ Round	A+B $F_2 \cdot F_4$ Trunc
01	A-B $F_2 \cdot F_2$ Round	A-B $F_2 \cdot F_2$ Trunc	CONVB $F_2 \cdot F_4$ x	CONVB $F_2 \cdot F_4$ x	A-B $F_4 \cdot F_4$ Round	A-B $F_4 \cdot F_4$ Trunc	CONVB $F_4 \rightarrow F_2$ Round	CONVB $F_4 \rightarrow F_2$ Trunc
10	B-A $F_2 \cdot F_2$ Round	B-A $F_2 \cdot F_2$ Trunc	CONVB $I \cdot F_2$ x	CONVB $I \cdot F_2$ x	B-A $F_4 \rightarrow F_4$ Round	B-A $F_4 \cdot F_4$ Trunc	CONVB $I \cdot F_4$ x	CONVB $I \rightarrow F_4$ x
11	-A-B $F_2 \cdot F_2$ Round	-A-B $F_2 \cdot F_2$ Trunc	CONVB $F_2 \cdot I$ Trunc	CONVB $F_2 \cdot I$ Trunc	-A-B $F_4 \rightarrow F_4$ Round	-A-B $F_4 \cdot F_4$ Trunc	CONVB $F_4 \rightarrow I$ Trunc	CONVB $F_4 \cdot I$ Trunc

Notes:

1. M_0 = Round
   M_1 = Convert
   M_2 = 34-bit
   M_3 = Negate B
   M_4 = Negate A
2. For floating-point to fixed-point conversions round-toward-zero is implemented.
3. F_2 and F_4 are 32-bit and 34-bit floating-point formats respectively.
4. I = Integers (fixed-point).
5. x = Don't care.
6. Round = Round-to-nearest
7. Trunc = Round-toward-zero.
8. For all CONVB (convert B) instructions, the A-operand field is ignored.

TMC3201 Functional Description

The TMC3201 consists of four sections: the input registers, the significand multiplier/exponent adder and pipeline register, the renormalize/round/limit block, and the output registers and drivers.

Input Section

The input section accepts the AIN and BIN operands along with a 2-bit instruction word which determines the data format of the operands and the rounding mode. CLK is divided by two generating MSCI which is used internally for I/O multiplexing and is also available as an output, the MSC flag.

The AIN and BIN operands each enter on their respective 17-bit half-width input buses. Input preload registers latch in the data on the input buses on the rising edge of CLK. When the enable controls ($\overline{ENA}$ and $\overline{ENB}$) for the operand registers are LOW, the data present in the preload registers and the data present on the input bus are simultaneously loaded into the operand registers on the rising edge of internal MSCI. The MSW must be present on the rising edge of CLK which generates the falling edge of MSCI, and the LSW must be present on the rising edge of CLK which generates the rising edge of MSCI. $\overline{SYNC}$ allows the user to align the MSCI signal with the desired phase of CLK. Initially, $\overline{SYNC}$ must be LOW to align the falling edge of MSCI with the rising edge of CLK and HIGH to align the rising edge of MSCI with CLK. After initial synchronization, alignment of CLK and MSCI will remain set as long as $\overline{SYNC}$ is held HIGH.

The 2-bit instruction is loaded into the instruction register on the rising edge of CLK and must be input at the same time as the MSW of the operands with which it is associated. The instruction word must be held through both load cycles (MSW and LSW input) of the data to which it applies. The Extended-Range control (XTND) selects the data format and Round ($\overline{RND}$) controls whether round-to-nearest or IEEE round-toward-zero is used.

The input traps test AIN and BIN for the special cases of infinity, zero, NAN and denormalized numbers. If NAN is found, the NANA or NANB flag is set immediately and the product output will be the product NAN with the IOP flag. Multiplication of zero times infinity also produces a NAN output and sets the IOP flag. The TMC3201 is not able to process denormalized operands and will set the appropriate ADEN or BDEN flag. The product output in this case will be zero corresponding to the "fast" implementation of IEEE Standard 754.

Significand Multiplier/Exponent Adder

Floating-point multiplication consists of multiplying the fraction fields and adding the exponent fields. Since the TMC3201 operates only on normalized numbers, the 23 bits of each input fraction field are input to the multiplier array with the implicit "hidden bit" (which is always a one) added. This output is latched by the pipeline register which follows the multiplier array.

The A and B exponent fields are added generating a two's-complement product exponent. The result is passed through the pipeline registers and the exponent adjust section performs further processing before final output.

The significand product, the exponent sum, the instructions, the IOP flag and the product sign are latched into the pipeline register on the rising edge of internal MSCI if FT is LOW.

Renormalize/Round/Limit Section

The significand is renormalized and passed to the rounding adder. If $\overline{RND}$ is LOW, the TMC3201 will round-to-nearest according to the IEEE default standard. If $\overline{RND}$ is HIGH, the significand is truncated (IEEE round-toward-zero).

The product exponent is checked for overflow or values greater than or equal to 255 for IEEE 32-bit format or 511 for extended-range 34-bit format. Underflow has occurred if the exponent is less than or equal to zero in 32-bit format or -512 in extended-range 34-bit format.

The limiter forces the significand and exponent fields to appropriate signed infinities, zero or NAN. Overflow cases are forced to signed infinities, underflow and zero cases are forced to a signed zero, and illegal operation cases are forced to NAN. Also, the two status flags Overflow (OVF) and Underflow (UNF) are generated for output in this section. The output of this section is a 34-bit field, interpreted as either IEEE 32-bit or extended-range 34-bit data.

Output Register And Drivers

The output section contains a 34-bit output product register, a 4-bit output flag register, the output multiplexer and the output drivers.

The output registers are clocked by internal MSCI. The contents of the registers are the 34-bit output from the limit section along with the output flags. The flags are valid while the result is held in the output register except for the NANA, NANB, ADEN and BDEN flags. These operand trap flags are set when their particular input operand is a NAN or a denormalized number and will remain set until a new legal operand is loaded. The flags are always enabled independent of the $\overline{OE}$ control.

The output multiplexer passes either the MSW or LSW to the output drivers. The output multiplexer selects the MSW when MSC is HIGH and the LSW when MSC is LOW. The output drivers are enabled when $\overline{OE}$ is LOW and in the high-impedance state when $\overline{OE}$ is HIGH.

J

Signal Definitions

Power

V_{DD}, GND — The TMC3200 and TMC3201 operate from a single +5 Volt supply. All power and ground lines must be connected.

Data Inputs

AIN_{16-0}, BIN_{16-0} — AIN and BIN are the 17-bit input ports. AIN_{16} and BIN_{16} are the extension bits for 34-bit floating-point operation.

Data Outputs

R_{16-0} — R_{16-0} is the 17-bit result output port of the TMC3200. R_{16} is the extension bit for 34-bit floating-point operation.

P_{16-0} — P_{16-0} is the 17-bit product output port of the TMC3201. P_{16} is the extension bit for 34-bit floating-point operation.

Clock

CLK — The CLK frequency is twice the data throughput rate to allow for data multiplexing. All operations are with respect to the rising edge of CLK. CLK is internally divided by two to generate internal MSCI. The rising edge of MSCI is coincident with every other rising edge of CLK.

Controls

$\overline{ENA}$, $\overline{ENB}$ — Enable A (Enable B) enables register A (B) when LOW. Register A (B) is then loaded with the output of Multiplexer A (Multiplexer B) on the rising edge of internal MSCI.

$\overline{SYNC}$ — $\overline{SYNC}$ causes the falling edge of MSCI to be coincident with the rising edge of CLK when LOW for t_S before the rising edge of CLK. This signal must go HIGH for the device to operate properly. Bringing $\overline{SYNC}$ LOW with the incoming MSW and then HIGH during the LSW will initialize the device.

$\overline{OE}$ — Output Enable controls the three-state outputs. When $\overline{OE}$ is LOW, the output drivers are enabled. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state. $\overline{OE}$ does not affect the flag outputs and must be held LOW for two CLK cycles to obtain a complete output result.

FT — Feedthrough controls the pipeline register. When FT is LOW, the pipeline register is enabled. When FT is HIGH, the pipeline register is transparent. FT is a DC control.

$\overline{ENI}$ — Enable Instruction enables register I when LOW for t_S before the rising edge of CLK. Register I is then loaded with an instruction M_{4-0} and S_{2-0}. If $\overline{ENI}$ is held LOW, the instruction words must be valid for two cycles of CLK for a valid operation. (TMC3200)

S_{2-0} — Source decoding selects the A and B operands of the TMC3200 by controlling Multiplexer A and Multiplexer B.

M_{4-0} — These controls (instruction, mode, round select) define the various ways the TMC3200 operates. When M_0 is LOW, the result will round-to-nearest (round). When M_0 is HIGH, the result will round-toward-zero (truncate). M_2 selects 32 or 34-bit formats. When M_1 is LOW, M_4 and M_3 control the A and B operands.

XTND — Extended-range 34-bit data format is in effect when XTND is HIGH. This control signal is loaded on every rising edge of CLK. (TMC3201)

$\overline{RND}$ — When Round is LOW, the result will round-to-nearest. When HIGH, the result will round-toward-zero or truncate. This control signal is loaded on every rising edge of CLK. (TMC3201)

Flags

MSC — Most Significant Word Clock output synchronizes the data output. When the output is enabled and MSC is HIGH, the MSW result is present at the output. When the output is enabled and MSC is LOW, the LSW result is present at the output.

OVF — Overflow will go HIGH when a floating-point result exponent exceeds the maximum allowed or when a full-scale integer result is available at the output.

UNF — Underflow will go HIGH when a nonzero result is too small to be a normalized floating-point number and is available at the output.

INEX — Inexact Result will go HIGH when a result fractional part is not exactly equal to the results of an infinitely precise calculation and the result is available at the output.

NANA, NANB — Not-A-Number A and B flags will go HIGH when the A and B operand registers contain non-valid IEEE Standard 754 numbers.

IOP — Invalid Operation flag will go HIGH when an operation is requested which cannot be properly executed for any reason.

ZERO — All operations which result in zero cause this flag to go HIGH when the result is available at the output. (TMC3200)

DEN — Denormalize will go HIGH when any result with zero exponent and nonzero fraction is available at the output. (TMC3200)

ADEN, BDEN — A and B Operand Denormalized will go HIGH when the contents of the respective operand register is not a normalized IEEE Standard 754 number. (TMC3201)

No Connects

NC — The pin grid array version of the TMC3200 has one pin which is not connected internally. The pin grid array version of the TMC3201 has three pins which are not connected internally.

TMC3200 Package Interconnections

Signal Type	Signal Name	Function	G5 Package
Power	V_{DD}	Supply Voltage	H1, N2, N8, L12, L13, G12, B7
	GND	Ground	G2, M2, M7, F13, A6
Data Input	AIN_{16-0}	A Input Data	F1, F2, E1, E2, D1, D2, C1, C2, B1, B2, A1, A2, B3, A3, B4, A4, B2
	BIN_{16-0}	B Input Data	B8, A9, B9, A10, B10, A11, B11, A12, B12 A13, B13, C12, C13, D12, D13, E12, E13
Data Output	R_{16-0}	Result Output Data	M8, N9, M9, N10, M10, N11, M11, N12, N13 M12, K12, K13, J12, J13, H12, H13, G13
Clock	CLK	Clock	B6
Controls	$\overline{ENA}$	Enable A Register	A5
	$\overline{ENB}$	Enable B Register	A8
	$\overline{ENI}$	Enable I Register	N1
	$\overline{SYNC}$	Synchronize ALU	A7
	S_{2-0}	Operand Source	H2, J1, J2
	M_{4-3}	Instruction Select	L2, M1
	M_{2-1}	Mode Select	K1, L1
	M_0	Round	K2
	$\overline{OE}$	Output Enable	F12
	FT	Feedthrough	G1
Flags	MSC	MSW Clock	N4
	ZERO	Zero Result	N7
	DEN	Denormalized Result	M3
	OVF	Overflow	N5
	UNF	Underflow	M6
	INEX	Inexact Result	N6
	NANA	Not-A-Number A	N3
	NANB	Not-A-Number B	M4
	IOP	Invalid Operation	M5
No Connection	NC	None	M13

TMC3201 Package Interconnections

Signal Type	Signal Name	Function	G5 Package
Power	V_{DD}	Supply Voltage	H1, J2, L2, N2, N7, L12, L13, G12, B7
	GND	Ground	G2, H2, J1, L1, M3, M7, F13, A6
Data Input	AIN_{16-0}	A Input Data	F1, F2, E1, E2, D1, D2, C1, C2, B1, B2, A1, A2, B3, A3, B4, A4, B5
	BIN_{16-0}	B Input Data	B8, A9, B9, A10, B10, A11, B11, A12, B12, A13, B13, C12, C13, D12, D13, E12, E13
Data Output	P_{16-0}	Product Output Data	M8, N9, M9, N10, M10, N11, M11, N12, N13 M12, K12, K13, J12, J13, H12, H13, G13
Clock	CLK	Clock	B6
Controls	$\overline{ENA}$	Enable A Register	A5
	$\overline{ENB}$	Enable B Register	A8
	$\overline{SYNC}$	Synchronization	A7
	XTND	Extended Precision	K1
	$\overline{RND}$	Round	K2
	$\overline{OE}$	Output Enable	F12
	FT	Feedthrough	G1
Flags	MSC	MSW Clock	N4
	ADEN	A Denormalized	M1
	BDEN	B Denormalized	N1
	OVF	Overflow	N5
	UNF	Underflow	M6
	INEX	Inexact	N6
	NANA	Not-A-Number A	N3
	NANB	Not-A-Number B	M4
	IOP	Invalid Operation	M5
No Connection	NC	None	M2, N8, M13

Data Format

The TMC3200 arithmetic unit and TMC3201 multiplier conform to IEEE Standard 754, Version 10.0 data format for 32-bit arithmetic. These devices also have an extended-range 34-bit floating-point format. The two additional bits of the extended format are appended to the exponent field. Any two legal 32-bit operands can be added without generating an overflow if the 34-bit extended format is used for output. The ALU accumulate path uses the 34-bit extended format. For both data formats the arithmetic unit needs only two clock cycles to transfer a data word since the input and output buses are 17-bit wide.

Standard IEEE 32-Bit Floating-Point Format

The IEEE Standard 754, Version 10.0 specifies a 32-bit data format for floating-point arithmetic. In this format the MSB (bit 31) is the sign bit, the next eight bits (bits 30-23) are the exponent field, and the 23 LSBs are the fractional significand field (bits 22-0). The "hidden bit" completes the 24-bit significand.

Sign Bit

The MSB carries the sign information. A HIGH for a sign bit indicates a negative number and a LOW indicates a positive number.

Exponent Field

The 8-bit exponent field determines whether the floating-point number is a signed infinity, a NAN, a zero, a denormalized number or a normalized floating-point number.

The exponent values 0 and 255 are special. If the exponent field is all ones (1111 1111, 255_{10}) and the fraction (bits 22–0) is zero, the number is evaluated as infinity x $(-1)^S$ with S being the sign bit. Any exponent of 255 with a nonzero fraction is a NAN. NANs are generally used to communicate error information and have no numerical value.

When the exponent field is all zeros (0000 0000) and the fraction is also zero, the number is a true floating-point zero. Note that this data format allows both positive and negative zeros which are computationally treated identically. When the exponent is zero and the fraction is nonzero, the number is a denormalized floating-point number evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-126} \times (0.F)$$

where S is the sign bit, E is the value of the exponent field (base 10), and F is the value of the fractional field.

If the exponent field is neither all zeros nor all ones, the floating-point number is normalized and evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-127} \times (1.F)$$

Note that the exponent bias has changed from 126 to 127 and that 1.0 has been added to the fractional field. The exponent can assume values which run from −126 to +127 (0 to 254 biased by 127). Note that both exponent fields of zero and one map onto the exponent value of −126. These provisions ensure a smooth transition from normalized numbers through gradual underflow into the denormalized numbers.

Fractional Field

Bits 22–0 comprise the fractional field (mantissa). There is a binary point assumed between bit 22 and the implied "hidden" bit 23. For a nonzero exponent, the hidden bit assumes a value of "1." For a zero exponent, the hidden bit has a value of "0." Bit 22 carries a binary weighting of 2^{-1}. The following bits carry decreasing binary weights down to the LSB (bit 0) which carries the weight of 2^{-23}. This is identical to treating the fractional part (bits 22–0) like an integer F multiplied by 2^{-23}. The fractional part of the floating-point number is either 0 + F (in the case of a zero exponent), or 1 + F (in the case of a nonzero exponent).

The difference between the smallest normalized number (exponent = 1, fractional part = 0) and the largest denormalized number (exponent = 0, fractional part= all ones) is one LSB. The smallest normalized number is: exponent = −126, significand = 1.00...00. The largest denormalized number is: exponent = −126, significand = 0.11...11.

Extended 34-Bit Floating-Point Format

The 34-bit extended-data format is a superset of the IEEE 32-bit floating-point format because every number represented in the IEEE 32-bit format can be represented in the 34-bit format. The MSB (bit 33) is the sign bit; the next ten bits (bits 32–23) are the exponent field; and the 23 LSBs are the fractional field.

Sign Bit

The sign bit (bit 33) signifies the sign of the floating-point number. If the sign bit is HIGH, the number is negative. If the sign bit is LOW, the number is positive.

Exponent Field

As in the 32-bit format, the extreme exponents are special. The exponent field is interpreted as a 10-bit two's-complement integer which can vary from 10 0000 0000 (-512_{10}) to 01 1111 1111 (511_{10}). If the fraction is zero with an exponent of 511, the floating-point number is a signed infinity. A nonzero fraction with an exponent of 511 means that the number is a NAN.

If the exponent is −512, a fraction of zero signifies a true floating-point zero. As in the 32-bit format, there are both positive and negative zeros. A nonzero fraction with a −512 exponent signifies a denormalized number.

If the exponent is any value other than −512 or 511, the exponent value is the 10-bit two's-complement number minus a bias of 127 and the number is evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-127} \times (1.F)$$

where S is the sign bit, E is the exponent and F is the fraction to which the hidden bit of 1 is added. Note that the exponents can be in the range of −638 (−511−127) to 383 (510−127).

Two's-Complement 24-Bit Integer Format

The TMC3200 converts data between the floating-point formats and a 24-bit two's-complement integer format which is sign-extended to 32 bits.

Sign Bit

In the integer format, the bit occupying the position of the exponent LSB (E_0) is the two's-complement MSB/sign bit whose weighting is -2^{23}. When an integer is output, the sign extends this bit through the normal 32-bit floating-point sign and exponent fields. The nine MSBs will be all ones for negative numbers and zeros for positive numbers.

Fraction Field

The 23-bit floating-point fraction field becomes the magnitude portion of the two's-complement integer. The weighting is shifted giving the LSB a weighting of one. The numerical interpretation of an integer is:

$$I = E_0 \times (-2^{23}) + \sum_{n=0}^{22} F_n \times (2^n)$$

where F_n is the 23 fraction bits and E_0 is the exponent LSB. For integer input, the device ignores the 8 MSBs (floating-point sign and seven highest exponent bits) plus the 34-bit extension bit.

Application Discussion (TMC3200)

Comparisons

One function required of arithmetic systems is the comparison of two quantities. The device can perform this function by subtracting one IEEE or extended-range number from another (the rounding mode is not important for this function). The ZERO flag and sign output will reflect the results of the comparison of the operands. Normalized and denormalized numbers and infinities can be compared. The results will be correct in all meaningful cases: two normalized or denormalized numbers in any combination, a normalized or denormalized number and +/-infinity, and even +infinity compared to -infinity. The IOP flag will be HIGH when there is no mathematically meaningful order to the inputs. Note that magnitudes (absolute values) can be compared by using the magnitude function of the source select segment of the instruction.

Table 3. Flags For Comparison Results (Operation A – B)

Operand A	Operand B	Order	IOP	ZERO	Sign
Norm/Denorm	Norm/Denorm	A > B	0	0	0
Norm/Denorm	Norm/Denorm	A = B	0	1	X
Norm/Denorm	Norm/Denorm	A < B	0	0	1
+∞	Norm/Denorm		0	0	0
Norm/Denorm	+∞		0	0	1
+∞	-∞		0	0	0
-∞	+∞		0	0	1
+∞	+∞		1	0	X
-∞	-∞		1	0	X

Table 4. Flag Interpretation

IOP	ZERO	Sign	Interpretation
0	0	0	A > B
0	0	1	A < B
0	1	X	A = B
1	X	X	no mathematical order to inputs, e.g. comparison of two negative infinities.

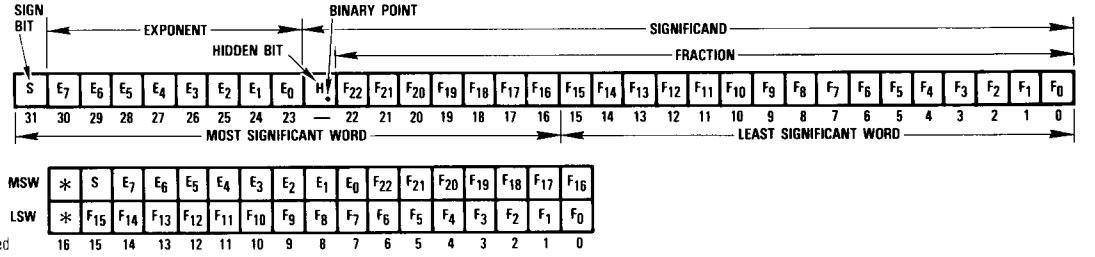
Reduced Microcode

The control signals are encoded to lower the device pin count. Because this encoding is relatively light, applications that do not require the full functionality of the TMC3200 can permanently connect many of the control signals resulting in a reduced microcode set.

The IEEE default round-to-nearest mode can be permanently selected by connecting M_0 to a logic LOW. If the 34-bit extended-range mode is not used for inputs or outputs (which would be the situation in IEEE standard systems), M_2 can be permanently connected to a logic LOW. Note that internal accumulation is always extended range. If a 32-bit output format is selected by the operation and mode controls, the flags and outputs are proper for the IEEE standard, but internally accumulated results are more accurate than those obtained by reducing the sum to 32 bits. This treatment can eliminate overflow or underflow errors in long accumulations. If magnitude operations are not required, then S_2 can be permanently connected to a logic LOW.

These suggestions enable the designer to reduce the number of instruction bits with little loss in functionality.

Figure 1. IEEE 32-Bit Format



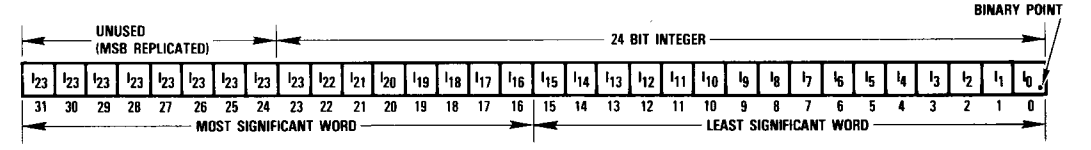
MSW	*	S	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0	F_{22}	F_{21}	F_{20}	F_{19}	F_{18}	F_{17}	F_{16}
LSW	*	F_{15}	F_{14}	F_{13}	F_{12}	F_{11}	F_{10}	F_9	F_8	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
*Not Used	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Exponent	Fraction	Value	Name
255	Not all zeros	--	Not-A-Number
255	All zeros	$(-1)^S \times \infty$	Signed Infinity
1 through 254	Any	$(-1)^S \times (1.F) \times 2^{E-127}$	Normalized Number
0	Not all zeros	$(-1)^S \times (0.F) \times 2^{E-126}$	Denormalized Number
0	All zeros	$(-1)^S \times 0.0$	Zero

Notes:

1. If an illegal operation generates a NAN, then $F = 200000_H$ in the TMC3200 and $F = 400000_H$ in the TMC3201.
2. H, the hidden bit, is one except for zero and denormalized numbers when it is zero.
3. E and F are magnitude representations.

Figure 2. 24-Bit Integer Format



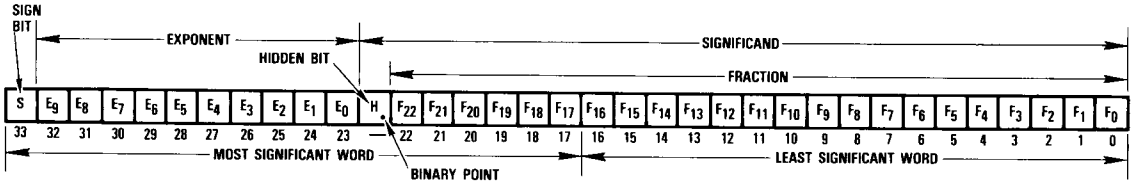
MSW	*	I_{23}	I_{23}	I_{23}	I_{23}	I_{23}	I_{23}	I_{23}	I_{23}	I_{23}	I_{22}	I_{21}	I_{20}	I_{19}	I_{18}	I_{17}	I_{16}
LSW	*	I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
*Not Used	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

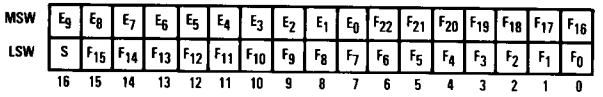
Notes:

1. $I = -2^{23} I_{23} + \sum_{i=0}^{22} 2^i I_i$
2. For fixed-point inputs, the sign bit is bit 23, and bits 31-24 are don't care.
3. For fixed-point outputs, the sign bit is replicated through bits 31-23.

J

Figure 3. Extended 34-Bit Format





Exponent	Fraction	Value	Name
511	Not all zeros	--	Not-A-Number
511	All zeros	$(-1)^S \times \infty$	Signed Infinity
-511 through 510	Any	$(-1)^S \times (1.F) \times 2^{E-127}$	Normalized Number
-512	Not all zeros	$(-1)^S \times (0.F) \times 2^{E-126}$	Denormalized Number
-512	All zeros	$(-1)^S \times 0.0$	Zero

Notes:

1. If an illegal operation generates a NAN, then F = 200000_H in the TMC3200 and F = 400000_H in the TMC3201.
2. $E = -2^9 E_9 + \sum_{i=0}^{8} 2^i E_i$ (true exponent = E -127 as in IEEE Format)

$$\text{Significand} = 2^0 + \sum_{i=0}^{22} 2^{i-23} F_i \quad \text{if } E > -512$$

$$\text{Significand} = \sum_{i=0}^{22} 2^{i-23} F_i \quad \text{if } E = -512$$

3. H, the hidden bit, is one except for zero and denormalized numbers, when it is zero.
4. F is a magnitude number.
5. E is a 10-bit two's-complement number. Note that the IEEE exponent is a subset of the extended-range exponent.
6. S, the sign bit, is in the LSW's MSB position.

Figure 4. Synchronization Timing Diagram

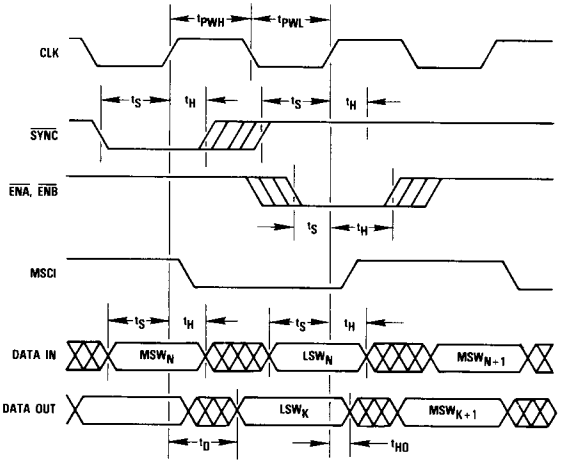


Figure 5. TMC3200 Non-Accumulate Mode Without Pipelining Timing Diagram

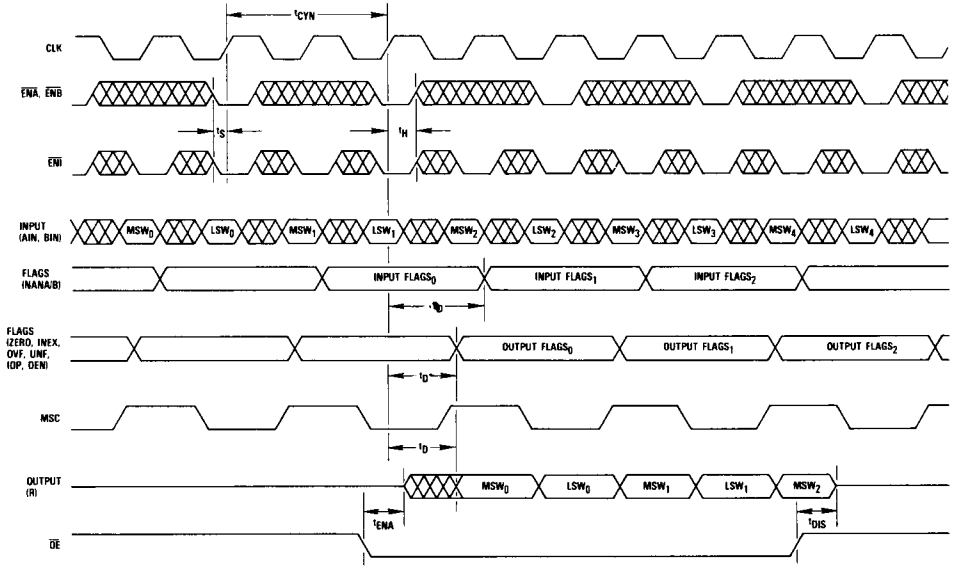
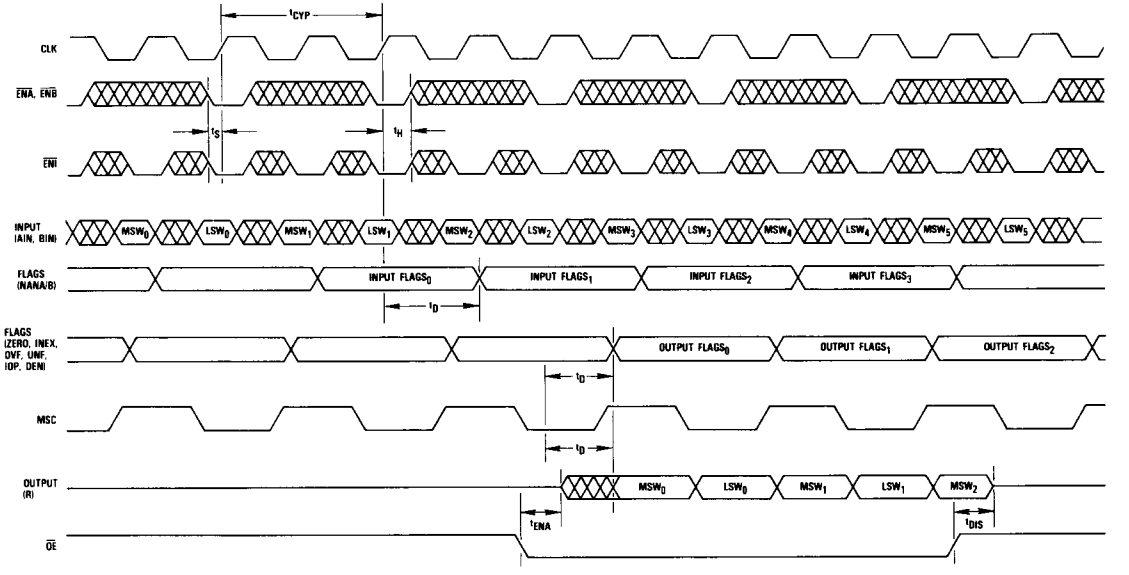


Figure 6. TMC3200 Non-Accumulate Mode With Pipelining Timing Diagram



J

Figure 7. TMC3200 Accumulate Mode Without Pipelining Timing Diagram

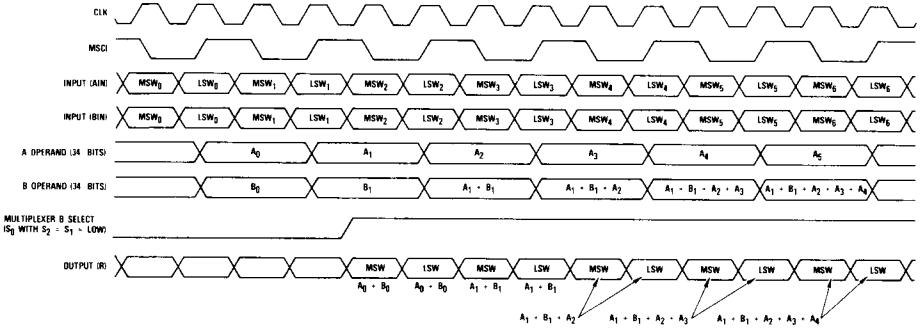


Figure 8. TMC3200 Accumulate Mode With Pipelining Timing Diagram

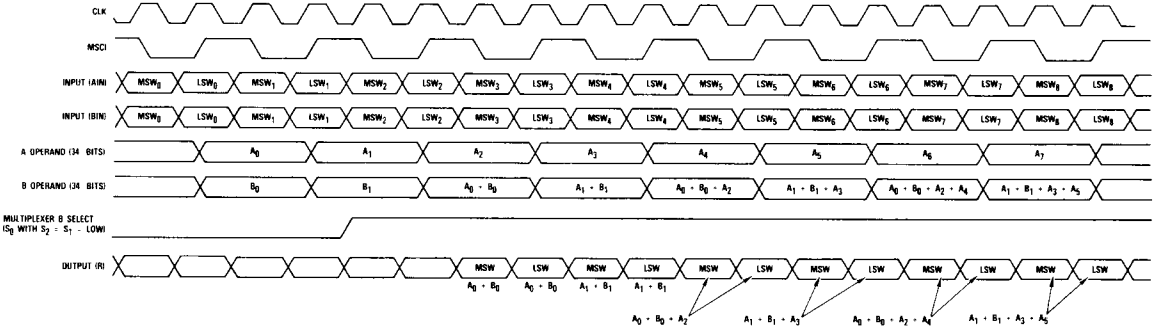


Figure 9. TMC3201 Multiplication Mode Without Pipelining Timing Diagram

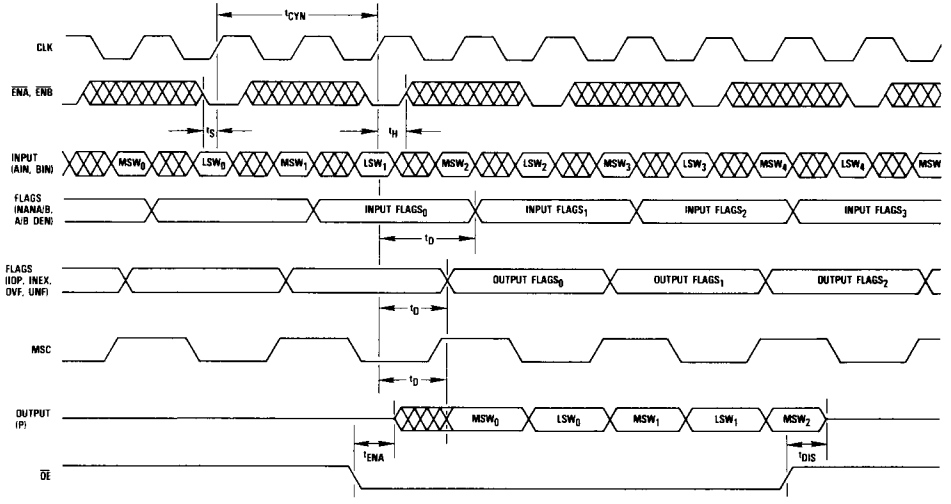


Figure 10. TMC3201 Multiplication Mode With Pipelining Timing Diagram

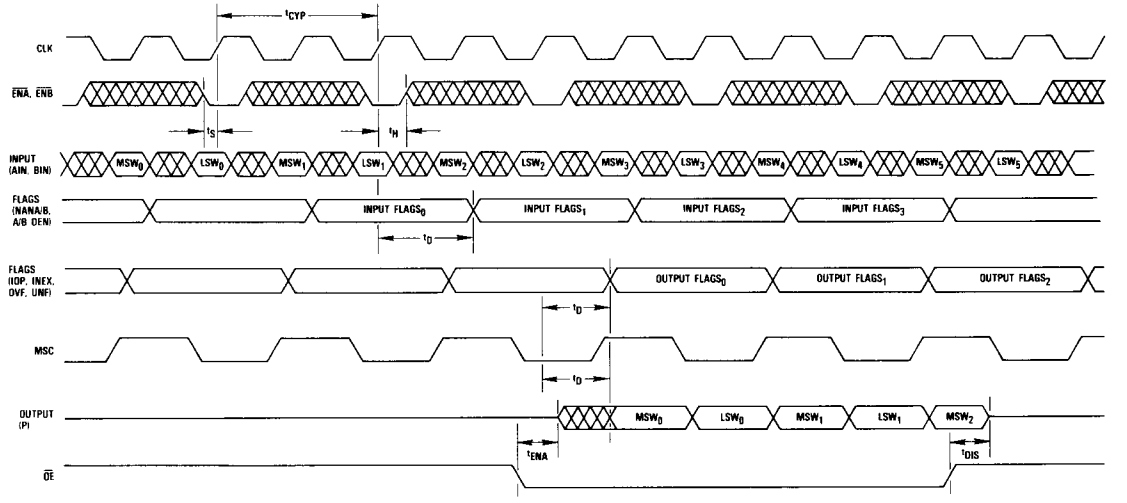


Figure 11. Equivalent Input Circuit

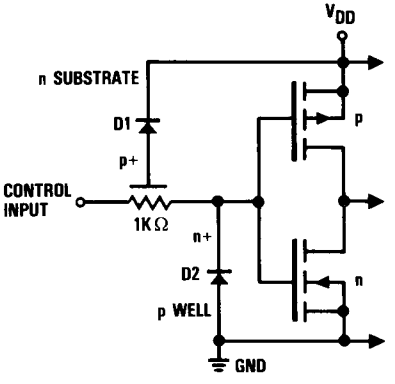


Figure 12. Equivalent Output Circuit

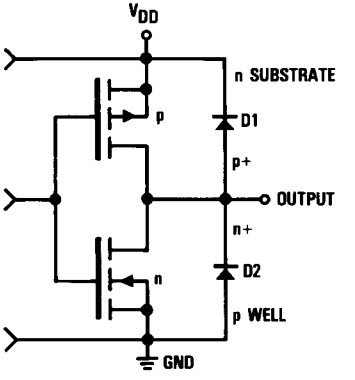
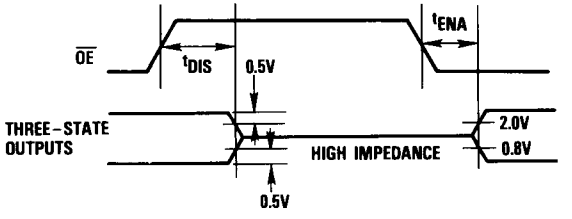


Figure 13. Threshold Levels For Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage [2]	−0.5 to (V_{DD} + 0.5)V
Forced current [3,4]	−1.0 to 6.0mA
Short circuit duration (single output in HIGH state to ground)	1 second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

DC characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OE}$ = 5V		20		20	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 16MHz, $\overline{OE}$ = 5V		30		30	mA
I_{DDL}	Supply Current, Loaded[2]	V_{DD} = Max, f = 16MHz, $\overline{OE}$ = 0V, C_{LOAD} = 40pF		50		50	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		-10		-10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{IL}	Input Voltage, Logic LOW			0.8		0.8	V
V_{IH}	Input Voltage, Logic HIGH	TMC3200	2.1		2.1		V
		TMC3201, (Except CLK)	2.2		2.2		V
		(CLK)	2.4		2.5		V
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = -2mA	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		-40		-40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		-100		-100	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		15		15	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		15		15	pF

Notes:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Worst case, all inputs and outputs toggling at specified rate.

J

AC characteristics within specified operating conditions

Parameter	Test Conditions	Temperature Range				Units
		Standard		Extended		
		Min	Max	Min	Max	
t_{CYP} Cycle Time, Pipelined	TMC3200, V_{DD} = Min		100		100	ns
	TMC3201, V_{DD} = Min		125		135	ns
t_{CYN} Cycle Time, Non-Pipelined	TMC3200, V_{DD} = Min		200		200	ns
	TMC3201, V_{DD} = Min		250		270	ns
t_{PWL} Clock Pulse Width, LOW	V_{DD} = Min	20		20		ns
t_{PWH} Clock Pulse Width, HIGH	V_{DD} = Min	20		20		ns
t_S Input Setup Time	TMC3200, (Except $\overline{ENI}$, $\overline{ENA}$, $\overline{ENB}$)	15		20		ns
	($\overline{ENA}$, $\overline{ENB}$)	0		0		ns
	($\overline{ENI}$)	5		5		ns
	TMC3201, (Except $\overline{ENA}$, $\overline{ENB}$)	15		20		ns
	($\overline{ENA}$, $\overline{ENB}$)	0		0		ns
t_H Input Hold Time	TMC3200, (Except $\overline{ENI}$, $\overline{ENA}$, $\overline{ENB}$)	0		0		ns
	($\overline{ENI}$, $\overline{ENA}$, $\overline{ENB}$)	15		15		ns
	TMC3201, (Except $\overline{ENA}$, $\overline{ENB}$)	3		3		ns
	($\overline{ENA}$, $\overline{ENB}$)	15		15		ns
t_D Output Delay	V_{DD} = Min, C_{LOAD} = 40pF					
	TMC3200, (Except NANA, NANB)		45		50	ns
	(NANA, NANB)		65		80	ns
	TMC3201, (Except ADEN, BDEN, NANA, NANB)		45		50	ns
	(ADEN, BDEN, NANA, NANB)		100		100	ns
t_{HO} Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	10		10		ns
t_{ENA} Three-State Output Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF					
	TMC3200		25		25	ns
	TMC3201		40		50	ns
t_{DIS} Three-State Output Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF					
	TMC3200		25		25	ns
	TMC3201		30		30	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3200G5C	STD–T_A=0°C to 70°C	Commercial	88 Pin Grid Array	3200G5C
TMC3200G5A	EXT–T_C=–55°C to 125°C	High Reliability	88 Pin Grid Array	3200G5A
TMC3201G5C	STD–T_A=0°C to 70°C	Commercial	88 Pin Grid Array	3201G5C
TMC3201G5A	EXT–T_C=–55°C to 125°C	High Reliability	88 Pin Grid Array	3201G5A

J