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ACL Products	

74AC/ACT11286

9-bit odd/even parity generator/ checker with bus drive I/O port

FEATURES

- Generates either odd or even parity for nine data lines
- Word length easily expanded by cascading
- Direct bus connection for parity generation or for checking by using the parity I/O port
- Glitch-free bus during power up/down
- Output capability: $\pm 24\text{mA}$
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11286 high-performance CMOS devices combine very high speed and high output drive compatible to the most advanced TTL families.

The 74AC/ACT11286 9-bit parity generator or checker is commonly used to detect errors in high-speed data transmission or data retrieval systems. It features

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
t_{PUH}/t_{PHL}	Propagation delay I_n to PARITY ERROR	$C_L = 50\text{pF}$	5.9	7.3	ns
C_{PD}	Power dissipation capacitance ¹	$f = 1\text{MHz};$ Enabled	53	56	pF
		$C_L = 50\text{pF}$ Disabled	46	50	
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	3.5	3.5	pF
C_{IO}	I/O capacitance	$V_{IO} = 0\text{V}$ or V_{CC} ; Disabled	8.5	8.5	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA

Note:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

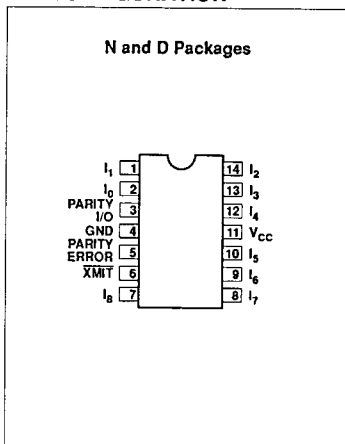
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

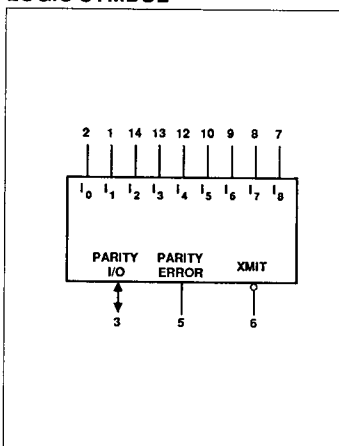
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to $+85^{\circ}\text{C}$	74AC11286N 74ACT11286N
14-pin plastic SO (150mil-wide)	-40°C to $+85^{\circ}\text{C}$	74AC11286D 74ACT11286D

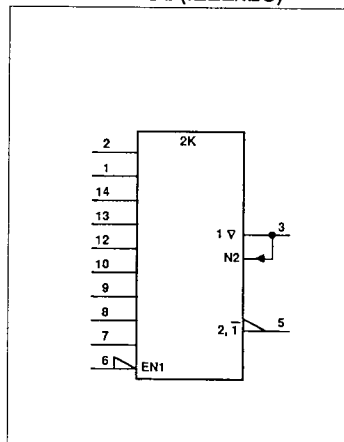
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



9-bit odd/even parity generator/checker
with bus drive I/O port

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tures a local output for parity checking
and a bus-driving parity I/O port for par-
ity generation/checking.

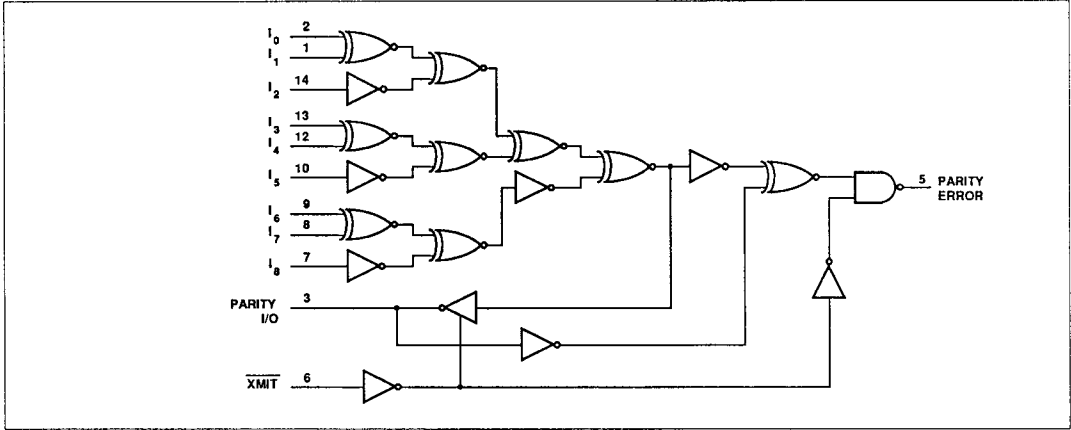
The $\overline{\text{XMIT}}$ control input is implemented
specifically for cascading for expanding
word length. When $\overline{\text{XMIT}}$ is held Low

the parity tree is disabled and the Parity
Error output remains at a High logic
level regardless of the other inputs ($I_0 - I_8$). When $\overline{\text{XMIT}}$ is High the parity tree
is enabled. Parity Error indicates a par-
ity error when either an even number of
inputs are High and Parity I/O is forced

to Low, or when an odd number of in-
puts are High and Parity I/O is forced
High.

The I/O control circuitry is designed so
that the I/O port will remain in the high-
impedance state during power-up or
power-down to prevent bus glitches.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 1, 14, 13, 12, 10, 9, 8, 7	$I_0 - I_8$	Data inputs
3	PARITY I/O	Parity I/O
6	$\overline{\text{XMIT}}$	Transmit input (active Low)
5	PARITY ERROR	Parity error output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

Number of High Data Inputs ($I_0 - I_8$)	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	L	H	H
1, 3, 5, 7, 9	L	L	H
0, 2, 4, 6, 8	h	h	H
	h	L	L
1, 3, 5, 7, 9	h	h	L
	h	L	H

L = Low voltage level input
h = High voltage level input
H = High voltage level output
L = Low voltage level output

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11286			74ACT11286			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} current		± 100	mA
	DC ground current		± 100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11286				74ACT11286				UNIT	
				T _{amb} = +25°C		T _{amb} = -40°C to +85°C		T _{amb} = +25°C		T _{amb} = -40°C to +85°C			
				V	Min	Max	Min	Max	Min	Max	Min		Max
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
			I _{OH} = -24mA	5.5	4.94		4.8		4.94		4.8		
				5.5			3.85				3.85		
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
			I _{OL} = 24mA	5.5		0.36		0.44		0.36			0.44
				5.5				1.65					1.65
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5		±0.5		5.0		±0.5		5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

9-bit odd/even parity generator/checker with bus drive I/O port

74AC/ACT11286**AC ELECTRICAL CHARACTERISTICS AT 3.3V $\pm 0.3V$**

SYMBOL	PARAMETER	WAVEFORM	74AC11286					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay I _n to PARITY I/O	1	2.6 3.8	10.0 11.6	11.7 14.5	2.6 3.8	13.1 16.1	ns
t _{PLH} t _{PHL}	Propagation delay I _n to PARITY ERROR	1	3.0 4.0	8.5 10.9	13.1 16.0	3.0 4.0	14.7 17.8	ns
t _{PLH} t _{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	2.2 3.4	5.9 7.9	7.6 10.2	2.2 3.4	8.4 11.1	ns
t _{PZH} t _{PHZ}	Propagation delay XMIT to PARITY I/O	2	1.8 3.2	4.9 5.4	6.4 6.6	1.8 3.2	7.0 7.0	ns
t _{PZL} t _{PLZ}	Propagation delay XMIT to PARITY I/O	2	3.5 3.2	9.7 5.4	12.8 6.7	3.5 3.2	13.6 7.2	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

SYMBOL	PARAMETER	WAVEFORM	74AC11286					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay I _n to PARITY I/O	1	2.0 3.1	5.5 6.9	8.0 9.1	2.0 3.1	9.0 10.7	ns
t _{PLH} t _{PHL}	Propagation delay I _n to PARITY ERROR	1	2.5 3.3	5.2 6.5	8.9 10.7	2.5 3.3	10.0 12.0	ns
t _{PLH} t _{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	1.9 2.9	3.9 5.0	5.6 7.2	1.9 2.9	6.2 7.9	ns
t _{PZH} t _{PHZ}	Propagation delay XMIT to PARITY I/O	2	1.4 3.1	3.3 4.8	4.9 6.1	1.4 3.1	5.3 6.5	ns
t _{PZL} t _{PLZ}	Propagation delay XMIT to PARITY I/O	2	3.0 3.0	5.4 4.6	8.3 6.0	3.0 3.0	8.9 6.3	ns

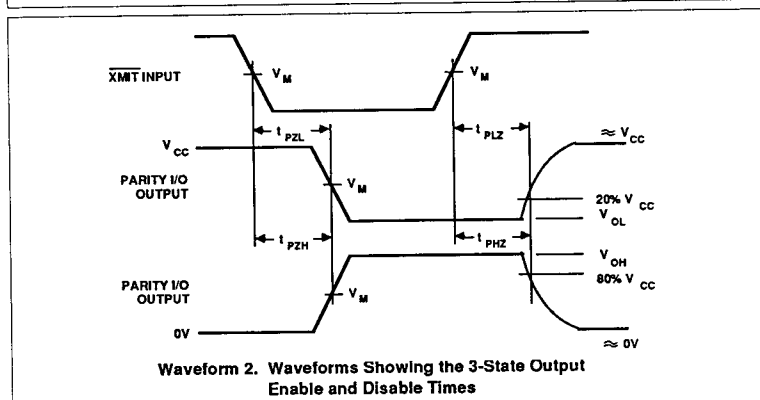
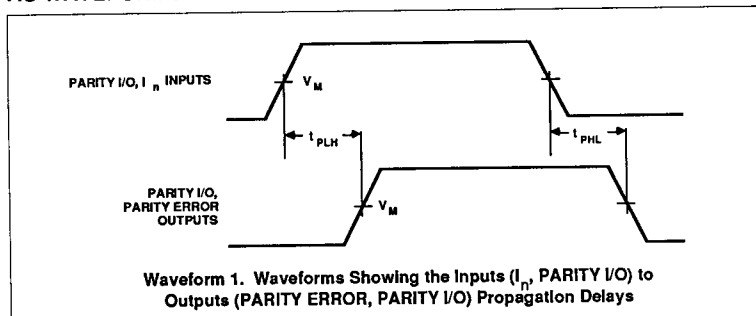
AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

SYMBOL	PARAMETER	WAVEFORM	74ACT11286					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay I _n to PARITY I/O	1	2.7 3.6	6.1 7.3	8.0 10.8	2.7 3.6	10.4 12.0	ns
t _{PLH} t _{PHL}	Propagation delay I _n to PARITY ERROR	1	3.0 3.9	6.9 7.7	9.7 11.4	3.0 3.9	11.3 12.9	ns
t _{PLH} t _{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	2.2 3.1	4.6 5.6	6.8 8.3	2.2 3.1	7.7 9.1	ns
t _{PZH} t _{PHZ}	Propagation delay XMIT to PARITY I/O	2	1.8 4.7	4.2 6.5	6.3 7.9	1.8 4.7	7.3 8.5	ns
t _{PZL} t _{PLZ}	Propagation delay XMIT to PARITY I/O	2	3.0 4.1	6.3 6.0	9.4 7.3	3.0 4.1	11.4 7.8	ns

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AC WAVEFORMS



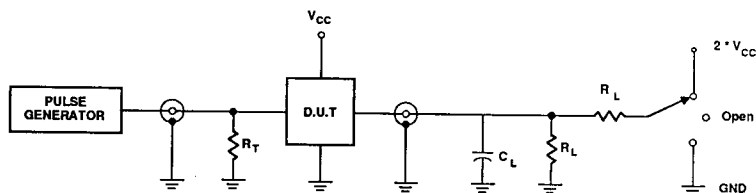
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC},$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V,$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

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TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500 Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: $PRR \leq 10\text{MHz}$

$t_r = t_f = 3\text{ns}$