



Integrated Device Technology, Inc.

3.3V FAST CMOS REGISTERED ADDRESS LINE DRIVER

IDT74ALVCH16345
IDT74ALVCH162345
ADVANCE INFORMATION

FEATURES:

- **Common features:**
 - 0.5 MICRON CMOS Technology
 - **Typical tsk(o) (Output Skew) < 250ps**
 - ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
 - 25 mil pitch SSOP, 19.6 mil pitch TSSOP,
and 15.7 mil pitch TVSOP packages
 - Extended commercial range of -40°C to +85°C
 - Vcc = 3.3V ±0.3V, Normal Range
 - Vcc = 2.7V to 3.6V, Extended Range
 - Vcc = 2.5V ±0.2V
 - CMOS power levels (0.4μW typ. static)
 - Rail-to-Rail output swing for increased noise margin
- **Features for ALVCH16345:**
 - High Drive Outputs: ±24mA
 - Suitable for heavy loads
- **Features for ALVCH162345:**
 - Light Balanced Output Driver: ±12mA
 - Minimal switching noise

DESCRIPTION:

The ALVCH16x345 is a registered address driver built us-

ing advanced dual metal CMOS technology. The device is configured with fan out of four use in high speed synchronous memory applications.

The ALVCH16x345 is ideal for driving memory modules in systems where multiple memory modules are used. Each of the four output banks drives a different module, modules can be added or removed without affecting the signal integrity of the other modules in the system.

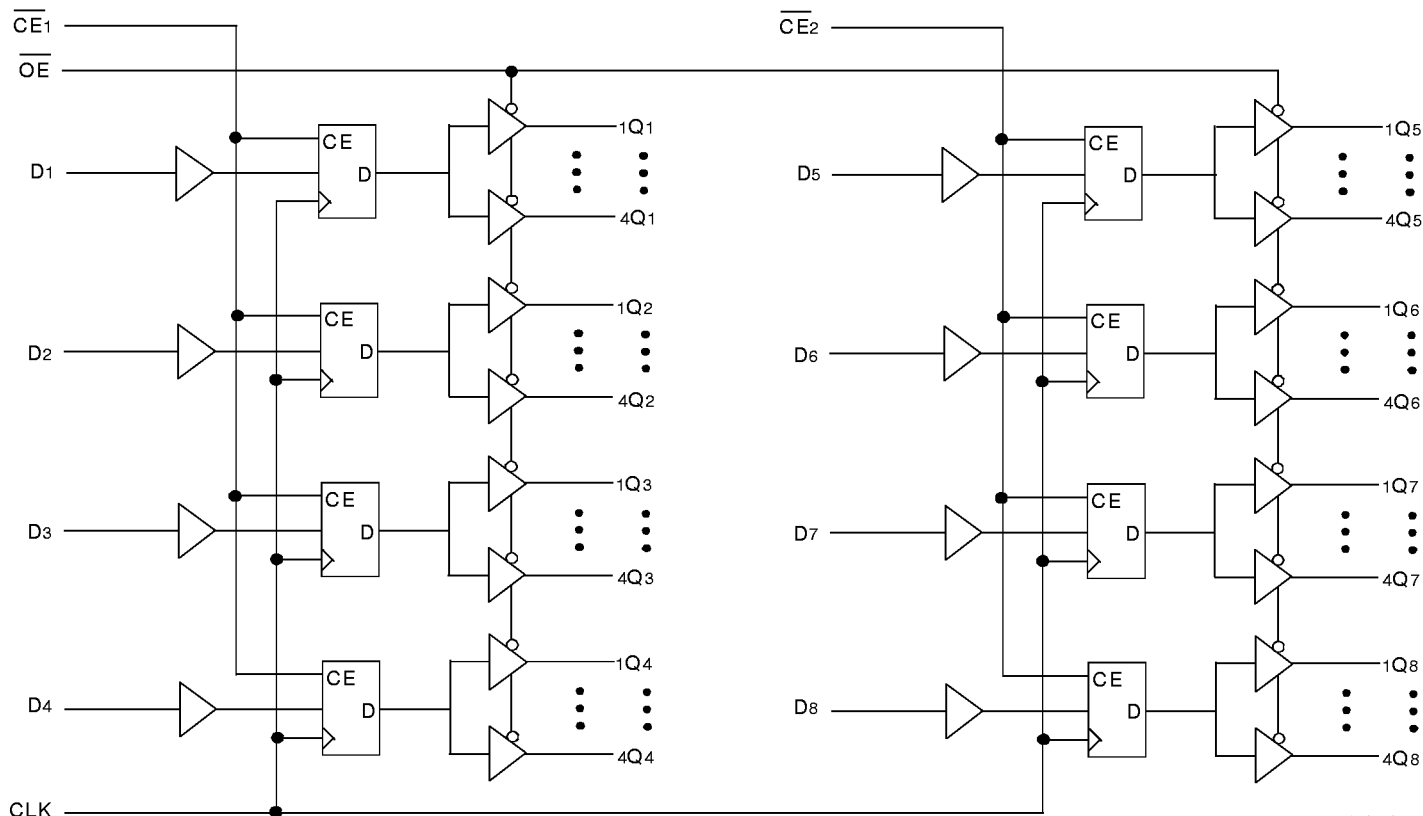
Dual Clock Enables CEx allow use of the ALVCH16x345 in high speed memory interleaving applications where the clock can be alternately enabled and disabled, allowing the address to be held for additional cycles during memory access.

The ALVCH16x346 have "bus-hold" which retains the input's last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistor.

The ALVCH16345 has been designed with a ±24mA output driver. These drivers are capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH162345 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

FUNCTIONAL BLOCK DIAGRAM



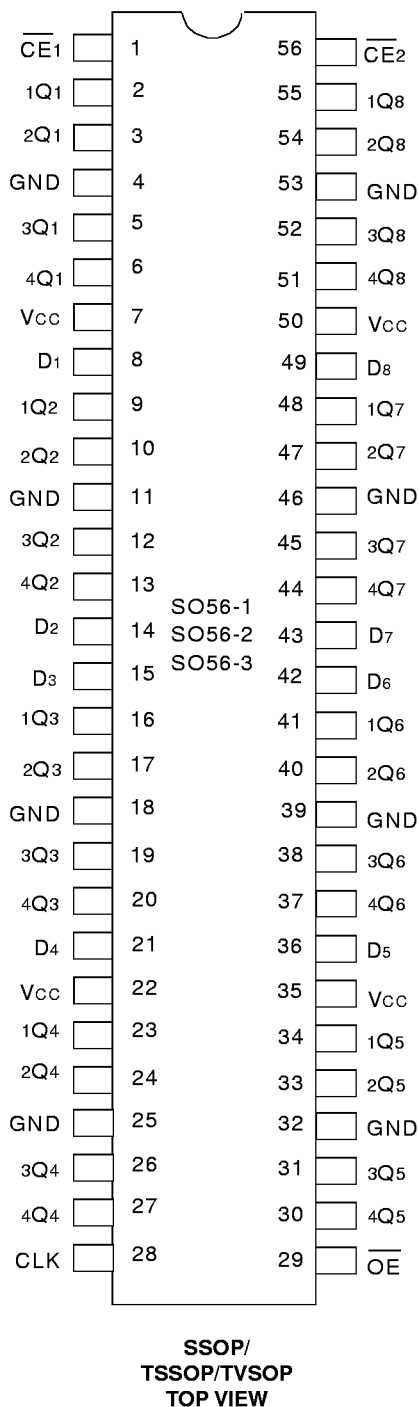
4215 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

EXTENDED COMMERCIAL TEMPERATURE RANGE

NOVEMBER 1997

PIN CONFIGURATION



4215 drw 02

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
Dx	Inputs ⁽¹⁾
xQx	3-State Outputs
CLK	Clock Input
$\overline{CE_x}$	Clock Enable (Active LOW)

4215 tbl 01

NOTE:
1. On ALVCH these pins have "Bus-hold". All other pins are standard inputs outputs or I/Os.

ABSOLUTE MAXIMUM RATING⁽¹⁾

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	mA
I _{IK} I _{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	-50	mA
I _{CC} I _{SS}	Continuous Current through each V_{CC} or GND	±100	mA

4215 lmk 02

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC} .

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	5.0	7.0	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	7.0	9.0	pF
C _{I/O}	I/O Port Capacitance	$V_{IN} = 0V$	7.0	9.0	pF

4215 lmk 03

NOTE:

- As applicable to the device type.

FUNCTION TABLE⁽¹⁾

Inputs				Outputs
$\overline{CE_x}$	CLK	$\overline{OE}$	Dx	xQx
H	X	L	X	B ⁽²⁾
X	L	L	X	B ⁽²⁾
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

4215 tbl 04

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- Output level before indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7 V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	±1	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	±1	
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	±1	μA
			V _O = GND	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCCL} I _{CCCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA

4215 Ink 05

BUS-HOLD CHARACTERISTICS FOR ALVCH16x345

Symbol	Parameter ⁽²⁾	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	-45	—	—	μA
			V _I = 0.7V	45	—	—	
I _{BHHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Pins with Bus-hold are identified in the pin description.

4215 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR ALVCH16345

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC-0.2	—	V
		VCC = 2.3V	IOH = -6mA	2	—	
		VCC = 2.3V	IOH = -12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = -24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

4215 Ink 07

OUTPUT DRIVE CHARACTERISTICS FOR ALVCH162345

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC-0.2	—	V
		VCC = 2.3V	IOH = -4mA	1.9	—	
		VCC = 2.3V	IOH = -6mA	1.7	—	
		VCC = 2.7V	IOH = -8mA	2	—	
		VCC = 3.0V	IOH = -6mA	2.4	—	
		VCC = 3.0V	IOH = -12mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 8mA	—	0.6	
		VCC = 3.0V	IOL = 12mA	—	0.8	

NOTE:

4215 Ink 08

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

SWITCHING CHARACTERISTICS FOR ALVCH16345⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ±0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay CLK to xQx	1.5	5.4	1.5	4.4	1.5	4.0	ns
t _{PZH} t _{PZL}	Output Enable Time OE to xQx	1.5	5.2	1.5	5.1	1.5	4.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE to xQx	1.5	5.5	1.5	4.5	1.5	5.2	ns
t _{SU}	Set-Up Time HIGH or LOW CE _x to CLK	1.5	—	1.5	—	1.5	—	ns
t _{SU}	Set-Up Time HIGH or LOW D _x to CLK	1.5	—	1.5	—	1.5	—	ns
t _H	Hold Time HIGH or LOW CE _x to CLK	0.5	—	0.5	—	0.5	—	ns
t _H	Hold Time HIGH or LOW CLK to D _x	0.5	—	0.5	—	0.5	—	ns
t _w	CLK Pulse Width HIGH or LOW	3.0	—	3.0	—	3.0	—	ns
t _{SK(o)}	Output Skew ⁽²⁾	—	500	—	500	—	500	ps
t _{SK(b)}	Output Skew ⁽²⁾	—	350	—	350	—	350	ps

4215 tbl 09

SWITCHING CHARACTERISTICS FOR ALVCH162345⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ±0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay CLK to xQx	1.5	—	1.5	—	1.5	4.5	ns
t _{PZH} t _{PZL}	Output Enable Time OE to xQx	1.5	—	1.5	—	1.5	5.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE to xQx	1.5	—	1.5	—	1.5	5.2	ns
t _{SU}	Set-Up Time HIGH or LOW CE _x to CLK	1.5	—	1.5	—	1.5	—	ns
t _{SU}	Set-Up Time HIGH or LOW D _x to CLK	1.5	—	1.5	—	1.5	—	ns
t _H	Hold Time HIGH or LOW CE _x to CLK	0.5	—	0.5	—	0.5	—	ns
t _H	Hold Time HIGH or LOW CLK to D _x	0.5	—	0.5	—	0.5	—	ns
t _w	CLK Pulse Width HIGH or LOW	3.0	—	3.0	—	3.0	—	ns
t _{SK(o)}	Output Skew ⁽²⁾	—	500	—	500	—	500	ps
t _{SK(b)}	Output Skew ⁽²⁾	—	350	—	350	—	350	ps

NOTES:

1. See test circuits and waveforms. T_A = −40°C to +85°C.
2. Skew between any two outputs of the same package switching in the same direction.

4215 tbl 10

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Standard Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2.0	30	μA
ΔI_{CC}	Quiescent Power Supply Current TTL Bus-hold Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	162	325	μA
I_{CCD}	Dynamic Power Supply Current ^(4,5)	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = GND$ One Input Bit Toggling Four Output Bits Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	140	190	$\mu A /$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = CEX = GND$ At $f_i = 5\text{MHz}$ 50% Duty Cycle One Input Bit Toggling Four Output Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—			mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	—			
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = CEX = GND$ At $f_i = 2.5\text{MHz}$ 50% Duty Cycle Eight Input Bits Toggling Thirty Two Output Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—			
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	—			

NOTES:

4215 tbl 11

- $V_{CC} (\text{max.}) = 3.6V$
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- $CPD = I_{CCD} / V_{CC}$
 $CPD = \text{Power Dissipation Capacitance}$
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot D_{HNT} + I_{CCD} \cdot (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

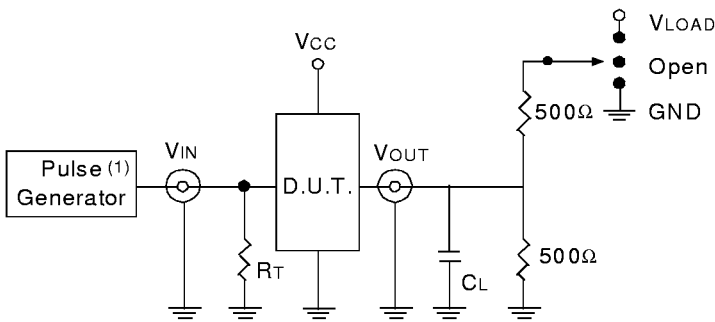
Symbol	V _{CC} = 3.3V ±0.3V	V _{CC} = 2.7V	V _{CC} = 2.5V±0.2V	Unit
V _{LOAD}	6	6	4.6	V
V _{IH}	2.7	2.7	2.3	V
V _T	1.5	1.5	V _{CC} /2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

4215 lmk 12

TEST CIRCUITS FOR ALL OUTPUTS

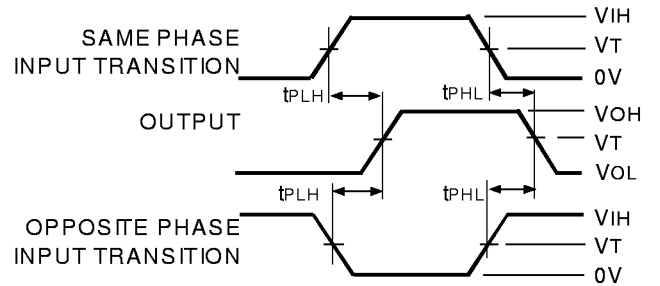


4215 drw 03

NOTE:

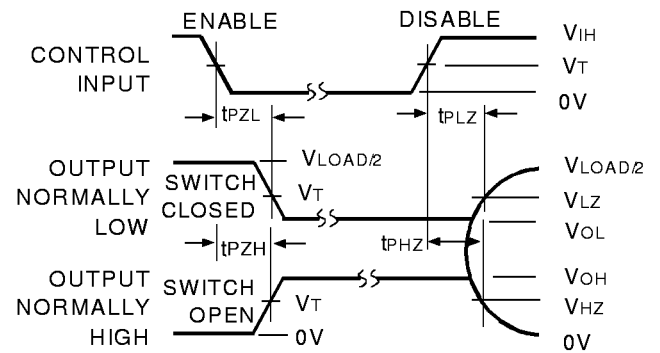
1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

PROPAGATION DELAY



4215 drw 05

ENABLE AND DISABLE TIMES



NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

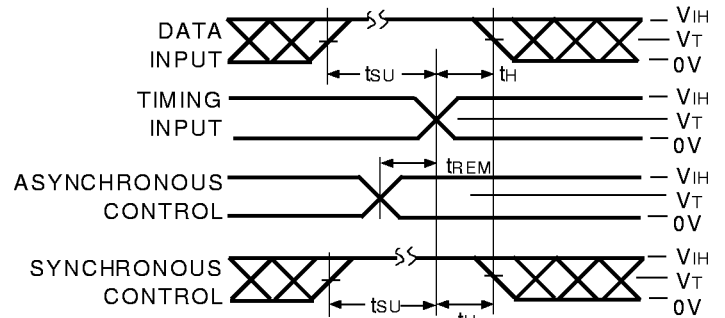
4215 drw 06

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

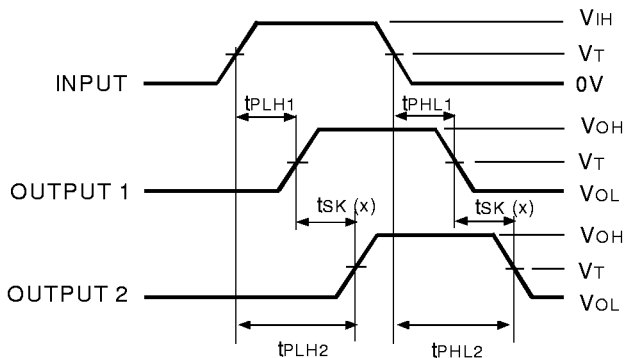
4215 lmk 13

SET-UP, HOLD AND RELEASE TIMES



4215 drw 07

OUTPUT SKEW - tsk (x)



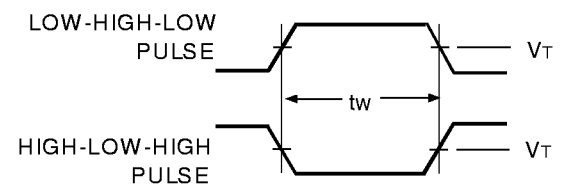
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

4215 drw 04

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.

PULSE WIDTH



4215 drw 08

ORDERING INFORMATION

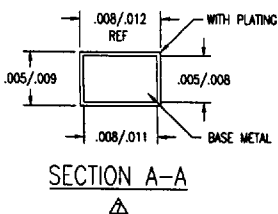
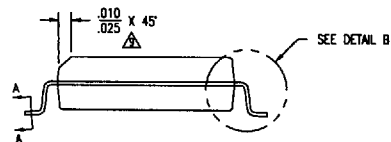
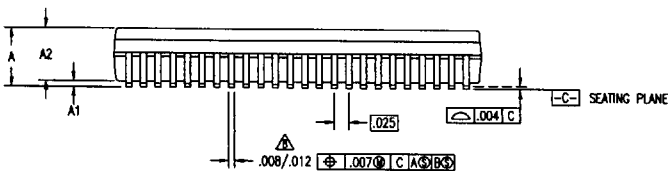
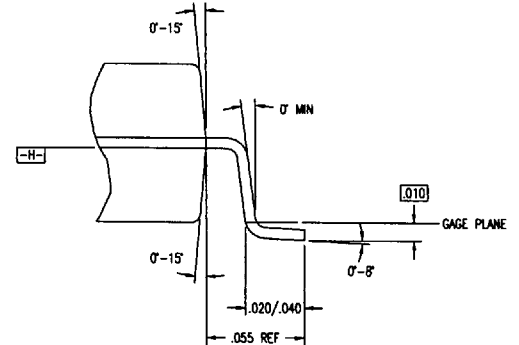
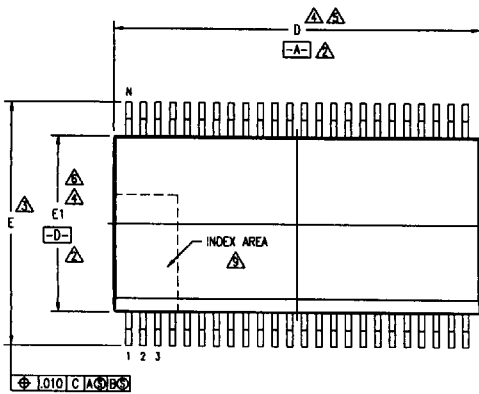
IDT	XX	ALVC	X	XX	XXX	XX	
Temp. Range	Bus-Hold	Family	Device Type	Package			
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					345		Registered 1 to 4 Address Line Driver
					16		Double-Density 3.3 Volt w/Resistors, ±24mA
					162		Double-Density 3.3 Volt w/Resistors, ±12mA
					H		Bus-hold
					74		−40 °C to +85 °C

4215 drw 09

PACKAGE DIAGRAM OUTLINES

SSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	



TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Slender Way, Santa Clara, CA 95054	
XXX	±	PHONE: (408) 727-8118	
XXXS		FAX: (408) 482-8874	
XXXSS		TWC: 910-338-2070	
APPROVALS	DATE	TITLE	REV
DRAWN AA	08/15/90	PV PACKAGE OUTLINE	02
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE C	
		DRAWING No. PSC-4029	
		DO NOT SCALE DRAWING	

PACKAGE DIAGRAM OUTLINES SSOP (Continued)

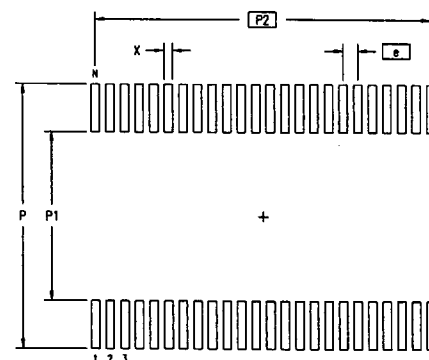
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WJ
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

DWG #		S048-1				DWG #		S056-1			
SYMBOL	JEDEC VARIATION				NOTE	JEDEC VARIATION				NOTE	
	AA			AB							
	MIN	NOM	MAX	MIN		NOM	MAX				
A	.095	.102	.110		.095	.102	.110				
A1	.008	.012	.016		.008	.012	.016				
A2	.088	.090	.092		.088	.090	.092				
D	.620	.625	.630	4,5	.720	.725	.730	4,5			
E	.395	.405	.420	3	.395	.405	.420	3			
E1	.291	.295	.299	4,6	.291	.295	.299	4,6			
N	48				56						

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARIATION AA & AB

LAND PATTERN DIMENSIONS



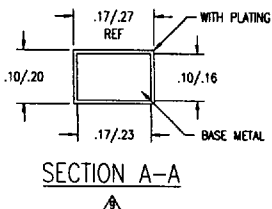
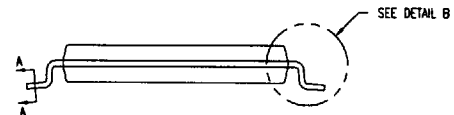
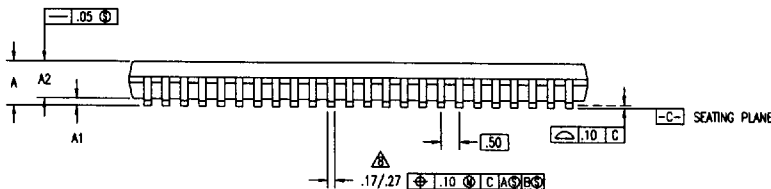
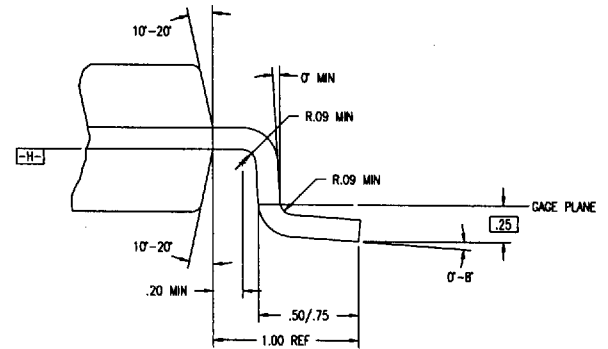
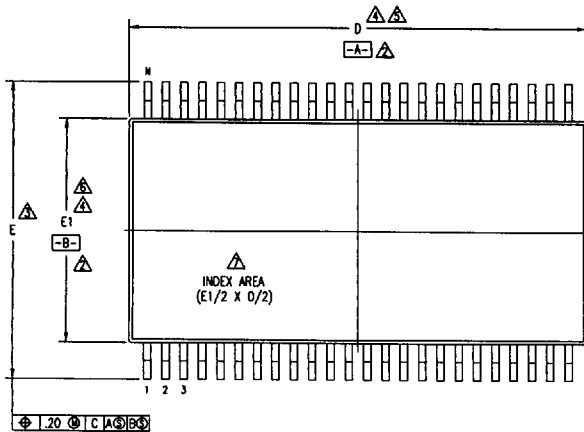
	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Stoner Way, Santa Clara, CA 95054	
X.XX	±	PHONE: (408) 727-8116	
X.XXX	±	FAX: (408) 482-8874	
X.XXX	±	TW: 810-338-2070	
APPROVALS	DATE	TITLE	REV
DRN	06/15/90	PV PACKAGE OUTLINE	
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE	REV
		C	02
		DRAWING No.	
		PSC-4029	
		DO NOT SCALE DRAWING	

PACKAGE DIAGRAM OUTLINES

TSSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	



TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, INC.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
XXX.X	±	PHONE: (408) 727-8118	
XXXX.X		FAX: (408) 492-8674	
XXXXX.X		TW: 910-336-2070	
APPROVALS	DATE	TITLE	REV
DRAWN	01/15/93	PA PACKAGE OUTLINE	
CHECKED		6.10 mm BODY WIDTH TSSOP	
		.50 mm PITCH	
		SIZE C	DRAWING No. PSC-4039
			REV 03
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES TSSOP (Continued)

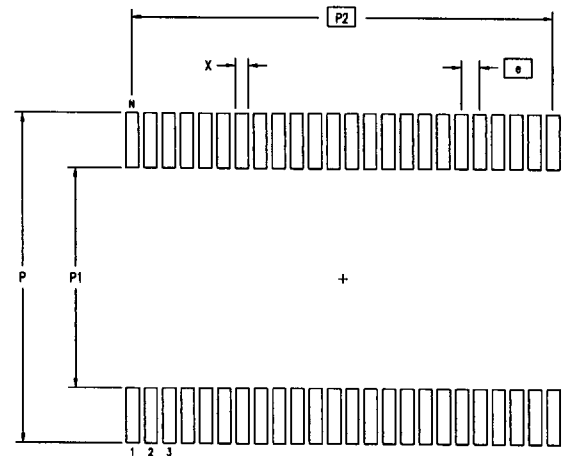
DWG #		S048-2			DWG #		S056-2				
SYMBOL	JEDEC VARIATION				NOTE	JEDEC VARIATION				NOTE	
	ED					EE					
	MIN	NOM	MAX			MIN	NOM	MAX			
A	—	—	1.10			—	—	1.10			
A1	.05	—	.15			.05	—	.15			
A2	.85	1.00	1.05			.85	1.00	1.05			
D	12.40	12.50	12.60	4,5		13.90	14.00	14.10	4,5		
E	7.95	8.10	8.25	3		7.95	8.10	8.25	3		
E1	6.00	6.10	6.20	4,6		6.00	6.10	6.20	4,6		
N	48					56					

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS $\square$ -A- and $\square$ -B- TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION E TO BE DETERMINED AT SEATING PLANE $\square$ -C-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MQ-153, VARIATION ED & EE

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

LAND PATTERN DIMENSIONS



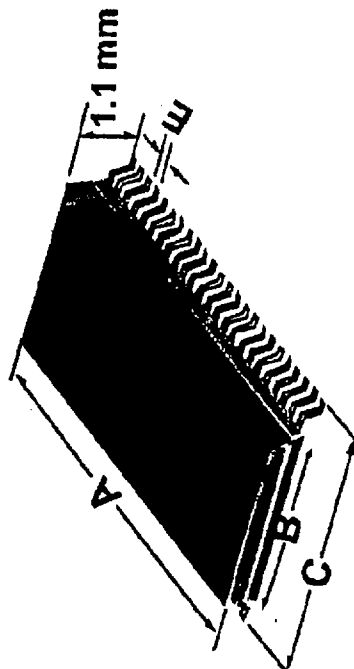
	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50	BSC	13.50	BSC
X	.30	.40	.30	.40
e	.50	BSC	.50	BSC
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Slender Way, Santa Clara, CA 95054	
±	±	PHONE: (408) 727-8118	
±	±	FAK: (408) 482-8874	
±	±	TWC: 910-338-2070	
APPROVALS	DATE	TITLE	PA PACKAGE OUTLINE
DRW	01/19/93	6.10 mm BODY WIDTH TSSOP	
CHECKED		.50 mm PITCH	
		SIZE	DRAWING No.
		C	PSC-4039
		DO NOT SCALE DRAWING	REV 03



TVSOP

The Most Compact Double Density Package

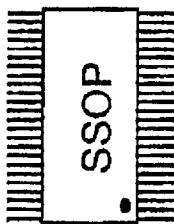


TVSOP Package	Typical Dimensions (in mm)				Area (mm ²)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50



Double Density Packaging

48-Pin



16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

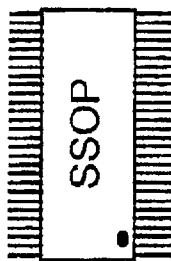


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²



9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin



18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²



14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²



11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm ²)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0