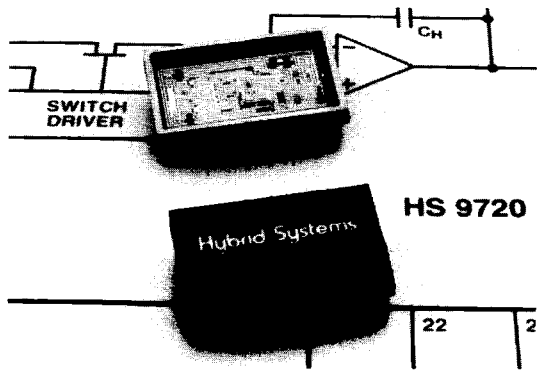
NOT RECOMMENDED FOR NEW DESIGNS SEE SP9730

HIGH SPEED, 12-BIT ACCURATE, SAMPLE/HOLD AMPLIFIER

FEATURES

- Pin-for-pin replacement for THA-05203, SHM-4860, TP-4860, MN376 and HTC-0300
- Hold mode feedthrough of −80 dB (20 Vp-p, 2.5 MHz)
- Maximum power dissipation 790 mW



DESCRIPTION

The HS9720 is a high speed sample/hold amplifier designed for use with 12-bit A/D converters. The maximum acquisition time of 200 nsec is specified to ±0.01% of 10V. The HS9720 is a complete sample/hold circuit containing a precision hold capacitor and a MOSFET switching driver. The HS9720 is particularly suited for use with high speed, 12-bit A/D converters.

The HS9720 is packaged in a 24-pin DIP and is specified for operation from 0°C to +70°C for commercial grades, and −55°C to +125°C for military grades. Full screening to MIL-STD-883C is available.

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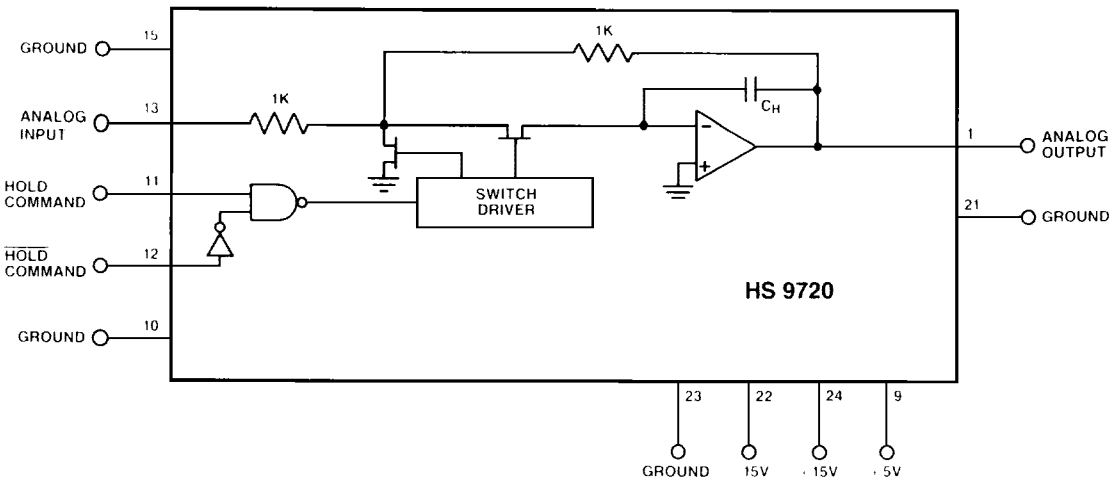
FUNCTIONAL DIAGRAM



SPECIFICATIONS

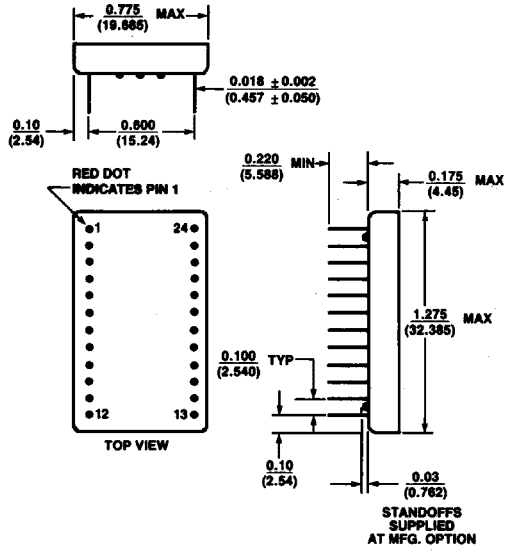
(Typical @ +25°C and nominal power supply voltages unless otherwise noted)

MODEL	HS 9720K	HS 9720TB
ANALOG INPUT		
Voltage Range	±11.5V typ, ±10.25V min	*
Input Impedance	1KΩ	*
DIGITAL INPUT[1]		
Logic "1"	+2V min to +5V max	*
Logic "0"	0V min to +0.8V max	*
Loading[2]	1 TTL Load	*
ANALOG OUTPUT		
Voltage	±11.5V typ, ±10.25V min	*
Current	±20 mA	*
Impedance	0.5Ω	*
Maximum Capacitive Load	200 pF	*
DC ACCURACY/STABILITY		
Gain	−1.00 V/V	*
Gain Error	±0.01% typ, ±0.1% max	*
Gain Nonlinearity	±0.005% typ, ±0.01% of FS max	*
Gain Drift	±1 ppm/°C typ, ±5 ppm/°C max	*
Offset	±0.5 mV, ±5 mV max	*
Offset Drift	±5 mV typ, ±20 mV max over full temperature range	*
TRACK (SAMPLE) MODE DYNAMICS		
Frequency Response		
Small Signal (−3 dB)	13 MHz typ, 8 MHz min	*
Full Power Bandwidth	3.5 MHz typ, 2.4 MHz min	*
Slew Rate	170V/μsec typ, 150V/μsec min	*
Noise in Track Mode		
DC to 5 MHz	90 μV rms	*
DC to 1 MHz	40 μV rms	*
DC to 0.1 MHz	13 μV rms	*
TRACK (SAMPLE)-TO-HOLD SWITCHING		
Aperture Delay[5]	6 nsec, 10 nsec max	*
Aperture Uncertainty	±50 psec	*
Offset Step (Pedestal)	±0.5 mV typ, ±10 mV max	*
Offset Step (Pedestal) Drift	±4 ppm of FSR/°C	*
Switching Transient		
Settling to ±10 mV (±0.1% FS)	40 nsec	*
Settling to ±1 mV (±0.01% FS)	60 nsec, 100 nsec max	*
Amplitude	180 mVp-p	*
HOLD MODE DYNAMICS		
Droop Rate	±0.5 μV/μsec, ±5 μV/μsec max	*
Droop Rate at T_{max}	±1.2 mV/μsec max	*
Feedthrough Rejection (20 Vp-p @ 2.5 MHz)	−90 dB typ, −80 dB min	*
HOLD-TO-TRACK (SAMPLE) DYNAMICS		
Acquisition Time to ±0.01% of 10V (±1 mV)	160 nsec, 200 nsec max	*
Acquisition Time to ±0.1% FS of 10V (±10 mV)	100 nsec, 170 nsec max	*
Acquisition Time to ±1% FS of 10V (±100 mV)	90 nsec	*
Acquisition Time to ±1.0% FS of 1V (+100 mV)	75 nsec	*
POWER REQUIREMENTS		
Nominal Voltages for Rated Performance	±15V (±3%)	*
	+5V (±5%)	*
Supply Current		
+15V	25 mA max	*
−15V	−25 mA max	*
+5V	+8 mA max	*
Power Dissipation	790 mW max	*
Power Supply Rejection	±0.5 mV/V	*
TEMPERATURE RANGE		
Operating	0°C to +70°C	−55°C to +125°C
Storage	−40°C to +85°C	−65°C to +155°C
PACKAGE		
24-Pin Double DIP		

NOTES:

1. Logic "1" to pin 12 or logic "0" to pin 11 will put the HS 9720 into the track (sample) mode.
2. One TTL load is defined as sinking 40 μA with a logic "1" applied and sourcing 1.6 mA with a logic "0" applied.
3. Manufacturer's option.
4. Lid is internally grounded.
5. From HOLD command pin 11.
6. FSR = 20 Volt Full Scale Range, FS = 10 Volt Full Scale

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG OUTPUT	24	+15V
2	NC	23	GROUND
3	NC	22	−15V
4	NC	21	GROUND
5	NC	20	NC
6	NC	19	NC
7	NC	18	NC
8	NC	17	NC
9	+5V	16	NC
10	GROUND	15	GROUND
11	HOLD COMMAND	14	NC
12	$\overline{\text{HOLD}}$ COMMAND	13	ANALOG INPUT

NC — No internal connection

ABSOLUTE MAXIMUM RATINGS

(Referenced to ground. Exceeding any one of these parameters may cause permanent damage to the unit.)

Voltage Between + 15V and − 15V Terminals	36V
Analog Input Voltage	Actual Supply Voltage
Digital Input Voltage	−0.5V to +5.5V
Output Current, Continuous	±50 mA
Storage Temperature Range	−65°C to +150°C
Output Short-Circuit to Ground	Indefinitely
Lead Temperature (Soldering, 10 secs.)	+300°C

OPERATING INSTRUCTIONS

Sample/Hold Control

A TTL logic "0" applied to pin 11 (or a logic "1" applied to pin 12) will put the HS 9720 into the track (sample) mode. In this mode, the device acts as an amplifier which exhibits normal operational behavior. Application of a logic "1" to pin 11 (or a logic "0" applied to pin 12) will put the HS 9720 into the hold mode, with the output voltage held constant at the value present when the hold command is given.

INSTALLATION

Grounding

The HS 9720 is a high speed, 12-Bit accurate sample/hold amplifier. Grounding of this component must be done with care for full performance. The HS 9720 has four ground pins (pins 10, 15, 21, and 23). All must be tied together and connected to system analog ground as close to the package as possible. It is preferable to have a large analog ground plane beneath the HS 9720 and have all four ground pins soldered directly to it. Pin 10 is particularly noise sensitive because the fast switching currents from the switch drivers are grounded to this pin. Therefore, most digital ground currents will be routed through pin 10. Care must be taken to insure that no ground potentials exist between pin 10 and the other ground pins. Therefore, pin 10 must be tied to the analog and not the digital ground system.

DECOUPLING

Internal 0.01 μF power supply bypass capacitors are included in the HS 9720 to maintain device stability. If the supply voltages contain excessive high frequency noise, additional external high frequency capacitors may be necessary to maintain low noise performance.

OUTPUT LOADING

A capacitive load more than 50 pf will result in degrading acquisition time. Capacitive loads more than 250 pf will result in a continuous oscillation. The specified load resistor is 500Ω min. Lower value loads can be driven if the input/output range is lowered and the load current does not exceed ±20 mA.

KEY SPECIFICATIONS DETERMINING 12-BIT ACCURACY

The key specifications of the HS 9720 which support its accuracy to 12 bits are listed below.

1. Gain Nonlinearity — For a ±10V output range, gain nonlinearity is ±0.01% max which is less than ½ LSB at 12 bits (0.012%).

2. Noise in Track Mode — For a noise bandwidth between DC and 5 MHz, the noise is specified at 90 μV rms. Since ½ LSB at 12 bits is 2.4 mV (FSR = 20V), the noise level is well below that required for 12-Bit accuracy.

3. Droop — The droop rate is specified at ±5 μV/ μsec max. For a 2.4 mV change (½ LSB, 12 bits, FSR = 20V), this S/H can accurately hold a signal for 480 μsec. The droop rate at +125°C is specified at 1.2 mV/ μsec max. Thus, for a 2.4 mV change, the HS 9720 can accurately hold a signal for 2 μsec at +125°C.

4. Acquisition Time — This is specified at 200 nsec max settling to ±0.01% of 10V, or ½ LSB at 12 bits.

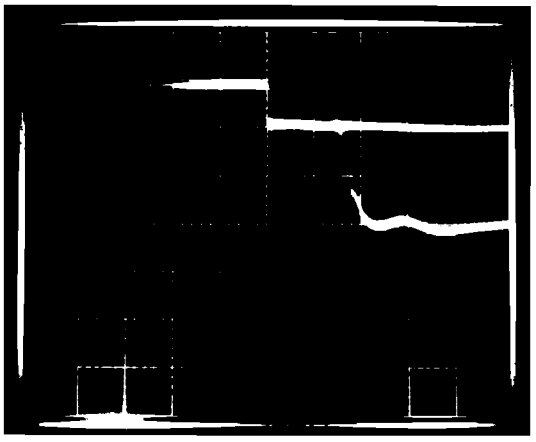
5. Feedthrough — Feedthrough rejection is specified at −90 dB typ, −80 dB min for a 20 Vp-p, 2.5 MHz input signal. This means that the hold mode will move no more than −80 dB less than the input. For a ±10V input, this is less than ½ LSB at 12 bits.

DISCUSSION OF SPECIFICATIONS

TERMINOLOGY

Sample/Hold Amplifier is actually a more common name for what really is a track/hold (T/H) amplifier. A true S/H amplifier normally spends most of its time in the hold mode. When commanded to the sample mode, it will take a very fast sample and immediately go back into the hold mode. A true T/H amplifier can track the input indefinitely and it can be in the hold mode indefinitely. In practice, most S/H amplifiers manufactured today are actually T/H amplifiers. This is why the HS 9720 data sheet specifies track (sample) in many places.

Acquisition Time is the time required by the device to "switch" from the hold mode to the track (sample) mode. This time is measured between the application of a "track" command and the point at which the output has settled to within a specified error band. This time includes the switch delay time, slewing time and settling time for a given output voltage change.



Acquisition Time of a + 10V Input Step

Top trace shows hold command going low in the middle of the photo. Lower trace shows output settling to a 2 mV/div. vertical scale. Horizontal scale is 100 nsec/div.

Switching Transient Settling (Hold Mode Settling) is the time required for the device to stabilize in the hold mode to within specified limits of its final value after the hold mode signal has been given.

Aperture Delay is the time lag between the application of the "hold" command and the instant the output stops tracking the input. It consists primarily of the propagation delay of the switch driver. Since it is a known quantity, the "hold" command can be advanced to account for this delay.

Aperture Uncertainty (Jitter) is the variation in the aperture delay from sample to sample. This time uncertainty produces a voltage uncertainty proportional to the input slew rate.

Offset Step (Pedestal) is a track (sample)-to-hold offset that results from unequal charge transfers when the device is switched into the hold mode.

Feedthrough is the amount of analog input signal that is coupled through to the analog output while the circuit is in the hold mode. It is usually expressed as a ratio in dB's. Since feedthrough increases with frequency, it should be specified at a given frequency.

Droop Rate is the rate of change in output voltage over time while in the hold mode. The droop rate will determine how long a signal can be accurately held before it changes more than 1 LSB. This, in turn, determines the maximum conversion time that an A/D converter can have to be used with a particular S/H.

Full Power Bandwidth is the frequency at which a full scale input/output sine wave becomes slew rate limited to −3 dB.

Small Signal Bandwidth is the maximum analog signal frequency that can be tracked before the gain is reduced by 3 dB. This assumes the signal amplitude is small enough so as not to be slew rate limited.

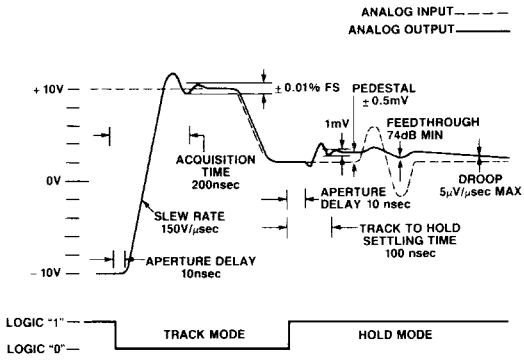


Figure 1. Pictoral Showing Various S/H Characteristics

APPLICATIONS

DIGITIZING DYNAMIC SIGNALS

Sample/hold amplifiers are normally used in front of A/D converters to hold the input voltage constant during conversion. Digitizing errors will result if the analog input signal varies by more than ½ LSB during conversion. In the case of the HS 9548, a 12-Bit A/D with a conversion time of 500 nsec to 12 bits, this results in a low input frequency which can be accurately digitized as explained below:

For a sine wave input, its maximum rate of change is calculated as 2π Af where f = frequency and A = amplitude. If one allows a ½ LSB change (2.4mV) during conversion for a ± 10V input swing to the A/D converter, the maximum rate of change limit would be 2.4mV/2 μsec, or 1.2mV/ μsec. Thus, the maximum sine wave input frequency that can be accurately digitized is calculated as:

$$1.2\text{mV}/\mu\text{sec} = 2\pi\,\text{Af}$$

For a ± 10V input sine wave, this frequency limit is 19 Hz.

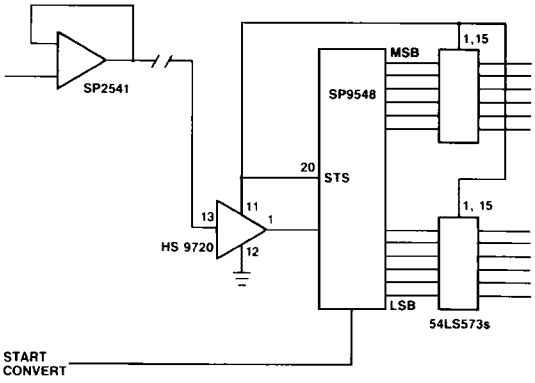
Expressed differently, the full scale bandwidth of the A/D is slew rate limited to 19 Hz. By using a S/H, such as the HS 9720 in front of the A/D , this bandwidth can be significantly increased. The S/H will "freeze" an input signal that is changing too rapidly for the A/D alone to handle and hold it constant while the A/D performs a conversion. A S/H can accurately "freeze" signals moving as fast as ½ LSB during its aperture uncertainty of 50 psec. Thus, the maximum rate of change limit would be 2.4mV (½ LSB, 12 bits, ± 10V swing) during 50 psec, or 48V/μ sec, which is within the slew limit of the HS 9720 (150V/μ sec min). Thus, the maximum full scale input frequency that can be accurately digitized is calculated as:

$$48V/\mu \text{ sec} = 2\pi Af$$

For a ± 10V full scale input, this frequency limit is 760 kHz. Expressed differently, the slew rate limited full scale bandwidth has now been increased to 760 kHz with the use of the HS 9720.

Throughput and the Nyquist criteria are other factors which will determine the highest input signal frequency that can be sampled. For the combination of 2μ sec ADC and the HS 9720, the throughput is related to the sum of the conversion time of the A/D (2 μ sec), the acquisition time of the S/H (0.2 μ sec) and the hold mode (switching transient) settling time of the S/H (0.1 μ sec). The total of 2.3μ sec represents a throughput of 434 kHz. Based on the Nyquist criteria of sampling more than twice per cycle, the highest input signal frequency that can be accurately digitized is slightly less than 217 kHz.

TYPICAL APPLICATION



Two importantly overlooked parameters are output impedance and settling time. The A/D is the S.A.R. type which means a current is injected into a comparator mode. This has a result of "dragging" the analog input to a new and distored value. The S/H must recover the signal to the original value before the comparator makes it's decision. For a 1.5μsec conversion this is 115 nanoseconds. The HS 9720 settles within a 100 nanoseconds, allowing it to be used with fast S.A.R. type A/Ds. Output impedance is also important because the input impedance of the A/D is relatively low (10kΩ). With a low output impedance of 0.5Ω max, this allows for very little distortion due to the HS 9720, and an adequate drive capability.

TRACK/HOLD COMMAND

There are two hold commands for the HS 9720, the HOLD AND $\overline{\text{HOLD}}$. To use the HOLD command, tie $\overline{\text{HOLD}}$ (pin 12) to a TTL logic 0. To generate a track command apply TTL logic 0 to HOLD (pin 11). In this mode, the HS 9720 will effectively be an op-amp in the − 1 gain mode. A TTL logic 1 will put the HS 9720 into the hold command.

To incorporate the $\overline{\text{HOLD}}$ (pin 12), tie the HOLD (pin 11) to a TTL logic 1. A TTL logic 1 will put the HS 9720 into the track mode, a TTL logic 0 will put the HS 9720 into the hold mode. In using the $\overline{\text{HOLD}}$ command, there will be an additional delay of 4 nsec (typ), 12 nsec (max). This will increase aperture delay to 22 nsec (max), but will have no effect on settling time, acquisition time, gain, etc.

DRIVING THE INPUT OF THE HS 9720

The input resistance of the HS 9720 is a 1kΩ (typical) load. If driven by a weak source a loss of accuracy can occur due to the relatively low input impedance of the HS 9720. This is especially true, if the source is driving a long cable with a high capacitive load. A high speed, low output resistance op-amp should be used to drive the HS 9720 (such as the SP2541) to increase system performance and accuracy.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	MIL PROCESSING
HS 9720K	0°C to + 70°C	–
HS 9720TB	− 55°C to + 125°C	883C

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