U 3800 BM

Multi Standard Feature Phone Integrated Circuit

Description

The U 3800 BM multi-standard feature phone circuit is designed to be used with a microcontroller using a 2-wire serial bus. It performs all speech and line interface functions required in an electronic telephone set: the ringing function with switching regulator and melody generator, the DTMF dialling, the loudhearing with antilarsen and antidistortion systems, a power supply, a clock and a reset for the microcontroller. Transmit, receive and loudhearing gains control / AGC range / DTMF frequencies, pre-emphasis and level / melody generator, and mutes are programmable through the serial bus.

Features

- Slope of DC characteristics adjustable by an external resistor.
- Gain of transmit and receive amplifiers automatically adjusted by line length control
- Regulation range adjustable by the serial bus
- Possibility of fixed gain (PABX)
- Sidetone balancing system adjustable with line length or by the serial bus.
- Dynamic impedance adjustable by external components.
- Stabilized power supply for peripherals.
- Confidence level during dialling.
- + 6 dB possibility on second stage transmit gain.
- Transmit and receive gains adjustable by serial bus.
- Extra transmit input for handsfree and answering machine purpose.
- + 6 dB possibility on receive gain.
- Receive amplifier for dynamic or piezo-electric earpieces.
- Extra receive output for handsfree purpose.
- High impedance microphone inputs are suitable for dynamic, magnetic, piezo-electric or electret microphone.
- Dynamic range limitation in transmission (anticlipping) prevents distortion of line signal and sidetone.
- Squelch system in transmission prevents "room noise" are being transmitted, and improves antilarsen efficiency (can be inhibited).
- Loudhearing gain programmable in eight steps of 4 dB using the serial bus, or linearly adjusted using a potentiometer.
- Antilarsen system efficiency is increased when inhibiting squelch.
- Loudhearing antidistortion system by automatic gain control versus available current.
- Switching regulator in ringing phase
- Input ringing detection, threshold and impedance adjustable with external resistors.
- Ringing zero crossing information for external microprocessor.
- Ringing programmable gain in eight steps of 4 dB using the serial bus.
- Melody generator, with 30 frequencies in steps of semi tones, driven by serial bus.
- Internal speed-up circuit permits a faster charge of VDD and VCC capacitor.
- DTMF dialer driven by serial bus, in particular level and pre-emphasis adjustment.
- Ability to transmit a confidence tone in speech mode using melody generator frequencies.
- Five independent mutes driven by serial bus (two in transmission, two in reception, one for the transmit / receive loop).
- Standard low cost ceramic 455 kHz / clock output for the microcontroller.

Applications

- Feature phones
- Answering machines
- Fax machines

Benefits

- Complete system integration of analog signal processing and digital control circuitry
- One IC for various PTT standards, e.g. programmable specification via µC
- Only three low-cost transducers needed (instead of four)

Figure 1. Block Diagram

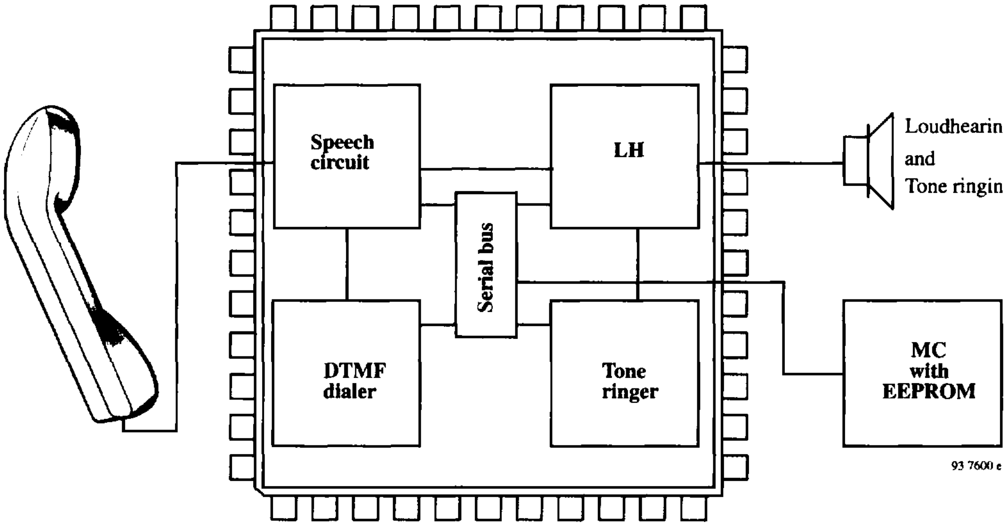

Figure 2. Block Diagram

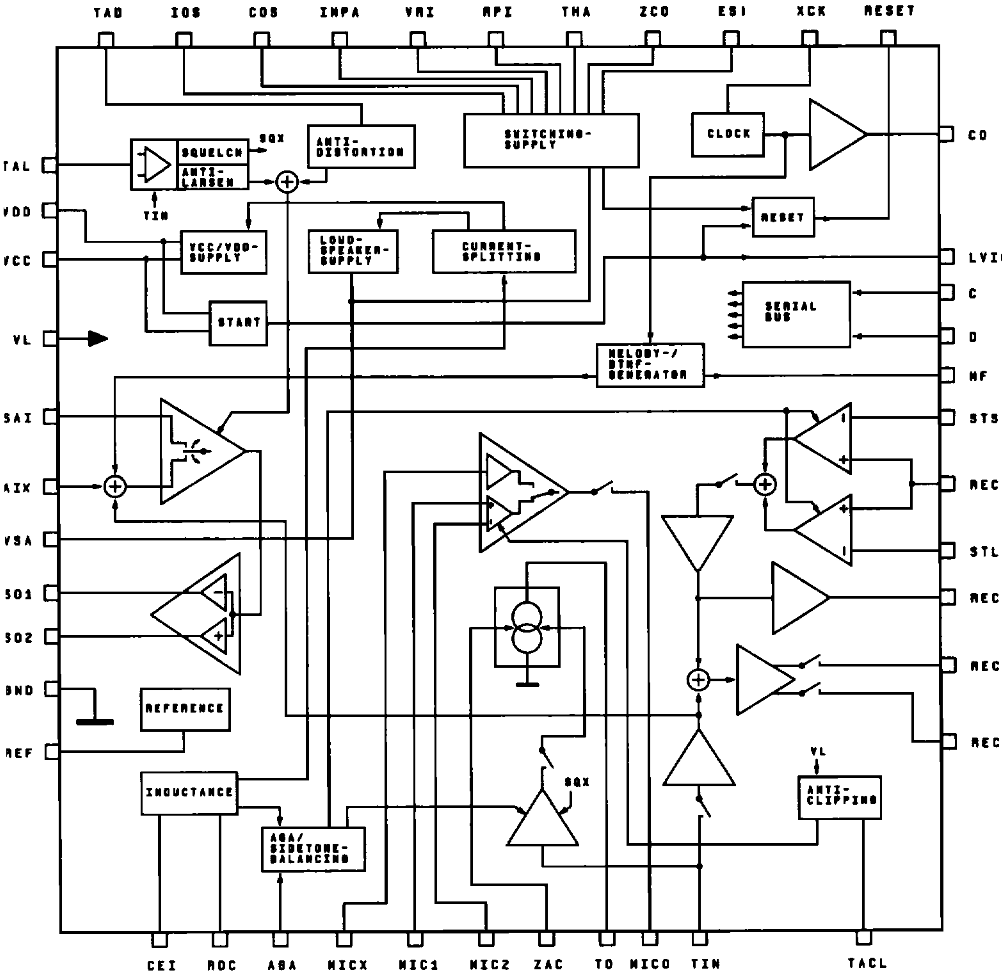

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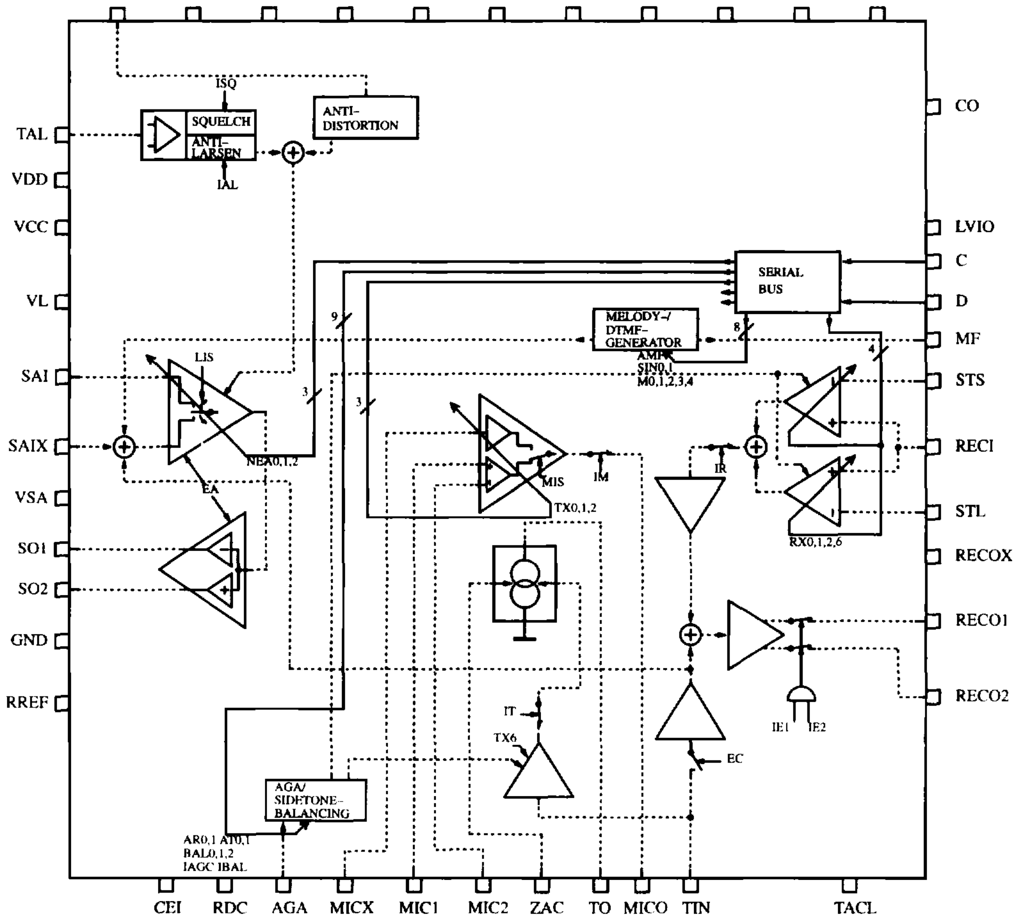
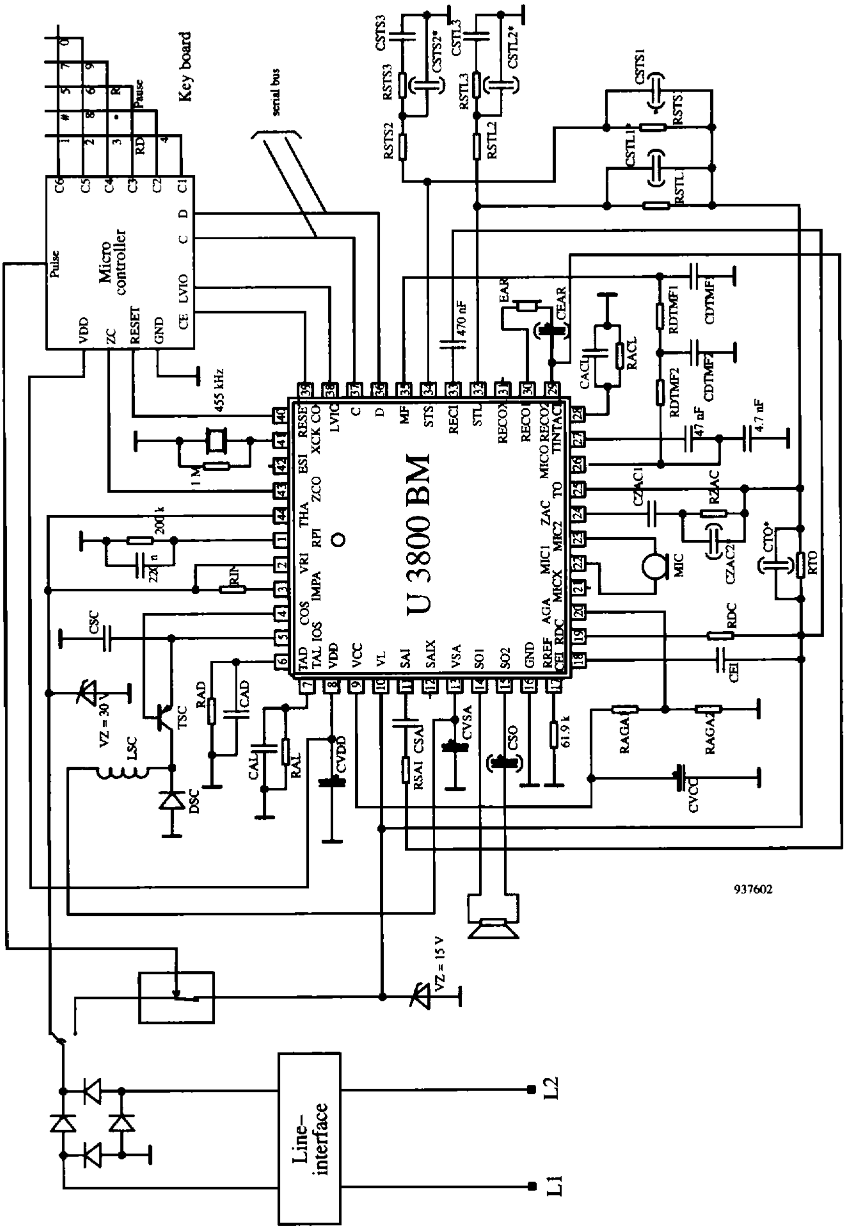
Figure 3. Digital Adjustment of the Analog Parameters by the Serial Bus Microprocessor-interface



..... signal path (analog)

—— control path (digital)

Figure 4. Application for Feature Phone



Typical value of external components

Components	Min	Typ	Max
RIN	0.3 MΩ	1.0 MΩ	1.5 MΩ
CSC		0.1 µF	
TSC		2N5401A	
LSC		1 mH	
DSC		SD103A	
RAD		100 kΩ	
CAD		470 nF	
CAL		470 nF	
RAL		68 kΩ	82 kΩ
CVDD		470 µF	
RSAI		20 kΩ	
CSAI		0.1 µF	
CVSA		220 µF	
CSO		47 µF	
CVCC		100 µF	
RAGA1		100 kΩ	
RAGA2		51 kΩ	
CEI		0.47 µF	
RDC		20 kΩ	
RTO		62 Ω	
(CTO		0.33 µF)	
CZAC1		0.47 µF	
RZAC		12 kΩ	

Components	Min	Typ	Max
(CZAC2		470 pF)	
RDTMF1		240 kΩ	
RDMTF2		330 kΩ	
CDTMF1		4.7 nF	
CDTMF2		220 pF	
CACL		0.47 µF	
RACL		6.8 MΩ	
CEAR		4.7 µF	
Earphone		[illegible]1 kΩ	
Loudspeaker		[illegible]100 Ω	
RSTL1		6.2 kΩ	
(CSTL1		330 pF)	
RSTS1		6.2 kΩ	
(CSTS1		330 pF)	
RSTL2		43 kΩ	
RSTS2		18 kΩ	
RSTL3		100 kΩ	
RSTS3		75 kΩ	
CSTL3		10 nF	
CSTS3		10 nF	
CSTS2		470 pF	
CSTL2		1.2 nF	
X1		CSB455E (Murata)	

Pin Description

Pin	Symbol	Function
1	RPI	Ringing power information. The RC combination smooths the drive current of the loudspeaker amplifier.
2	VRI	Tone-ringer supply voltage. The rectified ringing voltage is delivered to VRI and then converted into the lower supply voltage, VSA, by the converter.
3	IMPA	External adjustment of input ringing impedance. IMPA is adjusted with a resistance between pin 2 and 3. ZIN = RIN/100
4	COS	Control output switching supply. COS drives the base of the external switching transistor of the converter.
5	IOS	Current output of switching supply. This output provides a constant current, which supplies the external part of converter. The magnitude of the current depends on the VRI voltage and the value of resistance RIN.
6	TAD	Adjustment of antidistortion time constant in loudhearing with external RC combination.
7	TAL	Adjustment of antilarsen time constant in loudhearing with external RC combination.
8	VDD	External logic supply.
9	VCC	Power supply for peripherals. VCC and VDD are stabilized supply voltages buffered with external capacitors. They are derived internally from the same voltage source, but are separated from each other by electronic switches. VDD also supplies the digital part of the circuit and is achieved in all three modes: speech mode, ringing mode and operation with external supply. According to the application, peripherial modules are connected to VDD which, in addition to speech mode, must be supplied at least in one of the two other modes. The digital part of circuit and microprocessor must continue operating during line breaks, as they occur during pulse dialing or during flash–signal transmission. Since VDD in this time intervals is fed only from the buffer capacity, the power consumption from VDD must not cause the total voltage dump. VCC supplies no internal parts of circuit and is supplied exclusively in speech mode. External components, which must operate only in this mode, can be connected here. The power is drawn only from the relevant buffer capacitor in the supply intervals during pulse dialing or flash–signal transmission.
10	VL	Line voltage.
11	SAI	Speaker amplifier input. The signal coming from the receive part, e.g. from REC01 or RECO2, is fed in here.
12	SAIX	Speaker amplifier input for special application i.e. answering machine. SAIX is selected via the serial bus. Antidistortion and antilarsen are not effective in this case.
13	VSA	Supply voltage for the loudhearing amplifier. Stabilized supply voltage buffered with an external capacitor for the loudhearing amplifier and zero crossing detector; aditional connection point for an external supply. In speech mode, VSA is supplied by the analog part of the circuit. In this case, the stabilization point is adjusted to the DC line voltage VSA= VL/1.5. In ringing mode, and VSA is supplied directly from the converter. The stabilization point is permanently set. The logic supply, VDD, is fed by a switch from VSA. VSA=5.2V. In the case of an external supply, VSA serves as a point for a current from a power supply. The stabilization point of VSA and supply for the logic correspond to the operation conditions in ringing mode.
14	SO1	Loudspeaker output 1.

Pin Description (continued)

Pin	Symbol	Function
15	SO2	Loudspeaker output 2. Differential output of loudhearing amplifier. The loudspeaker can also be connected asymmetrically to ground or to VSA via a capacitor at one of the two outputs. As a result of this connection there is a bigger output power in reference to low line currents and loudspeakers with low impedance, while the differential connection method results in a higher power output and lower harmonic distortion with medium or high line currents
16	GND	Ground.
17	RREF	External reference resistor. Connection for external reference resistor to generate the reference current. All basic currents of the circuit which must satisfy certain absolute accuracy requirements depend on this current.
18	CEI	Capacitor for electronic inductance. Connection for capacitor of the electronic coil. The circuit contains a first order RC-active low-pass filter. The capacitor is connected externally between CEI and VL.
19	RDC	DC characteristic slope adjustment. A voltage across resistor RDC is proportional to the dc line voltage. This means the current flow through RDC is also proportional to the line voltage. This current drives the supply currents drawn from VL by the most important loads, and therefore defines the total current consumption of the circuit. Adjustment to the slope characteristic is realized by modification of RDC resistance.
20	AGA	Line length adjustment. Reference voltage level for AGA. The potential at this point defines the start threshold for the AGA and the automatic balancing in the receive part (both can be switched off by the serial bus). The potential is normally formed between VCC and ground using a voltage divider. When the line voltage exceeds the threshold level, the AGA or balancing becomes effective.
21	MICX	Asymmetrical microphone input for special applications. The input of the first stage of the transmit amplifier, selected by the serial bus. Anticlipping is not effective at this input.
22	MIC1	Inverting input of microphone amplifier.
23	MIC2	Noninverting input of microphone amplifier.
24	ZAC	AC impedance adjustment. Adjustment of the ac circuit impedance to the line by changing of RZAC.
25	TO	Transmit amplifier output. Transmit amplifier output modulates the current flowing into this output (typically 4.8 mA).
26	MICO	Microphone amplifier output. Output MICO; open-circuit potential = 2*Vbe
27	TIN	Transmit and DTMF input. Input of the second transmit stage.
28	TACL	Adjustment of anticlipping time constant with external RC combination. Anticlipping controls the transmitter input level to prevent clipping with high signal levels. The dynamic range of the transmit peak limiter is controlled by an internal circuit.
29	RECO2	Symmetrical output of receive amplifier.
30	RECO1	Symmetrical output of receive amplifier.
31	RECOX	Receive amplifier output for handsfree and answering machine applications.
32	STL	Long line sidetone network.
33	RECI	Receive amplifier input. It is driven by a signal from VL.
34	STS	Short line sidetone network.

Pin Description (continued)

Pin	Symbol	Function
35	MF	Multifrequency output. Output DTMF signal and confidence tone in pulse–density modulated form. DTMF signal and confidence tone are generated by special generators in the digital part of the circuit. The DTMF signal consists of two weighted and superimposed pulse-density modulated signals, while in the case of confidence tone, a pulse–density modulated signal is superimposed on a high frequency rectangular–pulse signal with pulse duty factor 0.5. The superimposed signals are sent out to MF for further processing.
36	D	Data input of serial bus (see Pin 37). Serial data input from microprocessor for programming the circuit.
37	C	Clock line: 2-wire serial bus. This pin is used together with the data input (pin 36) to transfer data from the microprocessor to the circuit. The last 8 bits, consisting of 5 data bits and 3 address bits, are accepted by the circuit if, during the high phase at pin 37, a positive edge on pin 36 takes place.
38	LVIO	Line voltage information output. State indicator of the line voltage, VL, and the supply voltage, VDD. Indicates to microprocessor whether line voltage VL is present across the circuit and the supply voltage VDD is sufficiently high. If both conditions are fulfilled, LVIO is on high level.
39	CO	Clock output. Output 455 kHz clock pulse for the microprocessor. The 455 kHz clock signal generated in the circuit is amplified and sent to CO. This signal is delivered to the microprocessor as a clock signal. Various internal signals can be output to CO in test mode.
40	RESET	Reset signal for periphery. A reset signal (active low) is generated to clear all registers of the circuit. This can be tapped by peripheral modules, particularly by the microprocessor. This pin enables synchronous resetting of the circuit and peripheral modules.
41	XCK	Clock signal generator. Connector for ceramic resonator (455 kHz). The clock for the digital part of the circuit is generated by a one-pin oscillator, the frequency of which is determined by the ceramic resonator.
42	ESI	Input for external supply information. Input to indicate the operating state external supply. In the case of VSA supplied by a power supply unit, the supply source is connected directly to ESI. ESI is connected to VSA by an external diode in forward mode. The ESI voltage will be one forward voltage higher than the voltage on VSA. This voltage causes the circuit to be in external supply mode.
43	ZCO	Zero crossing output in ringing phase. ZCO operates when the ringer voltage, VRI, and the supply voltage, VSA, are sufficiently high. The output voltage ZCO changes state each time the rectified AC signal of THA crosses the ringing detect turn–on and turn–off thresholds, thus providing information on the frequency of the ring signal. Further analysis of the ring frequency is be done by the microprocessor. Secondly, this pin is used as an input for switching on the test mode. Therefore, a negative voltage of approximately 1 V must be applied to pin 43.
44	THA	Ringing detection threshold adjustment. Input amplitude and frequency identification. The rectified ringing voltage is present at this pin. The circuit evaluates the amplitude of the rectified voltage at THA and the supply voltage VSA (pin 13). If both voltages exceed certain thresholds, the signal present at THA is converted to a rectangular–pulse signal and is sent via pin 43 to the microprocessor. If the frequency is in the required range, the microprocessor initiates transmission of the ringing signal. The start threshold can be raised with a resistor connected in series to pin 44.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
DC calling voltage (pin 2)	VRI	35	V
DC calling current (pin 2)	IR	30	mA
Conversation line voltage (pin 10)	V_L	15 17	V V pulse 20 ms
Conversation line current	I_L	150	mA
Total power dissipation	P_{tot}	1	W
Operating temperature range	T_{amb}	–25 to +55	°C
Storage temperature range	T_{stg}	–55 to +150	°C
Junction temperature	T_j	125	°C

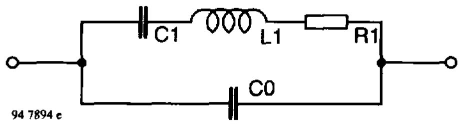
Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	70	K/W

Electrical Characteristics

I_L = 28 mA, T_{amb} = 25°C, f = 1 kHz, R_{DC} = 20 kΩ, all internal registers cleared, unless otherwise specified

Figure 5.



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- 455 kHz ceramic resonator: MURATA or equivalent
- Refer to the tests circuits

Resonance factor Q_m = 3100, L1 = 6.1 mH, C1 = 21 pF, CO = 268.5 pF, R1 = 5.5 Ω (Schematic above)

All resistances are specified at 1%, all capacitances at 2%.

Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
Line voltage	I_L = 15 mA I_L = 28 mA I_L = 60 mA	4.2 6.7 12.8	4.75 7.2 13.45	5.2 7.5 14.1	V	6
VDD, VCC stabilized power supply	I_L = 8 mA, –Idd (ICC) = 0.6 mA I_L = 28 mA, –Idd (ICC) = 2.3 mA	2.5 3.2	2.65 3.45	3.6	V	6
IDD at VDD = 3.5 V Internal operating supply current	S4 on 3		180	210	µA	9
Leakage current				100	nA	
Speed up off threshold VSOFF Speed up on line–current ISON	See fig. 11 I_{Lmax} = 80 mA, V_L = 4 V See fig. 14 I_L decreasing, VDD = 2.8 V	2.45 5.0	2.65 5.9	2.8 7.5	V mA	7
Speed up current	V_L = 4 V	40	70		mA	7

Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
Transmission						
Transmit gain (note 1) on MIC1 / MIC2 on MICX	V_{MIC} = 3 mV_{rms} MIS TX2 TX1 TX0 max. gain 0 1 1 1 min. gain 0 0 0 0 V_{MICX} = 5 mV_{rms} MIS TX2 TX1 TX0 max.gain 1 1 1 1 min. gain 1 0 0 0	 47.0 39.8 42.5 35.3	 48.0 41.0 43.5 36.5	 49.0 42.2 44.5 37.7	 dB dB dB dB	6
Gain adjustment of microphone amplifier	Gain change between two steps (both on MIC1/MIC2 and on MICX)	0.8	1.0	1.2	dB	6
Transmit gain without AGC G_T at 28 mA ΔG_T at I_L = 20 to 28 mA ΔG_T at I_L = 28 to 60 mA	V_{MIC} = 3 mV_{rms}, Bit AGC=1 TX2 TX1 TX0 0 1 1 0 1 1 0 1 1	 42.6 −0.5 −0.5	 44.0 0.0 0.0	 45.5 0.5 0.5	dB	6
Gain change between 28 and 60 mA on MIC1 / MIC2 on MICX	V_{MIC} = 3mV_{rms}: AT1 AT0 (MIS = 0) 0 0 0 1 or V_{MICX} = 5 mV_{rms} 1 0 (MIS = 1) 1 1	 3.6 4.9 6.3 7.7	 4.1 5.35 6.9 8.2	 4.6 5.9 7.4 8.7	dB	6
+ 6 dB delta transmit gain	I_L = 28 mA and 60 mA V_{MIC} = 1.5 mV_{rms}, Bit TX6 = 1	5.4	6.0	6.5	dB	6
Noise at line psophometrically weighted	GT = max. gain V_{MIC} = 0 (MIS = 0) ISQ = 0 V_{MIC} = 0 (MIS = 0) ISQ = 1 V_{MICX} = 0 (MIS = 1) ISQ = 1		 −79 −71	 −75 −68.5 −64	dBmp	6
*Max. gain is without + 6 dB function which is especially devoted for DTMF						
Muted gain on MIC1 / MIC2 on MICX	V_{MIC} = 3 mV_{rms} (MIS = 0) or V_{MIC} = 5 mV_{rms} (MIS = 1) (at max. and min. gain) Bit IM = 1 Bit IT = 1 V_{MIC} = 3 mV_{rms} (MIS = 1) or V_{MIC} = 5 mV_{rms} (MIS = 0)	 65 45 60 60			 dB dB dB dB	6
Microphone input impedance on MIC1/MIC 2 on MICX	 V_{MIC} = 3 mV_{rms} (MIS = 0) V_{MICX} = 5 mV_{rms} (MIS = 1)	 70 35	 110 55		 kΩ kΩ	6
CMRR common mode rejection ratio	G_T = at maximum gain		65		dB	6
Voltage step on pin 26 when going from transmission to mute mode Bit IM from 0 to 1	I_L =28 mA and 60 mA V_{MIC} = 0 (MIS = 0) or V_{MICX} = 0 (MIS = 1) At maximum gain	−110		+110	mV	6
Dynamic limiter (anticlipping) CACL = 470 nF, RACL = 6.8 MΩ operational only on MIC1/MIC2						
Output voltage swing (peak to peak value)	TX2 TX1 TX0 1 1 1 V_{MIC} = 4 mV_{rms} + 10 dB	3.5	3.95	4.4	V_{pp}	6
Delta output voltage swing	TX2 TX1 TX0 0 0 0 V_{MIC} = 9 mV_{rms} + 10 dB	−200	0	200	mV_{pp}	6
Delta output voltage swing	TX2 TX1 TX0 0 0 0 IL = 60 mA AT1 = AT0 = 1 V_{MIC} = 22 mV_{rms} + 10 dB	−200	0	200	mV_{pp}	6

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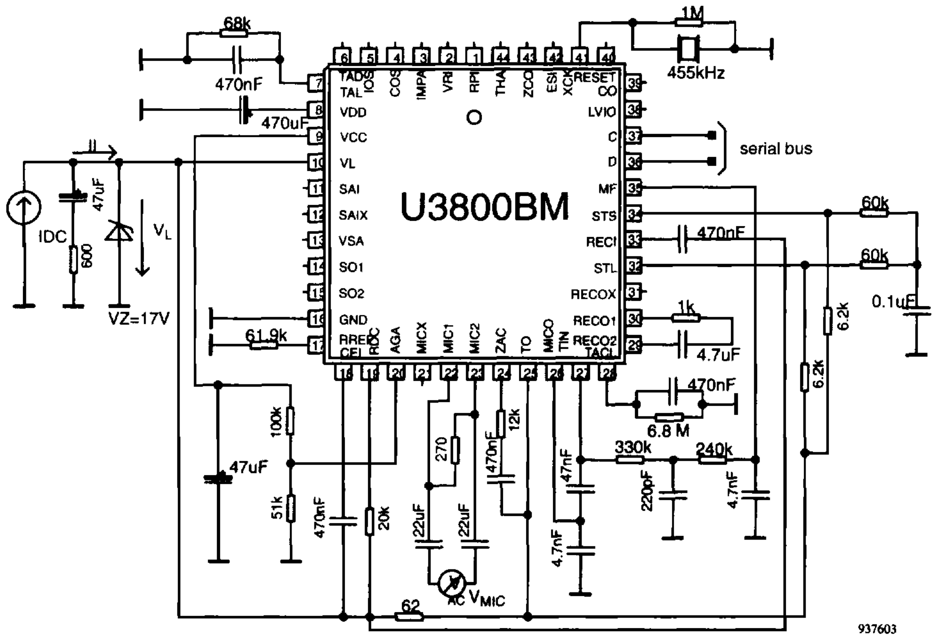
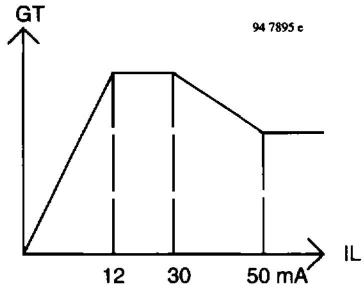
Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
Line distortion (on 600 Ω)	TX6 TX2 TX1 TX0 0 0 0 0 V_{MIC} = 9 mV_{rms} V_{MIC} =9mV_{rms}+26 dB 1 1 1 1 V_{MIC} = 2 mV_{rms} V_{MIC} = 2mV_{rms}+26dB I_L = 60 mA AT0 = AT1 = 1 0 0 0 0 V_{MIC} = 22 mV_{rms} V_{MIC}=22mV_{rms}+26dB			2 3 2 3.5 3 3	% % % % % %	6
Squelch function CAL = 470 nF, RAL = 68 kΩ						
Dynamic range attenuation	(note 2) I_L = 28 mA and 60 mA	8.3	9.3	10.3	dB	6
Squelch inhibition (tested on GT)	$\Delta G_T = G_{T1}(ISQ = 1) - G_{T2}(ISQ = 0)$ G_{T1} (V_{MIC} = 160 µV_{rms}), G_{T2} (V_{MIC} = 3 mV_{rms}) At maximum gain	−0.3	0	0.3	dB	6

Figure 6.



TEST CIRCUIT

- Note 1: transmit gain: $G_T = V_L/V_{MIC}$ on MIC1/MIC2
  $G_T = V_L/V_{MIC}$ on MICX with the above values of RAG1 and RAG2
- Note 2: Squelch dynamic range: $\Delta G_T = G_{T0} - G_{T1}$
  G_{T0} measured at $V_{MIC} = 1\ mV_{rms}$
  G_{T1} measured at $V_{MIC} = 160\ \mu V_{rms}$



Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
Receive						
G_R receiving gain $G_R = V_R^*/V_L$ (for normal output)	$V_{GEN} = 0.3\ V_{rms}$ RX2 RX1 RX0 maximum gain 1 1 1 minimum gain 0 0 0	 3.5 −3.7	 4.5 −2.5	 5.5 −1.3	 dB dB	 7
$\Delta G_R = V_R/V_{E3}$	$V_{GEN} = 0.3\ V_{rms}$	14.0	15.0	16.0	dB	7
Gain adjustment at earphone	I_L = 28 mA and 60 mA Attenuation between two steps (both on REC01/REC02 and on RECOX)	0.8	1.0	1.3	dB	7
Receiving gain without AGC $G_R = V_R/V_L$ G_R at 28 mA ΔG_R at 20 mA < I_L < 28 mA ΔG_R at 28 mA < I_L < 60 mA	$V_{GEN} = 0.3\ V_{rms}$ Bit: AGC = 1 IBAL = 1 Bits RX2 RX1 RX0 1 1 1 1 1 1 1 1 1	 −3 −0.5 −0.5	 −1.5 0 0	 0 0.5 0.5	 dB dB dB	 7
ΔG_R receiving gain betw. 28 and 60 mA on RECO1/RECO2 and on RECOX	$V_{GEN} = 0.3\ V_{rms}$ Bits AR1 AR0 0 0 0 1 1 0 1 1	 3.6 4.9 6.3 7.5	 4.1 5.5 6.9 8.3	 4.6 5.9 7.4 8.7	 dB dB dB dB	7
+ 6 dB delta receiving gain on RECO1/RECO2 and on RECOX	$V_{GEN} = 0.3\ V_{rms}$, I_L = 28mA and 60mA (At maximum and minimum gain) Bit RX6 = 1	5.6	6.1	6.7	dB	7
Muted gain	$V_{GEN} = 0.3\ V_{rms}$ Mute on REC01/REC02 Bit IR=1 Bit IE1 = IE2 = 1 RECOX Bit IR=1	 65 60 36			 dB dB dB	7
Noise at earpiece psophometric weighted	At maximum gain V_{GEN} = 0 V		150	220	µVp	7
Receiving distortion	I_L = 28 mA and 60 mA max gain, RX6 = 1 VR = 5 V_{pp} min. gain, RX6 = 0 VR = 2 V_{pp}		1	3	%	7
Receiver output impedance on RECO1/RECO2 (pins 29−30)	$V_R = 50\ mV_{rms}$,	40	65	85	Ω	7
Receiver output impedance on RECOX (pin 31)	$V_{RECOX} = 50\ mV_{rms}$	950	1150	1350	Ω	7
Receiver output offset (pin 29 − 30)	I_L = 28 mA and 60 mA Maximum gainRX6 = 1	−800		+600	mV	7
Automatic sidetone balancing (V_R^*/V_{MIC})	At maximum gain $V_{MIC} = 4\ mV_{rms}$ I_L = 28 mA I_L = 60 mA		 24 16		 dB dB	6

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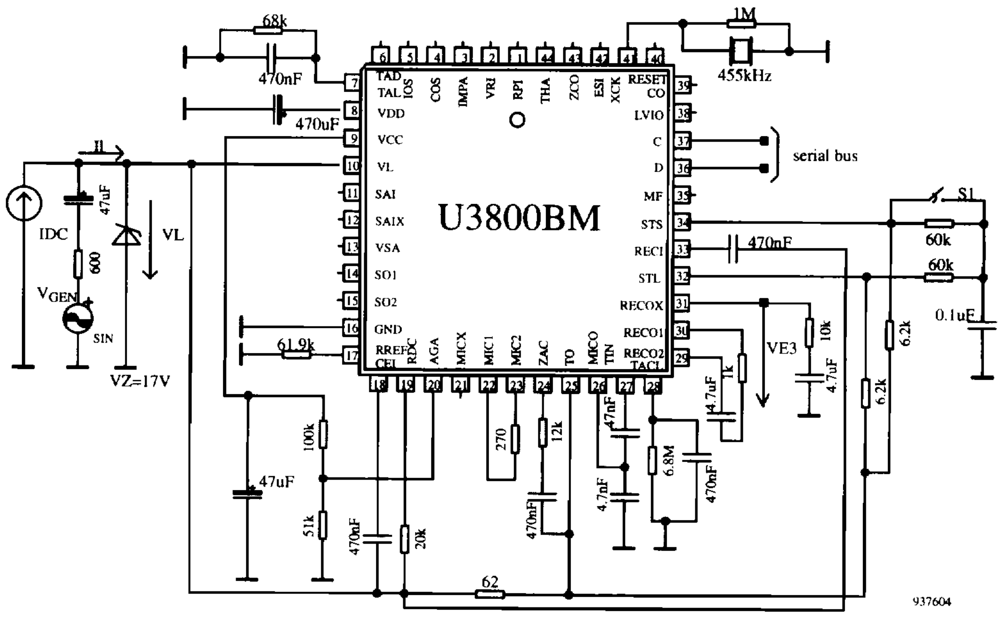
Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
Digital balanced sidetone tested on receiving gain V_R/V_L	V_{GEN} = 0.3 V_{rms} maximum gain close switch S1 Bit IBAL = 1 Bits BAL2 BAL1 BAL0					
	0 0 0	18.0	19.0	20.0	dB	7
	0 0 1	16.9	17.9	18.9	dB	
	0 1 0	15.5	16.5	17.5	dB	
	0 1 1		14.5		dB	
	1 0 1		12.3		dB	
	1 1 0		9.2		dB	
	1 1 1	4.2	5.7	7.2	dB	
Confidence level attenuation	V_{MIC} = 2 mV_{rms}Bit I_R = 1	60			dB	6
Confidence level gain V_R/V_{MIC}	V_{MIC} = 2 m$V_{rms}I_R$ = 1EC = 1	19.5	22.0	23.5	dB	6
Z line match. impedance	V_{GEN} = 0.3 $V_{rms}I_L$ = 28 and 60 mA	520	570	620	Ω	7

* VR = VRECO1 – VRECO2

Figure 7.

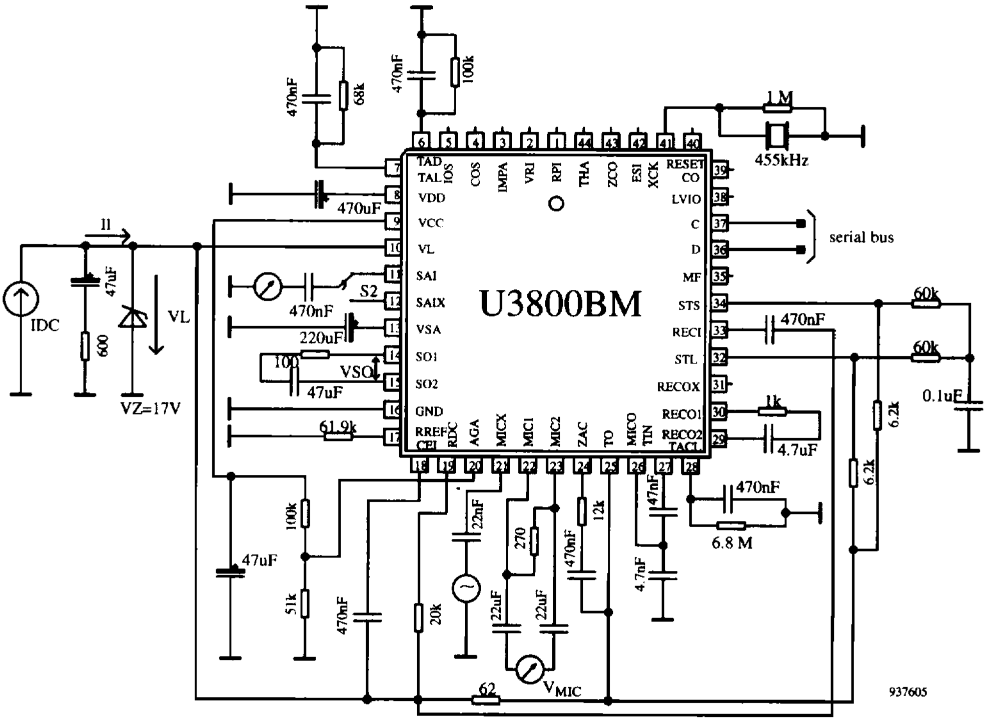


Test circuit

Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
Speaker amplifier						
VSA shunt regulator power supply (pin 13) in transmission mode	Speaker amplifier without signal EA = 1 IL = 28 mA IL = 60 mA	 4.0 7.85	 4.3 8.3	 4.6 8.7	 V V	8
Loudhearing gain (note3) from SAI/SAIX to SO1, SO2	$GSA1 = \frac{VSO1 - VSO2}{VSAI}$ EA = 1 $GSA2 = \frac{VSO1 - VSO2}{VSAIX}$ Bits NEA2 NEA1 NEA0 VSAI = VSAIX 1 1 1 VSAI = 3.5 mV_{rms} 0 0 0 VSAI = 88 mV_{rms}	 33 5	 34 6	 35 7	 dB dB	8
Loudhearing gain between 28 and 60 mA GSA1 and GSA2 (note 3)	EA = 1	−0.5	0	0.5	dB	8
Gain adjustment of speaker amplifier	EA = 1 gain change between two steps	3.8	4.0	4.2	dB	8
Distortion (measured on 100 Ω load)	EA = 1 Bits NEA2 NEA1 NEA0 VSAI 1 1 1 VSAI = 12 mV_{rms} VSAI = 30 mV_{rms} 0 0 0 VSAI = 250 mV_{rms} Bits EA = 1 I_L = 60 mA NEA2 NEA1 NEA0 1 1 1 VSAI = 80 mV_{rms} 0 0 0 VSAI = 250 mV_{rms}			 2.0 4.0 1.5 2.0 2.0	 % % % % %	8
Input impedance SAI SAIX	EA = 1	4 4	7 7	10 10	kΩ	8
Confidence gain in loudhearing	V_{MIC} = 4 mV $\frac{VSO}{V_{MIC}}$ EA = 1 EC = 1	36		40	dB	8
Loudhearing input cross talk attenuation	NEA = 7 EA = 1 VSAI = 12 mV_{rms} LIS = 1 VSAIX = 12 mV_{rms} LIS = 0	 50 45			 dB dB	8
Output power (Note 4, 6)	EA = 1 I_L = 20 mA 100 Ω load EA = 1 I_L = 28 mA 50 Ω load 100 Ω load EA = 1 I_L = 60 mA 50 Ω load 100 Ω load	3.0 8.0	4.5 7 12 100 150		mW mW mW mW mW	8
Output offset (pin 14 − 15)	LIS = 0, 1 EA = 1 max. and min. gain	−200		+200	mV	8
Leakage current (pin 6)	EA = 1			140	nA	8
Offset (pin 7)	RAL = 68 kΩ I_L = 28 mA and 60 mA EA = 1			140	mV	6
Antilarsen system	CAL = 470 nF, RAL = 68 kΩ					
Dynamic range attenuation	(note 5) IL = 28 mA and 60 mA EA = 1 VSAI = 6 mV_{rms} Bit ISQ = 0 BIT ISQ = 1	 5.5 15.0	 6.0 16.3	 6.5 17.5	 dB dB	8

5

Figure 8.



Test circuit

- Note 3: GSA1 measured with S2 on 11
  GSA2 measured with S2 on 12
  and Bit LIS = 1
- Note 4: With 50 Ω single ended load, it is possible, at low line current, to have power 6 dB higher than with 50 Ω differential load. Un this case antidistortion function is not completely effective.
- Note 5: Antilarsen dynamic range:
  $\Delta GLS = GLSA - GLSB$
  GLSA measured at $V_{MIC} = 160\ \mu V_{rms}$
  GLSB measured at $V_{MIC} = 1\ mV_{rms}$
- Note 6: The available output current of the speaker amplifier can be increased by reduction of the quiescent current of the receiver output stage (bits IE1, IE2, see "contents of internal registers").

DTMF Dialing

The output pin MF provides the multifrequency signal to be transmitted on line. This signal is the result of the sum of two frequency pulse modulations and requires an external filter to compose a dual sine wave. The frequencies are chosen in a low group and a high group.

The circuit conforms to the T/CS 46–02 CEPT recommendation concerning DTMF option 1 (−9/−11 dBm) and option 2 (−6/−8 dBm) transmit level 5 (example: in fig. 6, option 2 can be fulfilled with 3.5 dB pre–emphasis and 1.5 Vpp low frequency level pin 35).

Two different low levels (with 3 dB difference) and two different pre–emphasis (2.5 and 3.5 dB) can be chosen through the serial bus.

Melody – Confidence Tone

Melody/confidence tone frequencies are given in table 2.

In the state SIN1 = 1, SIN0 = 0, the IC delivers a single pulse density modulated frequency at pin MF (the same behavior as DTMF), denoted as a confidence tone. The confidence tone is sent either to the line or on the earpiece.In the state SIN1 = 0, SIN0 = 1, a square wave is sent to the loudhearing input for ringing melodies.

Table 1 : Frequency Tolerance of the Output Tones for DTMF Signalling Tone Output frequency when using 455 kHz

Standard Frequency Hz	Tone Output Frequency Hz	Frequency Deviation %	Frequency Deviation Hz
Low Group			
697	697.85	0.12	+0.85
770	771.18	0.15	+1.18
852	852.06	0.01	+0.06
941	940.08	–0.10	–0.92
High Group			
1209	1210.1	0.09	+1.1
1336	1338.2	0.17	+2.2
1477	1477.3	0.02	+0.3
1633	1636.7	0.22	+3.7

Note: Frequency can be directly measured on CO when S3 is closed (Fig. 9)

5

AMF	SIN0	SIN1	CO
1	1	1	DTMF : HF
0	1	1	DTMF : LF
0	1	0	MELODY
0	0	1	CONFIDENCE TONE

	1209	1336	1477	1633
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	*	0	#	D

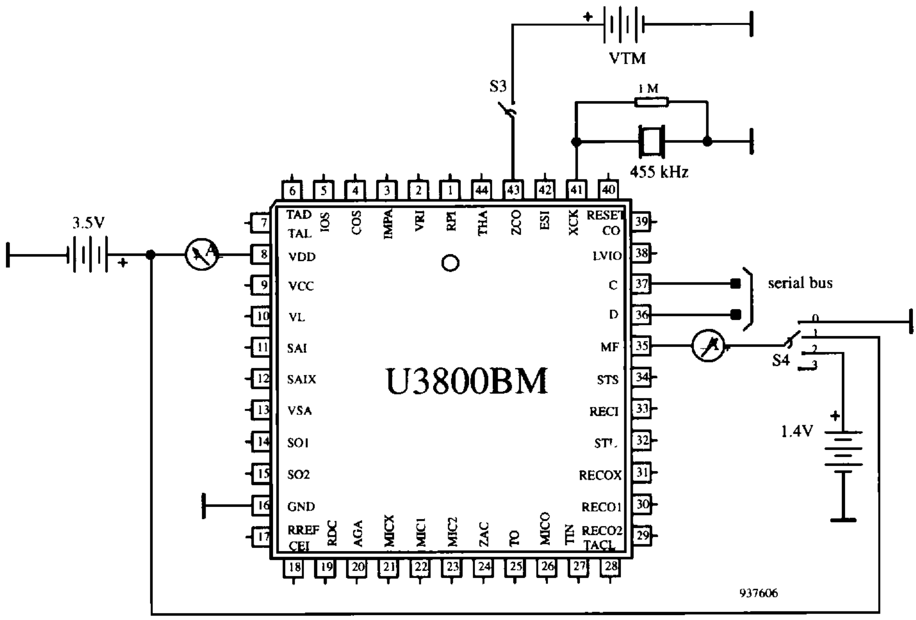
Standard Frequency Hz	Tone Output Frequency Hz	Frequency Deviation ‰
440	440.04	0.09
466.16	466.19	0.06
493.88	493.49	−0.78
523.25	522.99	−0.50
554.36	554.88	0.92
587.33	587.86	0.89
622.25	621.58	−1.07
659.25	659.42	0.26
698.46	697.85	−0.87
740	741.04	1.41
784	784.48	0.62
830	830.29	−0.37
880	878.38	−1.84
932.3	932.38	0.08
987.77	989.13	1.38
1046.5	1048.39	1.80
1108.73	1109.76	0.93
1174.66	1172.68	−1.69
1244.5	1243.17	−1.07
1318.5	1315.03	−2.63
1396.9	1395.71	−0.86
1480	1477.27	−1.84
1568	1568.97	0.62
1661.2	1660.58	−0.37
1760	1763.57	2.03
1864.65	1864.75	0.06
1975.5	1978.26	1.40
2093	2087.16	−2.79
2217.46	2208.74	−3.93
2349.3	2345.36	−1.68

Table 2 : Frequency Tolerance of the Output Tone
Tone Output Frequency when using 455 kHz

Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
DTMF Generation (specified pin MF)						
Tone frequency accuracy	See table 1					
Low group tone level without attenuation	Note 7 S3 closed BFOA (Pre-emphasis A) BFOB (Pre-emphasis B)	1.35 1.25	1.50 1.40	1.65 1.55	V V	9
High group tone level without attenuation	Note 7 S3 closed HFOA (Pre-emphasis A) HFOB (Pre-emphasis B)	1.80 1.90	2.00 2.10	2.20 2.35	V V	9
Pre-emphasis A without attenuation	Note 7 S3 closed PROA	2.04	2.54	3.04	dB	9
Pre-emphasis B without attenuation	Note 7 S3 closed PROB	3.02	3.52	4.02	dB	9
Low group tone level with attenuation	Note 7 S3 closed BF1A (Pre-emphasis A) BF1B (Pre-emphasis B)	0.95 0.90	1.05 1.00	1.15 1.10	V V	9
High group tone level with attenuation	Note 7 S3 closed HF1A (Pre-emphasis A) HF1B (Pre-emphasis B)	1.25 1.35	1.40 1.50	1.55 1.65	V V	9
Pre-emphasis A with attenuation	Note 7 S3 closed PR1A	2.04	2.54	3.04	dB	9
Pre−emphasis B with attenuation	Note 7 S3 closed PR1B	3.02	3.52	4.02	dB	9

Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
Leakage	S4 = 2 Bits SIN1 SIN0 S3 closed 0 0	– 100		100	nA	9
Distortion at line	IL = 28 mA M = 8 Key = «3» TX6 = 1 IM = 1		1	3	%	6
Low group tone level at line	IL = 28 mA and 60 mA M = 8 Key = «3» TX6 = 1 IM = 1	– 10	– 8	– 6	dBm	6
Melody generation						
Tone frequency accuracy	see table 2					
Confidence tone level	Note: 7 CTL	2.10	2.33	2.60	V	9

Figure 9.



Test circuit

	Internal Registers Set by Serial Bus				Internal Signal Set by Clock Count			
S4 (Fig. 9)	AMF	SIN1	SIN0	M4	FB	FH	F227	I measured
0	0	1	1	0	1	0	X	I1
0	0	1	1	0	0	1	X	I2
0	0	1	1	1	0	1	X	I3
0	0	1	0	0	0	X	1	I4
0	1	1	1	X	0	0	1	I5
1	0	1	1	1	0	1	X	I6
1	0	1	1	0	1	0	X	I7
1	0	1	1	1	1	0	X	I8
1	0	1	0	X	1	X	0	I9
1	1	1	1	X	1	1	0	I10

X: either 1 or 0

Note 7: DTMF calculations

BF level without attenuation with pre-emphasis A:
$$BFOA = \left(\frac{I1}{I1 + I7} + \frac{I6}{I6 + I2}\right)\frac{VDD}{2}$$

BF level without attenuation with pre-emphasis B:
$$BFOB = \left(\frac{I1}{I1 + I8} + \frac{I6}{I6 + I3}\right)\frac{VDD}{2}$$

HF level without attenuation with pre-emphasis A:
$$HFOA = \left(\frac{I2}{I2 + I6} + \frac{I7}{I7 + I1}\right)\frac{VDD}{2}$$

HF level without attenuation with pre-emphasis B:
$$HFOB = \left(\frac{I3}{I3 + I6} + \frac{I8}{I8 + I1}\right)\frac{VDD}{2}$$

Pre-emphasis A without attenuation:
$$PROA = 20 \log \left(\frac{HFOA}{BFOA}\right)$$

Pre-emphasis B without attenuation:
$$PROB = 20 \log \left(\frac{HFOB}{BFOB}\right)$$

BF level with attenuation with pre-emphasis A:
$$BF1A = \left(\frac{I1}{I1 + I7 + I10} + \frac{I6}{I6 + I2 + I5}\right)\frac{VDD}{2}$$

BF level with attenuation with pre-emphasis B:
$$BF1B = \left(\frac{I1}{I1 + I8 + I10} + \frac{I6}{I6 + I3 + I5}\right)\frac{VDD}{2}$$

HF level with attenuation with pre-emphasis A:
$$HF1A = \left(\frac{I2}{I2 + I6 + I10} + \frac{I7}{I7 + I1 + I5}\right)\frac{VDD}{2}$$

HF level with attenuation with pre-emphasis B:
$$HF1B = \left(\frac{I3}{I3 + I6 + I10} + \frac{I8}{I8 + I1 + I5}\right)\frac{VDD}{2}$$

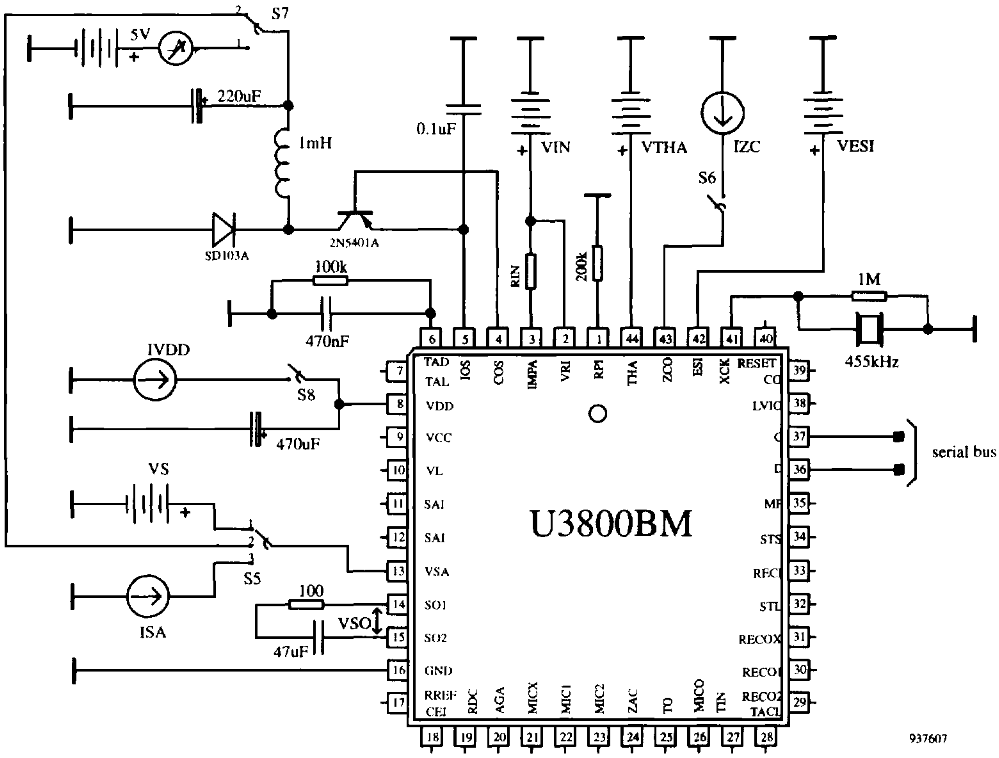
Pre-emphasis A without attenuation:
$$PR1A = 20 \log \left(\frac{HF1A}{BF1A}\right)$$

Pre-emphasis B without attenuation:
$$PR1B = 20 \log \left(\frac{HF1B}{BF1B}\right)$$

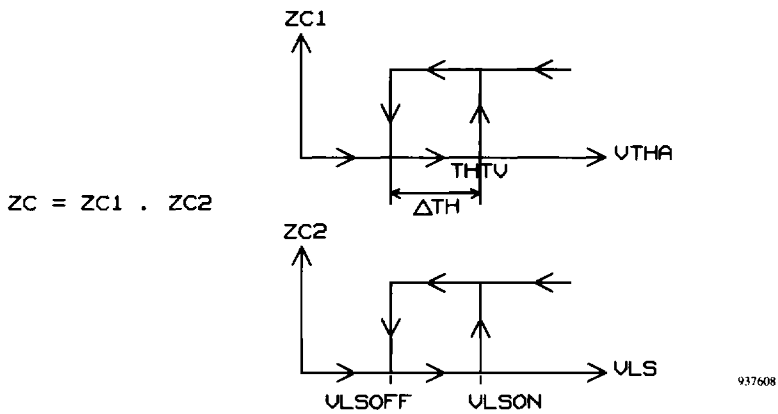
Confidence tone level:
$$CTL = \left(\frac{I1}{I1 + I9} + \frac{I6}{I6 + I4}\right)\frac{VDD}{2}$$

Parameters	Test Conditions	Min	Typ	Max	Unit	Fig
Ringer						
THA threshold voltage THTV	V_S = 5 V S5 on 1	8.30	8.75	9.20	V	10
THA hysteresis ΔTH	V_S = 5 V S5 on 1	435	465	495	mV	10
VSA threshold voltage VSAON (ring detector enabled)	VTHA = 12 V S5 on 1	3.0	3.2	3.4	V	10
VSA threshold voltage VSAOFF (ring detector disabled)	VTHA = 12 V S5 on 1	2.45	2.5	2.65	V	10
Switching supply output current	VS = 5 V VIN = 30 V S7 on 1 S5 on 1 RIN = 300 kΩ	33	37		mA	10
Input impedance VIN/IIN	S5 on 1 VS = 5 V S7 on 1 Off state VIN = 5 V RIN = 300 kΩ On state VIN = 30 V RIN = 300 kΩ On state VIN = 30 V RIN = 1500 kΩ	 50.0 2.78 13.4	 2.90 14.1	 3.05 15.0	 kΩ kΩ kΩ	10
RPI ringing power information	RIN = 300 kΩ S7 on 2 S5 on 2 VIN = 30 V VESI = 0 V S5 on 1 VIN = 0 V VESI = 5 V	 1.48 1.57	 1.55 1.61	 1.64 1.64	 V V	10
VSA/VDD switch off VSAOFF1 (measured on VSA)	S8 closed S5 on 1 IVDD = – 1 mA	5.55	5.8	6.0	V	10
VSA shunt regulator VSAL VSAH	 S5 on 3 ISA = 2 mA ISA = 45 mA	 4.75 5.0	 5.0 5.3	 5.15 5.7	 V V	10
Difference between max. VSA–voltage and cut–off–voltage	VSADIFF = VSAOFF1 – VSAH	250	500		mV	10
ZCO Zero crossing information	VS = 5 V S5 on 1 S6 closed IZCO = 100 μA VTHA = 7.5 V IZCO = –100 μA VTHA = 12.0 V	 4.4		 0.5	 V V	10
Ringer output power (on 100 Ω load)	VIN = 30 V RIN = 300 kΩ S7 on 2 S5 on 2 SIN1 SIN0 LIS EA 0 1 1 1 NEA – maximum gain	70	105	130	mW	10
Extra ringing attenuation	VIN = 30 V RIN = 300 kΩ S7 on 2 S5 on 2 SIN1 SIN0 LIS AMF EA 0 1 1 1 1 NEA – maximum gain	– 12.8	– 12.2	– 11.6	dB	10

Figure 10.



Test circuit



Electrical Characteristics of Logical Part

f_{xck} = 455 kHz VDD = 3.5 V

Parameter		Min.	Typ.	Max.	Unit
INPUTS : C, D					
Low-voltage input Vil				0.7	V
High-voltage input Vih		2.8			V
Input leakage current Ii (0 < VI < VDD)		– 1		1	µA
Output: RESET, CO, LVIO					
Low-voltage output (Iol = 100 mA) Vol				0.35	V
High-voltage output (Ioh = – 100 mA) Voh		3.1			V
CLOCK: CO (fig. 15)					
Using reference ceramic resonator					
period:	t_{cyc}	2.19	2.20	2.21	µs
High pulse width:	t_{wch}	1.10		1.45	µs
SERIAL BUS (fig. 19)					
Data set–up time	t_{sud}	0.1			µs
Data hold time	t_{hd}	0			µs
Clock low time	t_{cl}	2			µs
Clock high time	t_{ch}	2			µs
Hold time before transfer condition	t_{eon}	0.1			µs
Data low pulse on transfer condition	t_{eh}	0.2			µs
Data high pulse on transfer condition	t_{eoff}	0.2			µs
RESET TIMING (fig. 11, 12, 13)					
Clock start–up time	t_{on}		3	5	ms
Clock inhibition time	t_{off}	35.2		75	µs
Reset time (without t_{on})	t_r	30.0	31.6	32	ms

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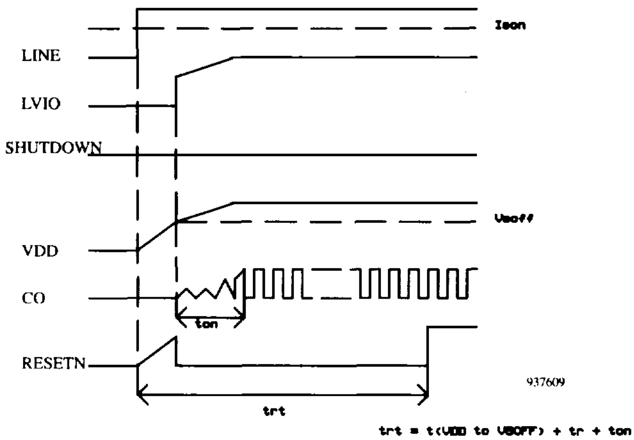
Power-on-reset And Reset Pin

The system (U 3800 BM + microcontroller) is woken up by an initial condition:
- line voltage (VL)
- ringer (THA)
- external supply (ESI)

To avoid undefined states of the system when it is powered on, an internal reset clears the internal registers, and maintains pin RESET low during trt.

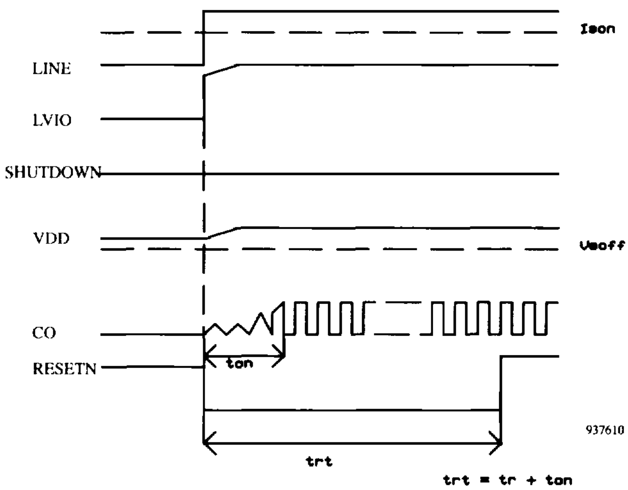
1.) Power–on in speed–up condition (VDD < VSON)

Figure 11.



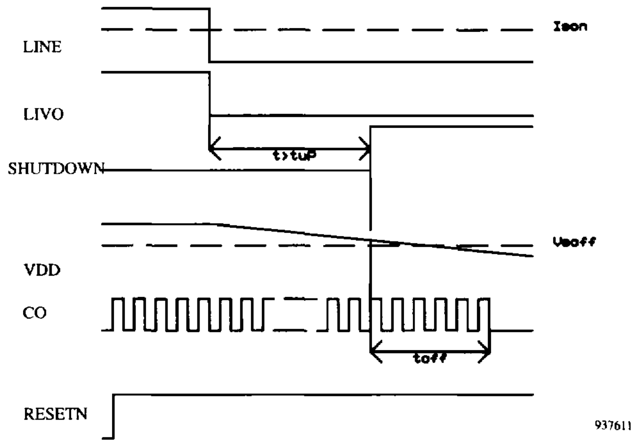
2.) Power–on without speed–up (VDD > VSON)

Figure 12.



3.) Line break

Figure 13.



When the microprocessor detects LIVO low during t > tµP (internal microprocessor timing special for line breaks), it forces high the shutdown bit through the serial bus, thus leading the IC, after t_{off}, to go into standby mode (oscillator stop). Pin RESET remains high.

When the line break is shorter than tµP, nothing appears.

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4.) Line current fall

Figure 14.

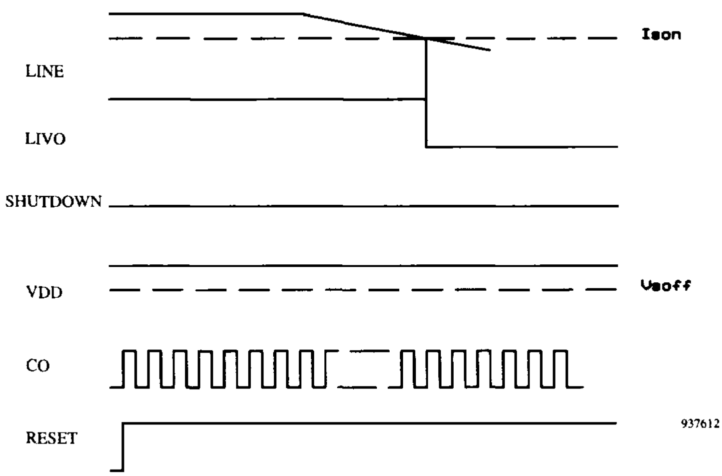
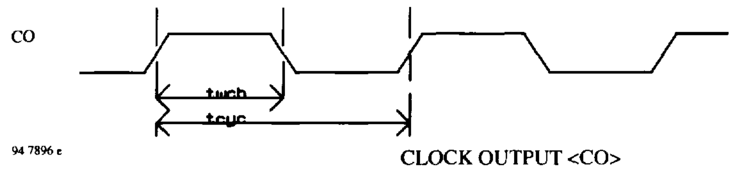


Figure 15.



Serial Bus

The circuit is remoted by an external microcontroller through the serial bus:

The data is an 8-bit word:
B7 – B6 – B5: address of the destination register (0 to 7)
B4 – B0: contents of register

The data line must be stable when the clock is high and data must be serially shifted.

After 8 clock periods, the transfer to the destination register is (internally) generated by a low to high transition of the data line when the clock is high.

Figure 16.

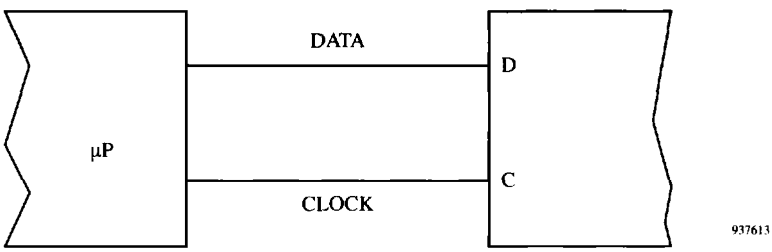


Figure 17.

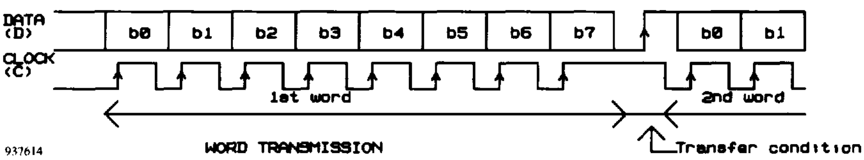


Figure 18.

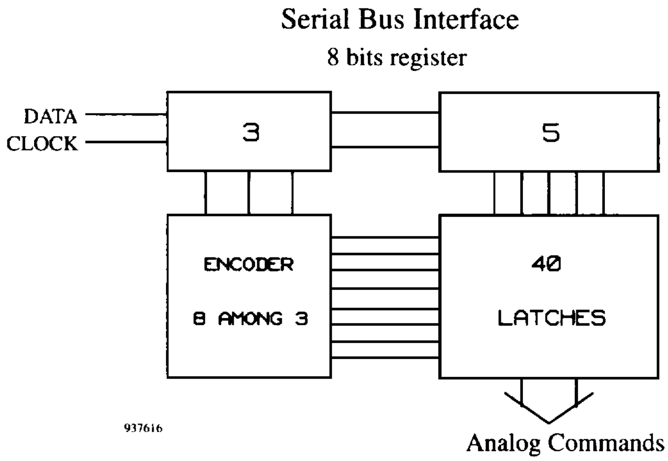
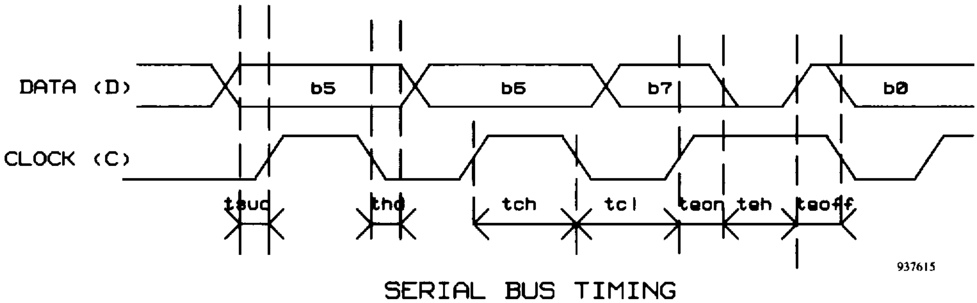


Figure 19.



Content of Internal registers

0: Transmission mode

MIS	TX6	TX2	TX1	TX0	MIS: Microphone input switching TX6: +6dB TX: Transmission gain adjustment

1: Reception mode

LIS	RX6	RX2	RX1	RX0	LIS: Loudhearing input switching RX6: +6dB RX: Reception gain adjustment

2: Loudhearing mode

IAL	EA	NEA2	NEA1	NEA0	IAL: Antilarsen inhibition EA: Loudhearing enable NEA: Loudhearing gain adjustment

3: AGC mode

IAGC	AR1	AR0	AT1	AT0	IAGC: AGC inhibition AT: Transmission AGC adjustment AR: Reception AGC adjustment

4: Sidetone mode

IE2	IBAL	BAL2	BAL1	BAL0	IE2: Reception output amplifier current adjustment IBAL: Inhibition of automatic sidetone balance

BAL	Z
0	1 STS
1	5/6 STS + 1/6 STL
2	2/3 STS + 1/3 STL
3	1/2 STS + 1/2 STL
4	1/2 STS + 1/2 STL
5	1/3 STS + 2/3 STL
6	1/6 STS + 5/6 STL
7	1 STL

5: Internal inhibitions

IR	EC	IT	IM	IE1	IR: Reception inhibition EC: Confidence enable IT: Transmit inhibition IM: Microphone inhibition IE1: Reception output amplifier current adjustment

IE1	IE2	IREC	
0	0	3 mA	
0	1	2 mA	
1	0	1 mA	
1	1	0 mA	Earpiece inhibition

6: Melody / DTMF choice

M4	M3	M2	M1	M0	

Table 3 :

M	Melody or confidence tone output		DTMF mode	
			Key	HF/LF
00	A3	440.0	«1»	2.5 dB
01	A#3	466.2	«4»	"
02	B3	493.5	«7»	"
03	C4	523.0	«*»	"
04	C#4	554.9	«2»	"
05	D4	587.8	«5»	"
06	D#4	621.6	«8»	"
07	E4	659.4	«0»	"
08	F4	697.8	«3»	"
09	F#4	741.0	«6»	"
0A	G4	784.5	«9»	"
0B	G#4	830.3	«#»	"
0C	A4	878.4	«A»	"
0D	A#4	932.4	«B»	"
0E	B4	989.1	«C»	"
0F	C5	1048.4	«D»	"
10	C#	1109.7	«1»	3.5 dB
11	D5	1172.7	«4»	"
12	D#5	1243.2	«7»	"
13	E5	1315.0	«*»	"
14	F5	1395.7	«2»	"
15	F#5	1477.3	«5»	"
16	G5	1569.0	«8»	"
17	G#5	1660.6	«0»	"
18	A5	1763.6	«3»	"
19	A#5	1864.7	«6»	"
1A	B5	1978.3	«9»	"
1B	C6	2087.2	«#»	"
1C	C#6	2208.7	«A»	"
1D	D6	2345.4	«B»	"
1E			«C»	"
1F			«D»	"

7: Control register

AMF	ISQ	SD	SIN1	SIN0	AMF: MF output attenuation −3 dB extra ringing attenuation (12 dB) ISQ: Squelch inhibition SD: Shutdown SIN: Generator mode 0: OFF 1: Melody (Ringer) 2: Confidence tone 3: DTMF

Order Information

Package	Type
PLCC 44	U 3800 BM-CL
SSO 44	U 3800 BM-FN

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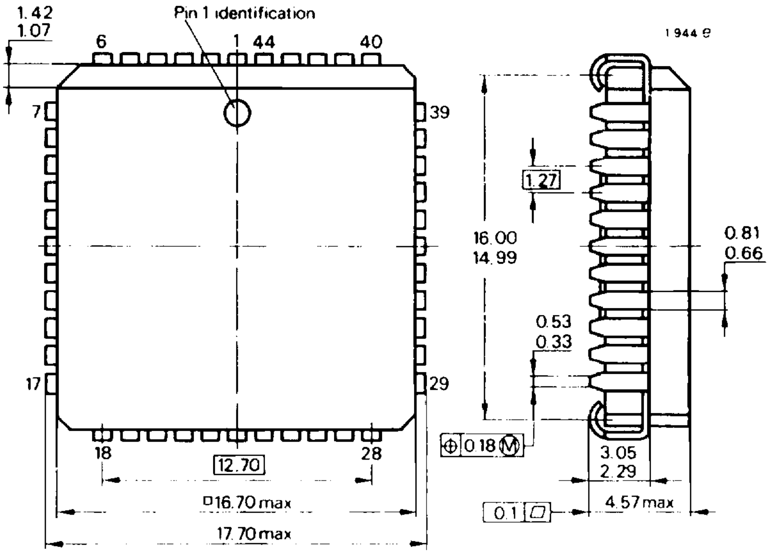
Dimensions in mm

Package PLCC 44



We reserve the right to improve technical design
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