## SILICON STACKED GATE CMOS

## 65,536 WORD x 16 BIT CMOS MASK ROM

### Description

The TC531024P/F is a 1,048,576 bit read only memory organized as 65,536 words by 16 bits.
The TC531024P/F is fabricated using Toshiba's advanced CMOS technology which results in high speed and low power features: access times of 120ns/150ns, an operating current of 40mA at 8.3MHz, and a standby current of 20μA.

The TC531024P/F is packaged in a standard 600mil 40-pin DIP or 525mil 40-pin SOP.

### Features

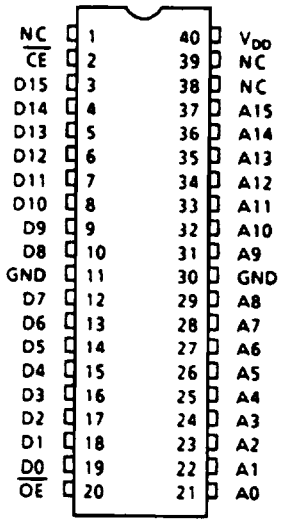
| TC531024P/F | -12 | -15 |
|---|---|---|
| Power Supply | 5V±5% | 5V±10% |
| Access Time (max.) | 120ns | 150ns |
| Operating Current (max.) | 40mA | 35mA |
| Standby Current (max.) | 20μA | 20μA |

- Single 5V power supply
- Fully static operation
- Inputs and outputs TTL compatible
- Three state outputs
- Package
  - TC531024P : DIP40-P-600
  - TC531024F : SOP40-P-525

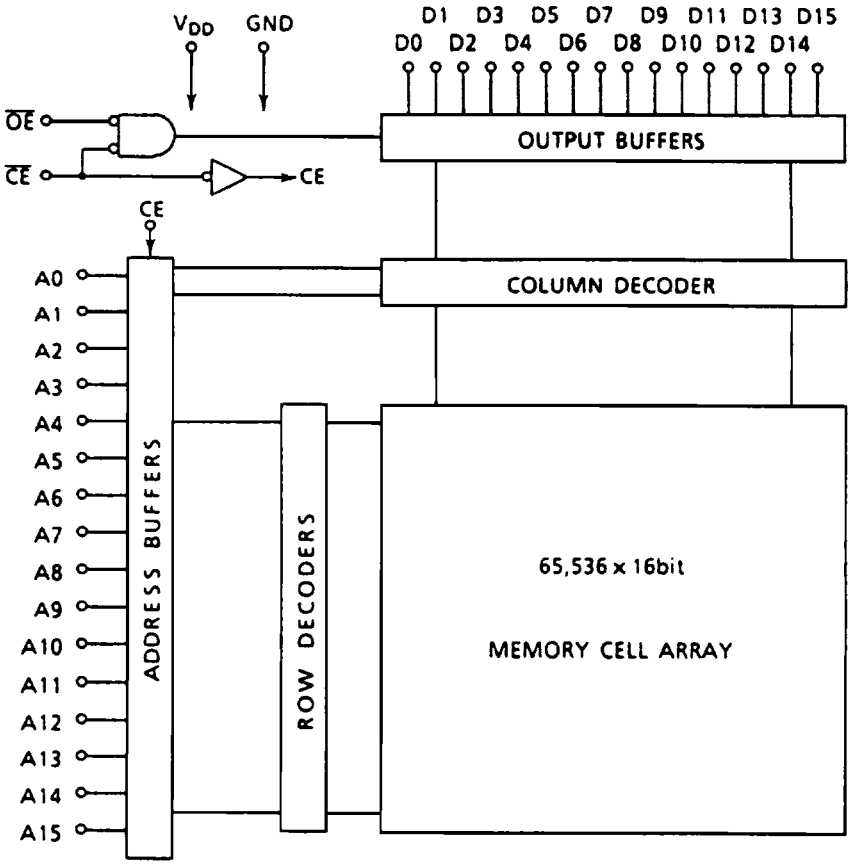
### Pin Names

| | |
|---|---|
| A0 ~ A15 | Address Inputs |
| D0 ~ D15 | Data Outputs |
| $\overline{OE}$ | Output Enable Input |
| $\overline{CE}$ | Chip Enable Input |
| $V_{DD}$ | Power Supply Voltage (+5V) |
| GND | Ground |
| NC | No Connection |

### Pin Connection (Top View)



## Block Diagram




## Operating Mode

| MODE | $\overline{CE}$ | $\overline{OE}$ | A0 ~ 15 | OUTPUTS | POWER |
|---|---|---|---|---|---|
| Read | L | L | Valid | Data Out | Operating |
| Standby | H | * | * | High-Z | Standby |
| Output Deselect | L | H | * | High-Z | Operating |

H = $V_{IH}$, L = $V_{IL}$, * = $V_{IH}$ or $V_{IL}$

## Maximum Ratings

| SYMBOL | ITEM | RATING | UNIT |
|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | -0.5 ~ 7.0 | V |
| $V_{IN}$ | Input Voltage | -0.5 ~ $V_{DD}$ | |
| $V_{OUT}$ | Output Voltage | 0 ~ $V_{DD}$ | |
| $P_D$ | Power Dissipation | 1.0/0.6* | W |
| $T_{STRG}$ | Storage Temperature | -55 ~ 150 | °C |
| $T_{OPR}$ | Operating Temperature | 0 ~ 70 | |
| $T_{SOLDER}$ | Soldering Temperature • Time | 260 • 10 | °C • sec |

* SOP

### DC Recommended Operating Conditions

| SYMBOL | PARAMETER | -12 | | | -15 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| $V_{DD}$ | Power Supply Voltage | 4.75 | 5.00 | 5.25 | 4.50 | 5.00 | 5.50 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | – | $V_{DD}$ + 0.3 | 2.2 | – | $V_{DD}$ + 0.3 | |
| $V_{IL}$ | Input Low Voltage | -0.3 | – | 0.8 | -0.3 | – | 0.8 | |

### DC Characteristics (Ta = 0 ~ 70°C)

| SYMBOL | PARAMETER | TEST CONDITION | | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 0 ~ $V_{DD}$ | | – | ±1.0 | μA |
| $I_{LO}$ | Output Leakage Current | $\overline{CE}$ = $V_{IH}$, $V_{OUT}$ = 0 ~ $V_{DD}$ | | – | ±5.0 | |
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V | | -1.0 | – | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | | 3.2 | – | |
| $I_{DDS1}$ | Standby Current | $\overline{CE}$ = 2.2V | | – | 2 | |
| $I_{DDS2}$ | | $\overline{CE}$ = $V_{DD}$ - 0.2V | | – | 20 | μA |
| $I_{DDO1}$ | Operating Current | $\overline{CE}$ = $V_{IL}$, $V_{IN}$ = $V_{IH}$/$V_{IL}$, $I_{OUT}$ = 0mA | $t_{cycle}$ = 120ns | – | 50 | mA |
| | | | $t_{cycle}$ = 150ns | – | 45 | |
| $I_{DDO2}$ | | $\overline{CE}$ = 0.2V, $V_{IN}$ = $V_{DD}$ - 0.2V/0.2V, $I_{OUT}$ = 0mA | $t_{cycle}$ = 120ns | – | 40 | |
| | | | $t_{cycle}$ = 150ns | – | 35 | |

### AC Characteristics (Ta = 0 ~ 70°C)

| SYMBOL | PARAMETER | -12 | | -15 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | |
| $t_{CYC}$ | Cycle Time | 120 | – | 150 | – | ns |
| $t_{ACC}$ | Address Access Time | – | 120 | – | 150 | |
| $t_{CE}$ | Chip Enable Access Time | – | 120 | – | 150 | |
| $t_{OE}$ | Output Enable Access Time | – | 70 | – | 70 | |
| $t_{CED}$ | Output Disable Time from $\overline{CE}$ | 0 | 60 | 0 | 60 | |
| $t_{OED}$ | Output DisableTime from $\overline{OE}$ | 0 | 60 | 0 | 60 | |
| $t_{OH}$ | Output Hold Time | 5 | – | 5 | – | |

### AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 2.4V/0.6V |
| Input Pulse Rise and Fall Times | 5ns max. |
| Input Timing Measurement Reference Levels | 2.2V/0.8V |
| Output Timing Measurement Reference Levels | 2.0V/0.8V |
| Output Load | 1 TTL Gate and $C_L$ = 100 pF |

### Capacitance* (Ta = 25°C, f = 1MHz)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | – | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | – | 10 | |

*This parameter is periodically sampled and is not 100% tested.

## Timing Waveforms