

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90A67N/F

Single Chip Picture-in-Picture IC (PAL/NTSC)

TC90A67N/F is a Picture-in-Picture (PIP) IC including a PIP controller and a PAL/NTSC decoder function on a chip. TC90A67N/F has an ADC, a video decoder, a vertical filter, a field memory, DACs and so on, so that it is easy to design a PIP application with the least external components.

Features

Video Decoder for the sub-picture

- NTSC, PAL (Europe), M-PAL and N-PAL systems
- Automatic color system identification
- 8-bit ADC for a composite video input
- Y/C separation by built-in digital filters
- ACC, Color killer circuits
- Contrast, Brightness, Tint and Color level controls
- Accessible V-chip signal data via IIC bus

Main-picture timing processing

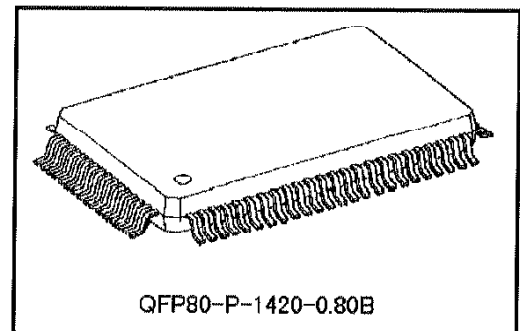
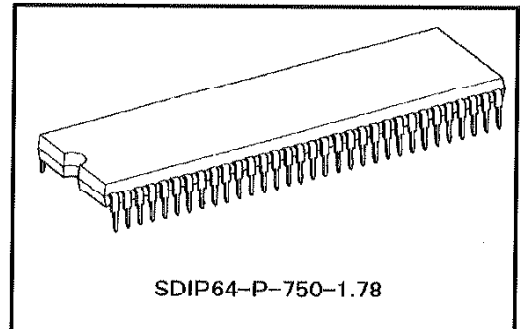
- Internal timing pulses synchronized to the HD/VD pulses from a main picture signal processor

PIP controller

- 525-60Hz, 626-50Hz and mixed are available
- Vertical filter
- Field memory (181kbit)
- PIP mode: Single PIP with 1/9 or 1/16 size, 6 PIPs with 1/36 size
- Flexible PIP position
- 3ch 8-bit DACs for YUV or RGB outputs
- YUV to RGB converter

Others

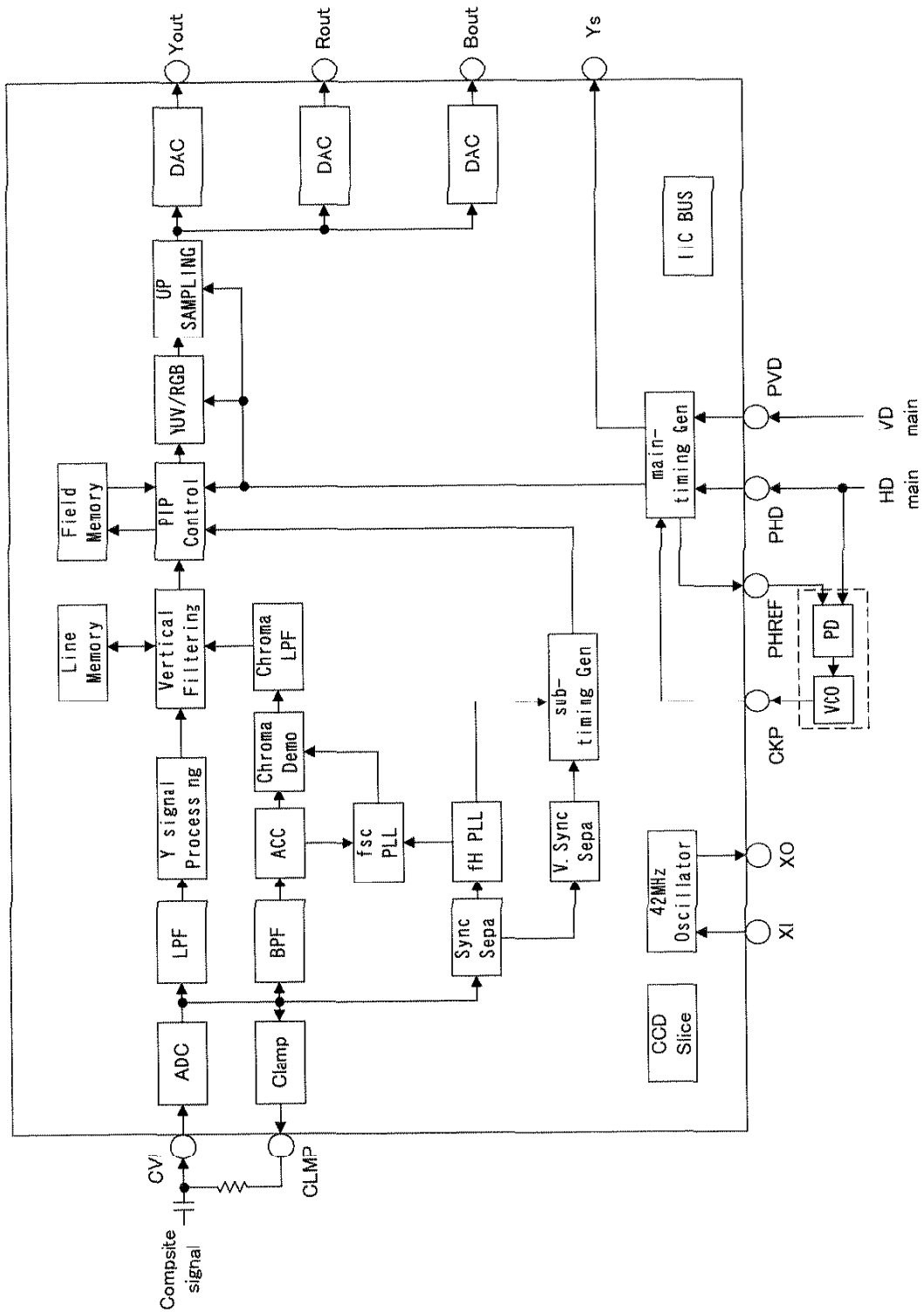
- 42MHz crystal oscillator
- I²C bus control
- Package : SDIP 64, QFP 80
- Power supply : 3.3 V



version1.0

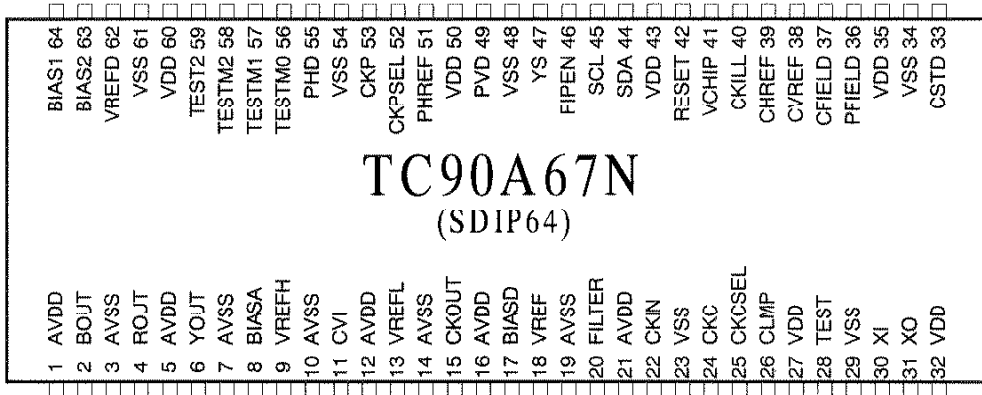
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BLOCK DIAGRAM

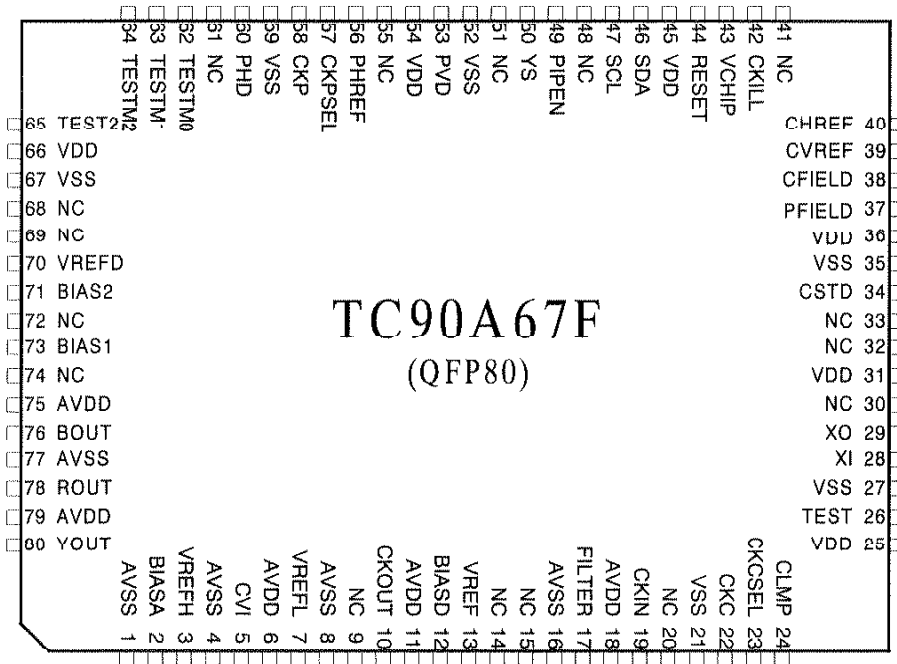


TERMINAL CONECTION DIAGRAM

SDIP64-P-750-1.78



QFP80-P-1420-0.80B



TERMINAL FUNCTION

• SDIP64-P-750-1.78

PIN	NAME	I/O	FUNCTION	CONDITION
1	AVDD	—	Power supply for DAC	
2	BOUT	O	Analog signal output (B-Y or B)	
3	AVSS	—	Ground for DAC	
4	ROUT	O	Analog signal output (R-Y or R)	
5	AVDD	—	Power supply for DAC	
6	YOUT	O	Analog signal output (Y or G)	
7	AVSS	—	Ground for DAC	
8	BIASA	—	ADC bias voltage	
9	VREFH	—	Upper limit reference voltage of ADC	normal : 2.3V
10	AVSS	—	Ground for ADC	
11	CVI	I	Composite video signal input	
12	AVDD	—	Power supply for ADC	
13	VREFL	—	Lower limit reference voltage of ADC	normal : 1.0V
14	AVSS	—	Ground for DAC	
15	CKOUT	O	384fH-clock output	
16	AVDD	O	Power supply for VCO	
17	BIASD	—	DAC bias voltage	
18	VREF	—	Lower limit reference voltage of DAC	normal : 1.8V
19	AVSS	—	Ground for VCO	
20	FILTER	O	VCO filter terminal	
21	AVDD	—	Power supply for DAC	
22	CKIN	I	384fH -clock input	
23	VSS	—	Ground for digital circuit	
24	CKC	I	Clock input (sub-picture)	
25	CKCSEL	I	Internal / external 384fH VCO select	L : internal , H : external
26	CLMP	O	Clamp level output	
27	VDD	—	Power supply for digital circuit	
28	TEST	I	Test pin	normal : H
29	VSS	—	Ground for crystal oscillator	
30	XI	I	42MHz crystal oscillator input	
31	XO	O	42MHz crystal oscillator output	
32	VDD	—	Power supply for crystal oscillator	
33	CSTD	O	Internal signal output	
34	VSS	—	Ground for DRAM	
35	VDD	—	Power supply for DRAM	
36	PFIELD	O	Field odd/even output(main picture)	H:even ,L:odd
37	CFIELD	O	Field odd/even output(sub picture)	H:even ,L:odd
38	CVREF	O	Vertical sync. output(sub picture)	
39	CHREF	O	Horizontal sync. output(sub picture)	
40	CKILL	O	Color killer detection output(sub picture)	H:color killer ON,L:OFF
41	VCHIP	I	23rd-line ID output	23rd -line :H
42	RESET	I	Reset input	L : reset
43	VDD	—	Power supply for digital circuit	
44	SDA	I/O	I ² C BUS data input , data and acknowledge output	
45	SCL	I	I ² C BUS clock input	

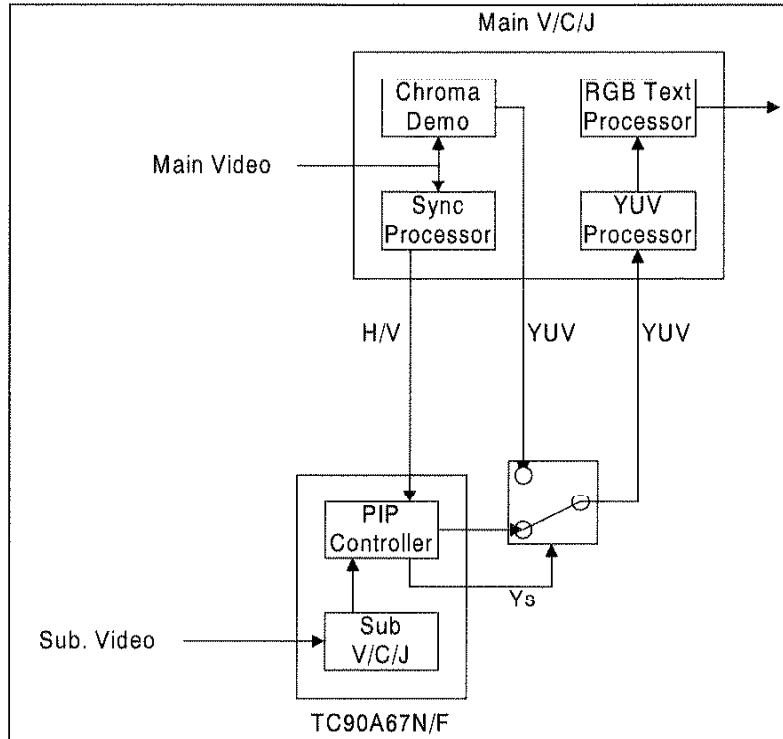
46	PIPEN	I	PIP enable	normal : H
47	YS	O	Main , sub-picture switching pulse	sub-picture : high
48	VSS	—	Ground for digital circuit	
49	PVD	I	Vertical sync. input (main picture)	normal : negative
50	VDD	—	Power supply for digital circuit	
51	PHREF	O	Horizontal sync. output(main picture)	
52	CKPSEL	I	CKP frequency selection	L:24MHz,H:48MHz
53	CKP	I	Clock input (main picture)	
54	VSS	—	Ground for digital circuit	
55	PHD	I	Horizontal sync. input (main picture)	normal : positive
56	TESTM0	I	Test pin	normal : H
57	TESTM1	I	Test pin	normal : H
58	TESTM2	I	Test pin	normal : H
59	TEST2	I	Test pin	normal : H
60	VDD	—	Power supply for digital circuit	
61	VSS	—	Ground for digital circuit	
62	VREFD	I	Lower limit reference voltage of DAC	normal : 1.8V
63	BIAS2	—	DAC bias reference voltage	
64	BIAS1	—	DAC bias reference voltage	

· QFP80-P-1420-0.80B

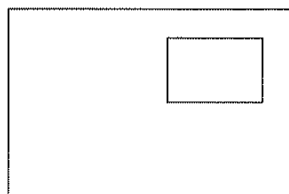
PIN	NAME	I/O	FUNCTION	CONDITION
1	AVSS	—	Ground for DAC	
2	BIASA	—	ADC bias voltage	
3	VREFH	—	Upper limit reference voltage of ADC	normal : 2.3V
4	AVSS	—	Ground for ADC	
5	CVI	I	Composite video signal input	
6	AVDD	—	Power supply for ADC	
7	VREFL	—	Lower limit reference voltage of ADC	normal : 1.0V
8	AVSS	—	Ground for DAC	
9	NC	—		
10	CKOUT	O	384fH-clock output	
11	AVDD	O	Power supply for VCO	
12	BIASD	—	DAC bias voltage	
13	VREF	—	Lower limit reference voltage of DAC	normal : 1.8V
14	NC	—		
15	NC	—		
16	AVSS	—	Ground for VCO	
17	FILTER	O	VCO filter terminal	
18	AVDD	—	Power supply for DAC	
19	CKIN	I	384fH -clock input	
20	NC	—		
21	VSS	—	Ground for digital circuit	
22	CKC	I	Clock input (sub-picture)	
23	CKCSEL	I	Internal / external 384fH VCO select	L : internal , H : external
24	CLMP	O	Clamp level output	
25	VDD	—	Power supply for digital circuit	
26	TEST	I	Test pin	normal : H
27	VSS	—	Ground for crystal oscillator	
28	XI	I	42MHz crystal oscillator input	
29	XO	O	42MHz crystal oscillator output	
30	NC	—		
31	VDD	—	Power supply for crystal oscillator	
32	NC	—		
33	NC	—		
34	CSTD	O	Internal signal output	
35	VSS	—	Ground for DRAM	
36	VDD	—	Power supply for DRAM	
37	PFIELD	O	Field odd/even output(main picture)	H:even ,L:odd
38	CFIELD	O	Field odd/even output(sub picture)	H:even ,L:odd
39	CVREF	O	Vertical sync. output(sub picture)	
40	CHREF	O	horizontal sync. output(sub picture)	
41	NC	—		
42	CKILL	O	Color killer detection output(sub picture)	H:color killer ON,L:OFF
43	VCHIP	I	23rd-line detect signal output	23rd -line :H
44	RESET	I	Reset input	L : reset
45	VDD	—	Power supply for digital circuit	

46	SDA	I/O	I ² C BUS data input , data and acknowledge output	
47	SCL	I	I ² C BUS clock input	
48	NC	—		
49	PIPEN	I	PIP enable	normal : H
50	YS	O	Main , sub-picture switching pulse	sub-picture : high
51	NC	—		
52	VSS	O	Ground for digital circuit	
53	PVD	I	Vertical sync. input (main picture)	normal : negative
54	VDD	O	Power supply for digital component	
55	NC	—		
56	PHREF	O	Horizontal sync. output(main picture)	
57	CKPSEL	I	CKP frequency selection	L:24MHz,H:48MHz
58	CKP	I	Clock input (main-picture)	
59	VSS	—	Ground for digital circuit	
60	PHD	I	Horizontal sync. input (main picture)	normal : positive
61	NC	—		
62	TESTM0	I	Test pin	normal : H
63	TESTM1	I	Test pin	normal : H
64	TESTM2	I	Test pin	normal : H
65	TEST2	I	Test pin	normal : H
66	VDD	—	Power supply for digital circuit	
67	VSS	—	Ground for digital circuit	
68	NC	—		
69	NC	—		
70	VREFD	I	Lower limit reference voltage of DAC	normal : 1.8V
71	BIAS2	—	DAC bias reference voltage	
72	NC	—		
73	BIAS1	—	DAC bias reference voltage	
74	NC	—		
75	AVDD	—	Power supply for DAC	
76	BOUT	O	Analog signal output (B-Y or B)	
77	AVSS	—	Ground for DAC	
78	ROUT	O	Analog signal output (R-Y or R)	
79	AVDD	—	Power supply for DAC	
80	YOUT	O	Analog signal output (Y or G)	

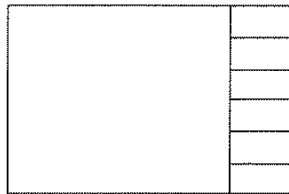
SYSTEM BLOCK DIAGRAM



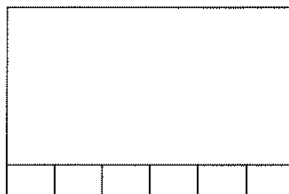
PIP mode



1 PIP mode
Size : 1/3,1/4,1/6



6 PIP mode 1
Size : 1/6 x 6



6 PIP mode 2
Size : 1/6 x 6

Function

TC90A67N/F has horizontal and vertical sync separation circuit for sub picture, color demodulation circuit for sub picture, horizontal and vertical timing generation circuit for main picture, PIP control circuit.

Color demodulation circuit consists of digital circuit, and corresponds to M-NTSC, PAL, M-PAL, N-PAL system. It is possible to process the sub picture easily, according to adopting system clock of 24MHz by digital PLL circuit locked fH. Horizontal and vertical timing generation circuit uses system clock (24MHz) generated by analog PLL circuit locked main picture's fH.

PIP control circuit consists of filter for horizontal and vertical reduction, line memory, field memory and according to changing horizontal and vertical reduction factors, it is possible to carry out various pip sizes.

1. ADC, clamping circuit

Dynamic range of ADC is 1.32Vpp whose voltage is fixed in IC. (top voltage is 2.31V, bottom voltage is 0.99V) ADC has pedestal clamp function, base voltage is output from CLMP terminal. The pedestal level becomes about 1.32V. (64LSB)

2. Horizontal and vertical sync for main picture

It is necessary to input main picture's H-sync and V-sync at PHD and PVD terminal in order to make system clock for readout stored data into the internal field memory. PHD and PVD are fitted to 5V. It can be inverted the polarity using IICBUS registers WHINV and WNINV at sub address 29hex.

At terminals of IC, polarity of H-sync is positive and V-sync is negative.

The clocks from external VCO are selectable in 24MHz and 48MHz, it can be switched by given voltage to CKPSEL(SDIP:52pin,QFP:57pin) terminal. (CKPSEL=L:24MHz、CKPSEL=H:48MHz)

3. The system clock locked to the sub picture's horizontal sync.

The signal converted into the digital environment passes through horizontal sync separation circuit, horizontal locked circuit, which construct PLL circuit, it makes the system clock locked to the sub picture's horizontal sync.

This clock is put in internal VCO and generated the system clock of 24MHz.

4.Horizontal reduction

It is necessary to limit to frequency bandwidth for Y signal and color difference signal concerning PIP mode. Horizontal reduction is selectable using HWS. (HWS : sub address 10hex)

HWS[1:0]	Horizontal reduction	Sampling rate for Y	Sampling rate for color difference
00	1/3	4MHz	1MHz
01	1/4	3MHz	0.75MHz
10	1/6	2MHz	0.5MHz
11	1/8	1.5MHz	0.375MHz

In order to horizontal reduction, LPFs are used for Y signal and color difference signal. It is selectable in two kinds of LPF for Y signal and six kinds of LPF for color difference signal.

5.Vertical reduction

It is necessary to reduce vertical direction concerning PIP mode, and vertical reduction is carried out from multiplication of coefficient as below. Vertical reduction is selectable using VWS. (VWS : sub address 10hex)

Vertical reduction	1H coefficient	2H coefficient	3H coefficient	4H coefficient	5H coefficient	6H coefficient
1/3 (VWS[1:0]=00)	1/4	1/2	1/4	—	—	—
1/4 (VWS[1:0]=01)	1/8	3/8	3/8	1/8	—	—
1/5 (VWS[1:0]=10)	1/16	1/4	3/8	1/4	1/16	—
1/6 (VWS[1:0]=11)	1/16	3/16	1/4	1/4	3/16	1/16

6.The sub picture's area of writing in the field memory and reading from the field memory

Writing start position is defined horizontal start point to write (sub address 16hex : CHS) and vertical start point to write. (sub address 16hex : CVSN or sub address 17hex : CVSP)

CVSN : Vertical frequency of sub picture is 60Hz

CVSP : Vertical frequency of sub picture is 50Hz

Horizontal width of the sub picture is defined by sampling number of horizontal direction. (sub address 1Ahex : HSPL) The number of writing vertical lines is determined internally according to vertical frequency of the main picture and VWS.

Reading start position is defined horizontal start point to read (sub address 14hex : PHS) and vertical start point to read. (sub address 14hex : PVSN or 15hex : PVSP)

PVSN : Vertical frequency of sub picture is 60Hz

PVSP : Vertical frequency of sub picture is 50Hz

Horizontal display size of the sub picture is defined by PHW (sub address 12hex) and the readout number of vertical lines is defined by PVWN (sub address 12hex) or PVWP (sub address 13hex).

PVWN : Vertical frequency of sub picture is 60Hz

PVWP : Vertical frequency of sub picture is 50Hz

7. DACs for Y signal and color difference signal

TC90A67N/F is built-in three 8bit-DAC in motion on 24MHz. Output dynamic range is determined by the difference between VDD and VREFD terminal voltage. Standard level is 1.5Vpp.

8. ACC control

ACC control is carried out comparing demodulation result of color burst signal with set reference level by ACCPAL or ACCNTSC register. (ACCPAL, ACCNTSC : sub address 21hex)

When compared value is less than the reference level, controller puts on gain, and more than reference level, controller cuts down one.

9. Peaking circuit for Y signal

It is possible to carry out a clear picture according to putting up some frequency bandwidth when sub picture becomes indistinct picture for reducing high frequency bandwidth using LPF for Y signal. There are two kinds of characteristics for LPF, and it is selectable about gain of four stages respectively using YPKGS and YPKGG.

YPKGS : select for LPF characteristics (sub address 10hex)

YPKGG : select for gain (sub address 10hex)

10. RGB matrix circuit

For a built-in RGB matrix circuit, and when RGBON=1, it can be changed R-Y,Y,B-Y into RGB signal. How to find the value of coefficient (a,b,c) is as below.

1Chex : MTXCR:a, MTXCG2:b, MTXCG1:c (on condition $0 \leq a < 1, 0 \leq b < 1, 0 \leq c < 1$)

$$R = a (R-Y) + Y$$

$$G = b \{ -(R-Y) \} + c \{ -(B-Y) \} + Y$$

$$B = (B-Y) + Y$$

12. Blue back function

It is possible to control blue back function using BBACK register.

(BBACK : sub address 13hex , BBACK=1:blue back mode)

It is available for only sub picture set to live mode. BBACK is useful when detected V chip or no signal. It can be selected in four kinds of colors using BLEVEL.

(BLEVEL : sub address 13hex)

13. Addition of frame

It is possible to add the frame to the sub picture. It is selectable frame width by FRAMEW and adjustable frame color for RGB or R-Y,Y-B respectively by FRAMEYG, FRAMER, FRAMEB.

(FRAMEW, FRAMEYG, FRAMER, FRAMEB : sub address 1Ehex)

14. CCD slice circuit

This IC has a CCD slice circuit, picks up CCD data, the CCD data and CCD slice conditions can be checked on using IIC BUS read mode.

DESCRIPTION OF I²C BUS REGISTERS

WRITE COMMAND

Sub address	bit	Name	Preset	Comment
10H	D15	—	0	Fix to '0'
	D14	TRAPFIX	0	Change fsc-trap mode. 0:auto, 1:fix
	D13	TRAP358	0	Select fsc-trap characteristic. (active at TRAPFIX=1 only) 0:4.43MHz, 1:3.58MHz
	D12,D11	YDLY1[1:0]	01	Y-output signal delay against I and V output signal (rough).
	D10	YPKGS	0	Select Y-peaking filter characteristic. 0:hi-band, 1:low-band
	D9	YLPFS	0	Select Y-horizontal decimation filter characteristic. 0:hi-band, 1:low-band
	D8,D7	YPKG[1:0]	00	Select Y-peaking gain level. 00:0, 01:1/4, 10:1/2, 11:1
	D6~D4	CLPF[2:0]	000	Select R-Y/B-Y horizontal decimation filter characteristic.
	D3,D2	VVS[1:0]	00	Select vertical decimation. 00:1/3, 01:1/4, 10:1/5, 11:1/6
D1,D0	HWS[1:0]	00	Select horizontal decimation. 00:1/3, 01:1/4, 10:1/6, 11:1/8	
11H	D15,D14	—	00	Fix to '0'
	D13	MF	0	Set single-field display mode. 0:normal, 1:Fixed to single-field display
	D12~D9	STRO[3:0]	0000	Select off-and-on cycle of field memory writing. (4 field step) 0000 : normal 0001 : strobe(once 6 fields) 1110 : strobe(once 58 fields) 0010 : strobe(once 10 fields) 1111 : still
	D8	TATEON	0	Sub-pictures' set at multi-pictures 0:horizontal, 1:vertical
	D7~D5	PIPNUM[2:0]	000	Set multi-picture numbers of the animation picture.
	D4	RON	0	Sub-picture display ON/OFF. 0:OFF, 1:ON
	D3~D1	MSNUM[2:0]	000	Select multi-strobe pictures number. 000:1-picture, 001:2-pictures, 010:3-pictures, 011:4-pictures, 100:5 pictures, 101:6 pictures
	D0	MSON	0	Select multi-strobe mode. (0:normal strobe mode, 1:multi-strobe mode)
12H	D15~D9	PHW[6:0]	011000 1	Sub-pictures range in the main-picture. (horizontal width, rough)
	D8~D0	PVWN[8:0]	001001 010	Sub-pictures range in the main-picture (vertical height) , when main-picture is 60Hz system.
13H	D15	BBACK	0	Replace sub-picture by blue-back at write-memory. 0:normal, 1:blue-back
	D14,D13	BLEVEL[1:0]	00	Select blue-back level. (DRAMCLR=1 or BBACK=1 only) 00 : black, 01 : blue1, 10 : blue2, 11 : blue3
	D12	SELGAIN	0	Control internal Y-level. 0:1.5 times, 1:Twice
	D11~D9	PHE0[2:0]	000	Sub-pictures range in the main-picture. (horizontal width, fine)
	D8~D0	PVWP[8:0]	001011 100	Sub-pictures range in the main-picture (vertical height) , when main-picture is 50Hz system.
14H	D15~D8	PHS[7:0]	001010 11	Horizontal starting point of the sub-pictures in the main-picture.
	D7~D0	PVSN[7:0]	100110 01	Vertical starting point of the sub-pictures in the main-picture , when main-picture is 60Hz system.
15H	D15~D9	PHC[6:0]	000000 0	Set clock frequency of main-picture processing. (Set the dividing number of fH PLL.)
	D8~D0	PVSP[8:0]	010000 011	Vertical starting point of the sub-pictures in the main-picture , when main-picture is 50Hz system.

Sub address	bit	Name	Preset	Comment
16H	D15~D8	CHS[7:0]	000110 01	Horizontal starting point to write into the memory in the sub-picture.
	D7~D0	CVSN[7:0]	000010 10	Vertical starting point to write into the memory in the sub-picture at 60Hz system.
17H	D15~D10	BRTRGB [5:0]	000000	Control bright at RGB mode. 100000:-32LSB, 000000:0LSB, 011111:+31LSB
	D9	—	1	Fix to '1'
	D8~D0	CVSP[8:0]	100010 010	Vertical starting point to write into the memory in the sub-picture at 50Hz system.
18H	D15	DRAMCLR	0	Field-memory reset 0:normal, 1:reset
	D14	—	1	Fix to '1'
	D13	—	0	Fix to '0'
	D12~D0	WADOS [12:0]	000000 000000 0	Set start-address to write the memory. (for the memory partition to memorize several sub-pictures at the same time.)
19H	D15~D13	—	000	Fix to '0'
	D12~D0	RADOS [12:0]	000000 000000 0	Set start-address to read from the memory. (for the select of sub-pictures in the memory)
1AH	D15~D10	HSPL[5:0]	110010	Set number of horizontal sampling on the input sub-picture.
	D9~D5	CLVL[4:0]	00000	Set color-level. 10000:-6dB, 00000: 0dB, 01111:+6dB
	D4~D0	CTRRT[4:0]	00000	Set contrast level. 10000:-5dB, 00000: 0dB, 01111:+3dB
1BH	D15,D14		00	Fix to '0'
	D13~D8	HUEBIAS [5:0]	000000	Adjustment the demodulation phases for R-Y signal. (NTSC only) 000000:0°, 111111:+45°
	D7~D0	HUE[7:0]	000000 00	Adjustment the demodulation phase for R-Y and B-Y signals. (NTSC only) 10000000:-45°, 00000000: 0°, 01111111:+45°

Sub address	bit	Name	Preset	Comment
1CH	D15~D10	MTXCB[5:0]	110001	Set RGB matrix coefficient 1.
	D9~D5	MTXCG [24:20]	01100	Set RGB matrix coefficient 2.
	D4~D0	MTXCG [14:10]	01010	Set RGB matrix coefficient 3.
1DH	D15~D10	YGOS[5:0]	000000	Set DC offset of sub-picture. (Y or G signal) 100000:-32LSB, 000000:0LSB, 011111:+31LSB
	D9~D5	ROS[4:0]	00000	Set DC offset of sub-picture.(R-Y or R signal) 10000:-16LSB, 00000:0LSB, 01111:+15LSB
	D4~D0	BOS[4:0]	00000	Set DC offset of sub-picture. (B-Y or B signal) 10000:-16LSB, 00000:0LSB, 01111:+15LSB
1EH	D15,D14	YSDLY[1:0]	01	Timing offset of Ys pulse. 00:-1ck, 01:center, 10:+1ck, 11:+2ck (24MHz)
	D13,D12	FRAMEW [1:0]	00	Select the side frame width of sub-picture 00 : OFF (no-frame) , 01 : narrow , 10 : center , 11 : wide
	D11~D8	FRAMEYG [3:0]	0000	Select frame signal level of PIP. (Y or G signal)
	D7~D4	FRAMER [3:0]	0000	Select frame signal level of PIP. (R-Y or R signal)
	D3~D0	FRAMEB [3:0]	0000	Select frame signal level of PIP. (B-Y or B signal)
1FH	D15,D14	TYDLY[1:0]	00	Y-output signal delay for U and V output signal. (fine).
	D13	—	0	Fix to '0'
	D12	PMDFIX	0	Clock frequency to read from the memory. 0:auto, 1:fix
	D11,D10	PMDS[1:0]	00	Select Clock frequency to read from the memory. (active at PMDFIX=1 only) 00:12MHz, 01:9MHz, 10:18MHz, 11:16MHz
	D9	OFF2527	0	Set 50Hz/60Hz-conversion mode. (VWS=1/3 mode only) 0:ON, 1:OFF
	D8	SELREV	0	Set reverse mode. 0:normal, 1:reverse
	D7~D3	—	00000	Fix to '0'
	D2	PFLDREV	1	Reverse PFIELD at internal circuit. 0:reverse, 1:normal
	D1	CFLDREV	0	Reverse CFIELD at internal circuit. 0:normal, 1:reverse
D0	RGBON	1	Select output signal format. 0:YUV, 1:RGB	
20H	D15~D8	CHLOADN [7:0]	111111 10	Set clock frequency of sub-picture processing at 60Hz system. (Set the dividing number of H-PLL)
	D7~D0	CHLOADP [7:0]	111110 01	Set clock frequency of main-picture processing at 50Hz system. (Set the dividing number of H-PLL)

Sub address	bit	Name	Preset	Comment
21H	D15,D14	—	00	Fix to '0'
	D13~D7	ACCPAL [6:0]	011101 0	Set ACC reference level (for PAL). 0:Minimum level 127:Maximum level
	D6~D0	ACCNTSC [6:0]	101000 1	Set ACC reference level (for NTSC). 0:Minimum level 127:Maximum level
22H	D15,D14	—	00	Fix to '0'
	D13~D7	KILON[6:0]	000110 0	Set color killer ON level. 0:Minimum level 63:maximum level It must be set "KILON" < "KILOFF"
	D6~D0	KILOFF[6:0]	001010 0	Set color killer OFF level. 0:Minimum level 63:maximum level It must be set "KILON" < "KILOFF"
23H	D15,D14	—	00	Fix to '0'
	D13~D7	NTSOFF [6:0]	001010 0	Set level to turn over from NTSC to PAL in NTSC/PAL detector. 0:Minimum level 63:maximum level It must be set "NTSON" < "NTSOFF"
	D6~D0	NTSON[6:0]	000110 0	Set level to turn over from PAL to NTSC in NTSC/PAL detector. 0:Minimum level 63:maximum level It must be set "NTSON" < "NTSOFF"
24H	D15~D7	—	000000 000	Fix to '0'
	D6~D0	PIDREF[6:0]	111011 0	Sensitivity of PAL-IDENT detection. 0 : Minimum Sensitivity 63:Maximum Sensitivity
25H	D15~D12	—	0000	Fix to '0'
	D11~D8	—	1111	Fix to '1'
	D7,D6	—	00	Fix to '0'
	D5,D4	FSSTM[1:0]	10	Set cycle of color system detection in color sub-carrier frequency detector. (1 field step) 0 : 1 field 3 : 4 fields
	D3,D2	FSSEL[1:0]	00	Set color system of sub-picture processing.(at FSMO=11 only) 00:N-PAL , 01:M-PAL , 10:M-NTSC , 11:BG-PAL/4.43NTSC
	D1,D0	FSMO[1:0]	01	Mode for color sub-carrier frequency search 00:M-NTSC only, 01:BG-PAL/4.43NTSC→M-NTSC, 10:N-PAL→M-PAL→M-NTSC, 11:FSSEL[1:0]

READ COMMAND

Sub address	bit	Name	Comment
00H	D15	CRI3DET	CRI detection.
	D14~D11	CRIN[3:0]	CRI number detection.
	D10	CFIELD	Field-detection. (Sub-picture)
	D9	SBDET	Start-bit (001) detection. 0:not start-bit detected,1:start-bit detected
	D8	AEDGE	Caution of too near sampling point for back-edge of data. 0:OK, 1:too near
	D7	BEDGE	Caution of too near sampling point for front-edge of data. 0:OK, 1:too near
	D6~D0	SLV[6:0]	Slice level data.
01H	D15~D0	CCDDATA [15:0]	CCD data including parity bits.
02H	D15	NOSIG	Result of no-signal detection (Sub-picture) 0: exist, 1:not-signal
	D14	CVMD525	Vertical sync frequency standard/non-standard detection. (Sub-picture) 0:Non-standard, 1:Standard
	D13	CNOVPN	Vertical sync detection. (Sub-picture) 0:exist, 1:No vertical sync
	D12	CVDET60	Vertical frequency detection. (Sub-picture) 0:50Hz, 1:60Hz
	D11,D10	BCF[1:0]	System mode detection. (Sub-picture) 00:N-PAL, 01:M-PAL, 10:M-NTSC, 11:BG-PAL/4.43NTSC
	D9	PVMD525	Vertical sync frequency standard/non-standard detection. (Main-picture) 0:Non-standard, 1:Standard
	D8	PNOVPN	Vertical sync detection. (Main-picture) 0:exist, 1:No vertical sync
	D7	PVDET60	Vertical frequency detection. (Main-picture) 0:50Hz, 1:60Hz
	D6	CKIL	Color Killer detection. (Sub-picture) 0:Killer-off, 1:Killer-on
	D5	PDUNLOCK	H-PLL condition. (Sub-picture) 0:Lock, 1:Un-lock
D4	PALDET	PAL signal detection. 0:NTSC or No-color, 1:PAL	

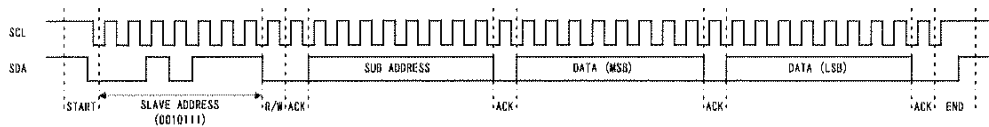
OUTLINE OF I²C BUS CONTROL FORMAT

Sub-pictures range in the main-picture. (horizontal width)

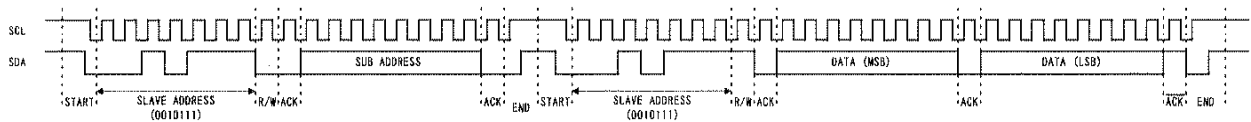
• SLAVE ADDRESS

A6	A5	A4	A3	A2	A1	A0	R/W
0	0	1	0	1	1	1	1/0

• WRITE FORMAT



• READ FORMAT



Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

ELECTRICAL CHARACTERISTICS**DC CHARACTERISTICS**DIGITAL PART OPERATING CONDITION: $V_{DD}=3.3V, T_a=25^{\circ}C$

CHARACTERISTIC		SYM-BOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINALS
Consumption Current		I_{DD}	—	—	—	160	230	mA	—
High Level Input Voltage	CMOS Input	V_{IH1}	—	—	2.4	—	V_{DD}	V	(*1)
	Schmitt Trigger input	V_{IH2}	—	—	2.4	—	V_{DD}	V	(*2)
Low Level Input Voltage	CMOS Input	V_{IL1}	—	—	—	—	0.8	V	(*1)
	Schmitt Trigger input	V_{IL2}	—	—	—	—	0.8	V	(*2)
Input Current	High Level	I_{IH}	—	—	-10	—	+10	μA	(*1) (*2)
	Low Level	I_{IL}	—	—	-10	—	+10	μA	(*1) (*2)
Output Voltage	High Level	V_{OH}	—	—	2.4	—	—	V	(*3)
	Low Level	V_{OL}	—	—	—	—	0.4	V	(*3)

(*1) CKC,CKOSEL,TEST,SDA,PIPEN,CKPSEL,CKP,TESTM0,TESTM1,TESTM2,TEST2

(*2) RESET,SCL,PVD,PHD

(*3) CLMP,CSTD,PFIELD,CFIELD,CVREF,CHREF,CKILL,VCHIP,YS,PHREF

ADC CHARACTERISTICS OPERATING CONDITION: $V_{DD}=3.3V, T_a=25^{\circ}C$

CHARACTERISTIC		SYM-BOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINALS	
A/D Converter	Resolution	R_{S1}	—	—	—	—	8	bit	—	
	Input Level	ADIN	—	$AV_{DD}=3.3V$	—	1.32	—	V_{P-P}	CVI	
	Pin Voltage	BIASA	—	—	—	—	0.9	—	V	BIASA
		VREFH	—	—	—	—	2.3	—	V	VREFH
		VREFL	—	—	—	—	1.0	—	V	VREFL
	Non-linear Error	ILE1	—	24MHz	—	—	± 3	—	LSB	—
Diferencial Non-linear Error	DLE1	—	24MHz	—	—	± 2	—	LSB	—	

DAC, VCO CHARACTERISTICS OPERATING CONDITION: $V_{DD}=3.3V, T_a=25^{\circ}C$

CHARACTERISTIC		SYM-BOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINALS
D/A Converter (VIDEO)	Resolution	R_{S2}	—	—	—	—	8	bit	—
	Output Level	YOUT	—	$AV_{DD}=3.3V$	—	—	1.5	$V_{P.P}$	YOUT
		ROUT	—	$AV_{DD}=3.3V$	—	—	1.5	$V_{P.P}$	ROUT
		BOUT	—	$AV_{DD}=3.3V$	—	—	1.5	$V_{P.P}$	BOUT
	Non-linear Error	ILE2	—	24MHz	—	—	± 1	LSB	—
	Differential Non-linear Error	DLE2	—	24MHz	—	—	± 1	LSB	—
	Pin Voltage	BIAS1	—	—	—	1.0	—	V	BIAS1
		BIAS2	—	—	—	2.0	—	V	BIAS2
	Reference Voltage Level	VREFD	—	—	—	—	1.8	V	VREFD
Output Impedance	ZOUT1	—	—	—	200	—	Ω	YOUT,ROUT, BOUT	
D/A Converter (CLOCK)	Resolution	R_{S3}	—	—	—	—	6	bit	—
	Output Level	CKOUT	—	$AV_{DD}=3.3V$	—	—	1.5	$V_{P.P}$	CKOUT
	Non-linear Error	ILE3	—	24MHz	—	—	± 3	LSB	—
	Differential Non-linear Error	DLE3	—	24MHz	—	—	± 2	LSB	—
	Pin Voltage	BIASD	—	—	—	1.0	—	V	BIASD
	Reference Voltage Level	VREF	—	—	—	—	1.8	V	VREF
	Output Impedance	ZOUT2	—	—	—	200	—	Ω	CKOUT
VCO	Pull-in Frequency	FCK	—	—	—	6.0	—	MHz	—
	Input Amplitude	VCK	—	—	1.0	—	—	V	CKIN

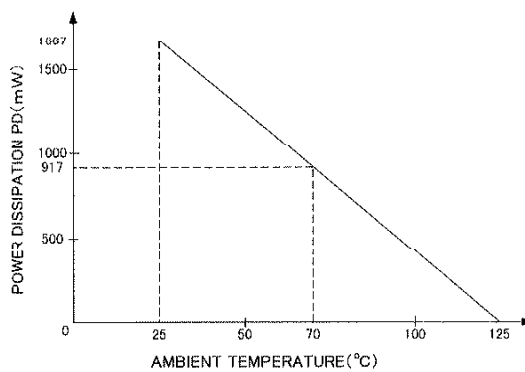
AC CHARACTERISTICS OPERATING CONDITION : $V_{DD}=3.3V, T_a=25^{\circ}C$

CHARACTERISTIC	SYM-BOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINALS
Operating Clock	Fopr1	—	CKP=1536fH	—	24.0	—	MHz	—
Operating Clock	Fopr2	—	CKC=1536fH	—	24.0	—	MHz	—

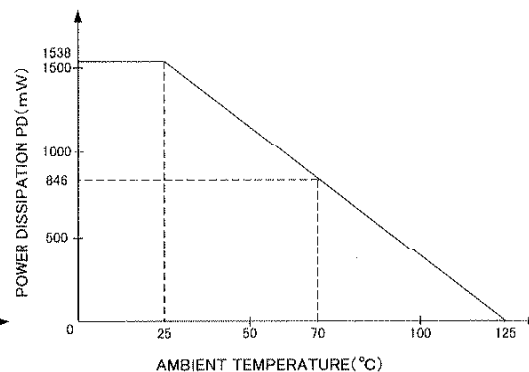
MAXIMUM RATINGS (V_{SS}=0V, T_a=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	V _{SS} to V _{SS} +4.5	V
Applied Voltage	V _{IN}	-0.3 to V _{DD} +0.3	V
Applied Current	I _{IN}	±10	mA
Power Dissipation	PD	SDIP64	1667
		QFP80	1538
Storage Temperature	T _{STG}	-55 to 125	°C

TD-PD (On board mounting)



(SDIP64)

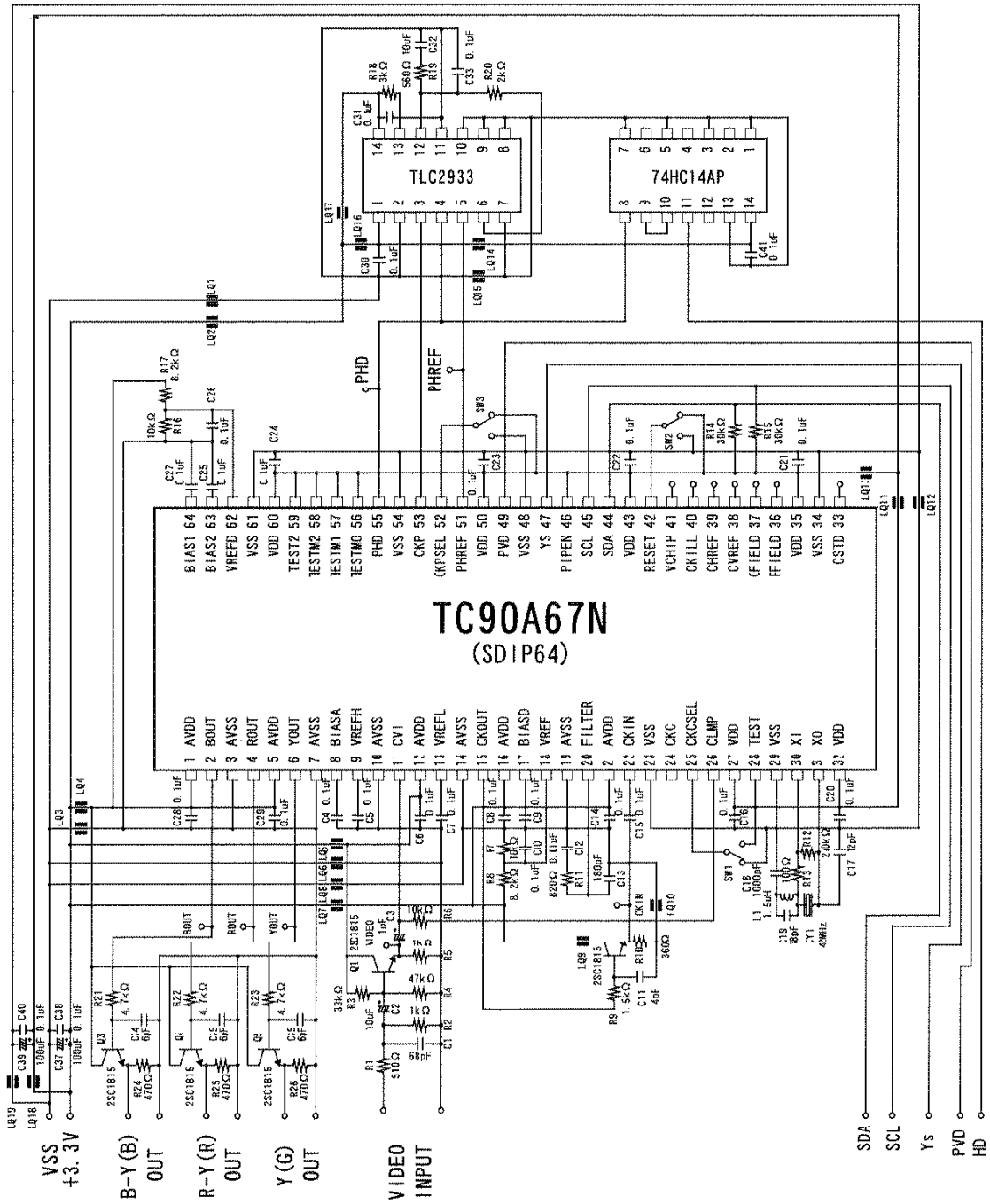


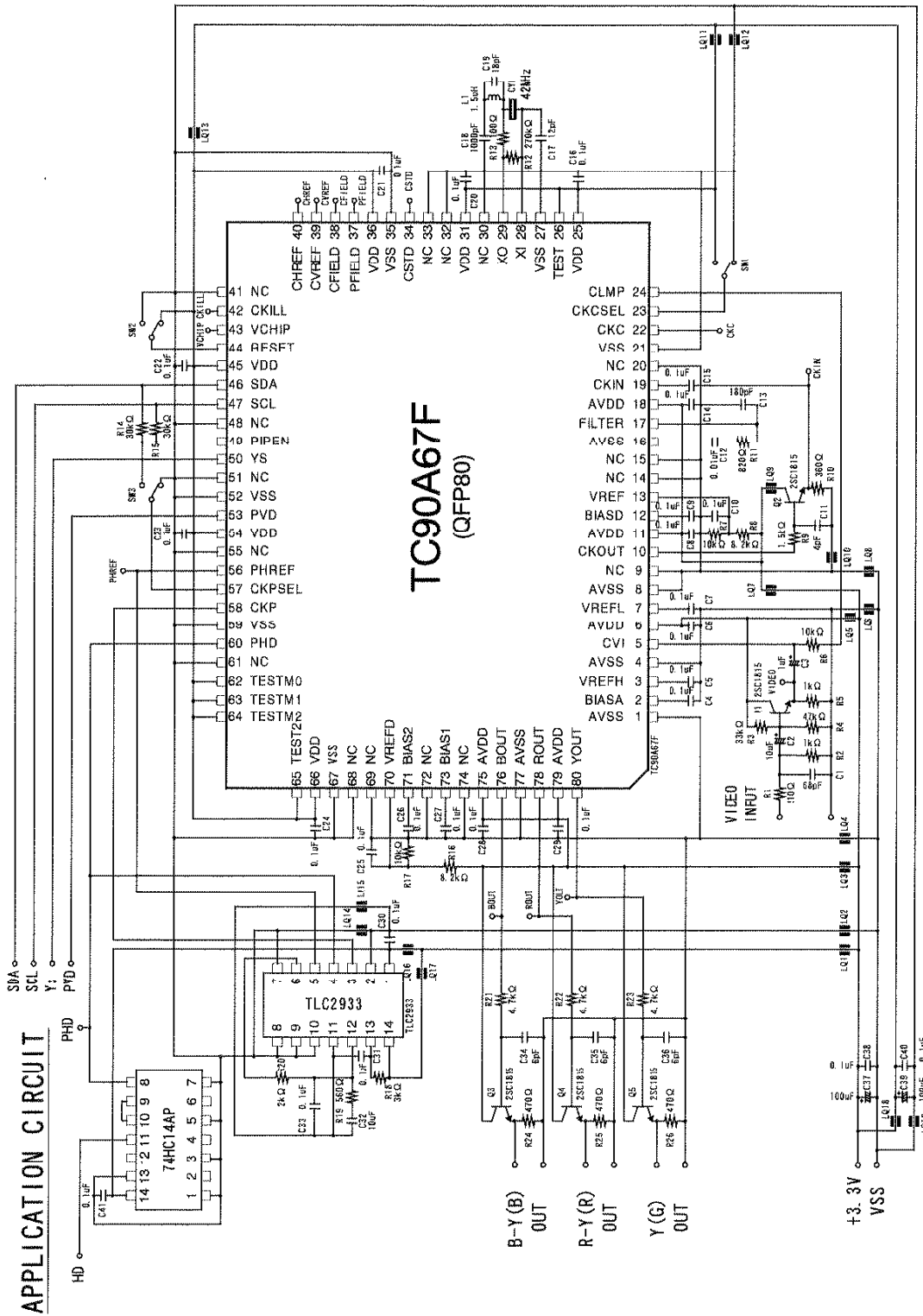
(QFP80)

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	3.0 to 3.6	V
Input Voltage	V _{IN}	0 to V _{DD}	V
Output Voltage	V _{OUT}	0 to V _{DD}	V
Ambient Temperature	T _{OPR}	-10 to 70	°C

APPLICATION CIRCUIT

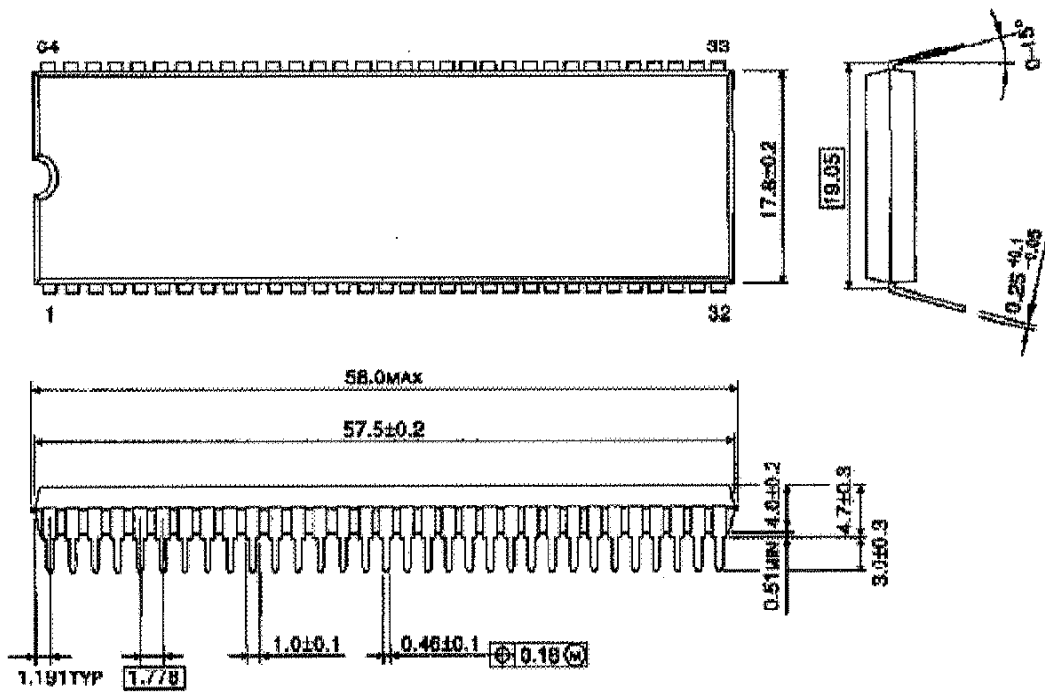




OUTLINE DRAWING

SDIP64-P-750-1.78

Unit : mm



QFP80-P-1420-0.80B

Unit : mm

