HD66115T

160-Channel Common Driver Packaged in a Slim Tape Carrier Package

HITACHI

Description

The HD66115T is a common driver for large dot matrix liquid crystal graphics displays. It features 160 channels which can be divided into two groups of 80 channels by selecting data input/output pins. The driver is powered by about 3 V, making it suitable for the design of portable equipment which fully utilizes the low power dissipation of liquid crystal elements. The HD66115T, packaged in a slim tape carrier package (slim-TCP), makes it possible to reduce the size of the user area (wiring area).

Features

- Duty cycle: About 1/100 to 1/480
- 160 LCD drive circuits
- High LCD driving voltage: 14 V to 40 V
- Output division function (2 × 80-channel outputs)
- Display off function
- Operating voltage: 2.5 V to 5.5 V
- Slim-TCP
- Low output impedance: 0.7 kΩ (typ)

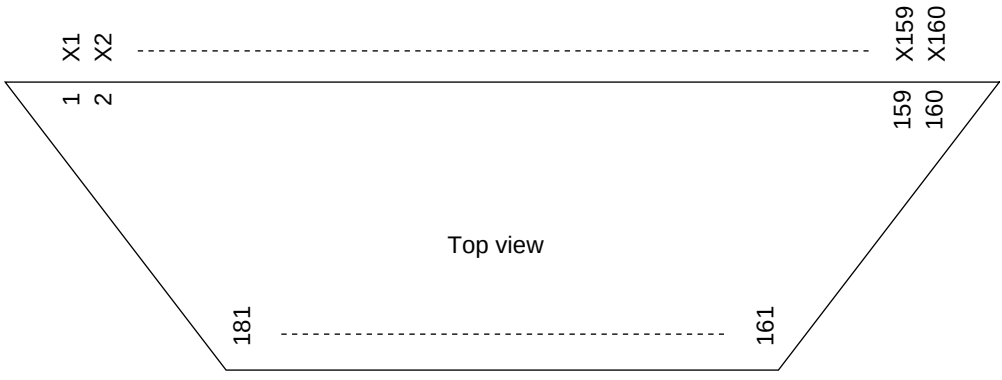
Ordering Information

Type No.	Outer Lead Pitch (µm)
HD66115TA0	180
HD66115TA1	250

Note: The details of TCP pattern are shown in “The Information of TCP.”

Hitachi semiconductor

Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

Pin Assignments

V2L	V5L	V6L	V1L	$V_{LCD}1$	GND1	CH	SHL	$\overline{DISPOFF}$	M	CL	GND2	DIO1	DI	DIO2	V_{CC}	V1R	V6R	$V_{LCD}2$	V5R	V2R
181	180	179	178	177	176	175	174	173	172	171	170	169	168	167	166	165	164	163	162	161

Pin Descriptions

Symbol	Pin No.	Pin Name	Input/Output	Classification
V_{LCD}1, 2	177, 163	V_{LCD}	—	Power supply
V_{CC}	166	V_{CC}	—	Power supply
GND1, 2	176, 170	GND	—	Power supply
V_1L, V_1R	165, 178	V_1L, V_1R	Input	Power supply
V_2L, V_2R	161, 181	V_2L, V_2R	Input	Power supply
V_5L, V_5R	162, 180	V_5L, V_5R	Input	Power supply
V_6L, V_6R	164, 179	V_6L, V_6R	Input	Power supply
CL	171	Clock	Input	Control signal
M	172	M	Input	Control signal
CH	175	CH	Input	Control signal
SHL	174	Shift left	Input	Control signal
DIO1	169	Data	Input/output	Control signal
DIO2	167	Data	Input/output	Control signal
DI	168	Data	Input	Control signal
$\overline{\text{DISPOFF}}$	173	Display off	Input	Control signal
X1–X160	1–160	X1–X160	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

V_{LCD}, GND: Supply power to the LCD drive circuits (figure 1).

V_1L, V_1R, V_2L, V_2R, V_5L, V_5R, V_6L, V_6R: Supply different power levels to drive the LCD. V_1 and V_2 are selected levels, and V_5 and V_6 are non-selected levels.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes the LCD drive outputs to AC.

CH: Selects the data shift mode. (CH = high: 2 × 80-output mode, CH = low: 160-output mode)

SHL: Selects the data shift direction for the shift register and the common signal scan direction (figure 2).

DIO1, DIO2: Input or output data. DIO1 is input and DIO2 is output when SHL is high. DIO1 is output and DIO2 is input when SHL is low.

DI: Input data. DI is input to X81–X160 when CH and SHL are high, and to X81–X1 when SHL is low.

$\overline{\text{DISPOFF}}$: Controls LCD output level. A low $\overline{\text{DISPOFF}}$ sets the LCD drive outputs X1–X160 to the V_2 level. A high $\overline{\text{DISPOFF}}$ is normally used.

LCD Drive Outputs

X1–X160: Each X outputs one of four voltage levels V_1, V_2, V_5, or V_6, depending on the combination of the M signal and the data level (figure 3).

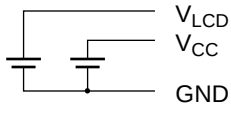


Figure 1 Power Supply for LCD Driver

SHL	Data shift direction
High	Shift to right DIO1 → SR1 → SR2 → SR3 • • • → SR160 → DIO2
Low	Shift to left DIO2 → SR160 → SR159 • • • → SR1 → DIO1

Note: SR1 to SR160 correspond to the outputs of X1 to X160, respectively.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL

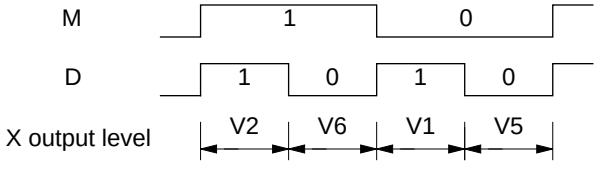
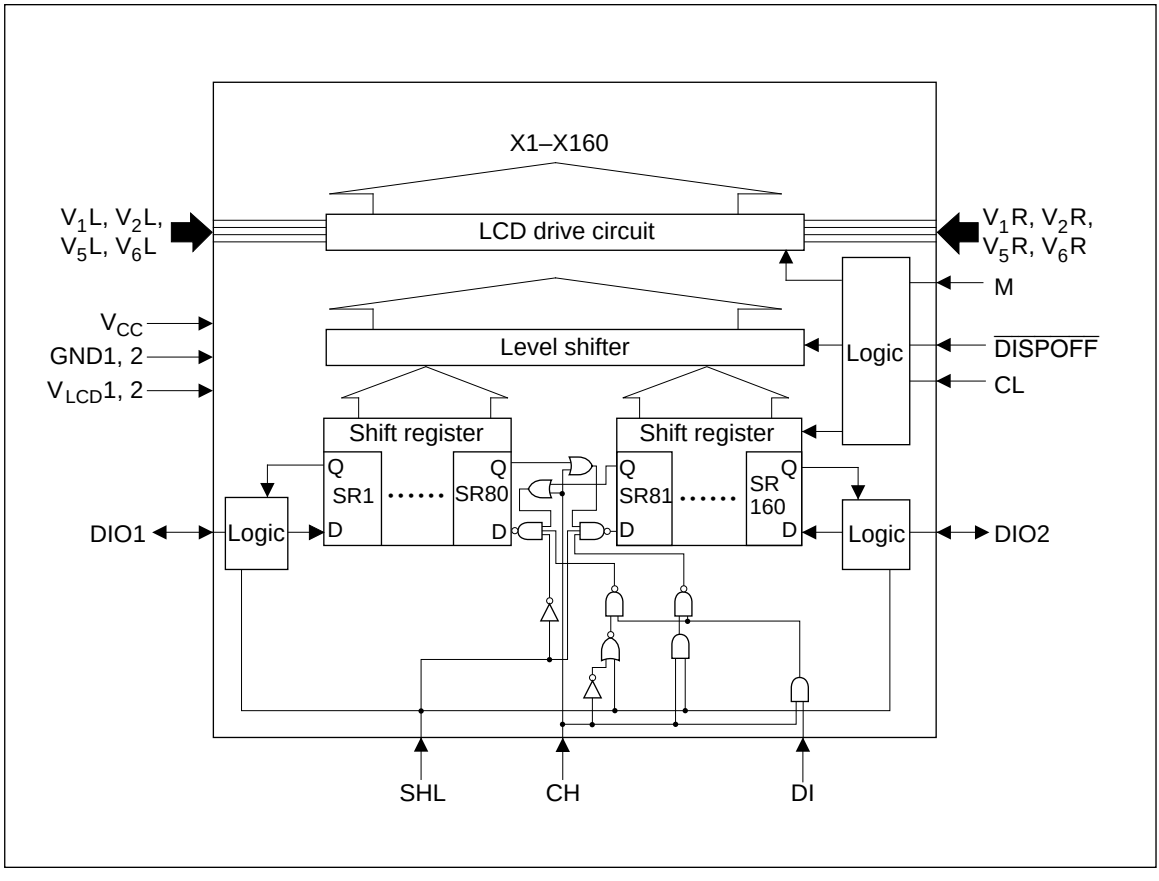


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuit

The 160-bit LCD drive circuit generates four voltage levels V_1, V_2, V_5, and V_6, which drive the LCD panel. One of these four levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

Level Shifter

The level shifter changes logic control signals (2.5 V–5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Register

The 160-bit shift register shifts the data input via the DIO pin by one bit at a time. The one bit of shifted-out data is output from the DIO pin to the next driver IC. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL pin selects the data shift direction.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	V_{LCD}	–0.3 to +42	V	1, 5
Input voltage 1	V_{T1}	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	V_{T2}	V_{LCD} – 7.0 to V_{LCD} + 0.3	V	1, 3
Input voltage 3	V_{T3}	–0.3 to +7.0	V	1, 4
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–40 to +125	°C	

Notes:
1. The reference point is GND (0 V).
2. Applies to pins CL, M, SHL, DI, $\overline{\text{DISPOFF}}$, and CH.
3. Applies to pins V_1 and V_6.
4. Applies to pins V_2 and V_5.
5. Power should be applied to V_{CC}–GND first, and then V_{LCD}–GND. It should be disconnected in the reverse order.
6. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged. It should always be used within its specified operating range in order to prevent malfunctions or loss of reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, V_{LCD} – GND = 14 to 40 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	1	0.8 × V_{CC}	—	V_{CC}	V		
Input low voltage	V_{IL}	1	0	—	0.2 × V_{CC}	V		
Output high voltage	V_{OH}	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	V_{OL}	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Xj on resistance	R_{ON}	3	—	0.7	1.0	kΩ	I_{ON} = 150 µA	1
Input leakage current 1	I_{IL1}	1	–5	—	5	µA	V_{IN} = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	V_{IN} = V_{LCD} to GND	
Current consumption 1	I_{GND}	—	—	—	0.5	µA	f_{CL} = 36 kHz f_M = 75 kHz	2
Current consumption 2	I_{LCD}	—	—	—	1.0	µA		

Note: Pins: 1. CL, M, SHL, CH, DI, DIO1, DIO2, $\overline{\text{DISPOFF}}$
2. DIO1, DIO2
3. X1–X160, V
4. V_1, V_2, V_5, V_6

Notes: 1. Indicates the resistance between one of the pins X1–X160 and one of the voltage supply pins V_1, V_2, V_5, or V_6, when load current is applied to the X pin; defined under the following conditions:

Ta = 25°C Note that RON depends on Ta (°C) (figure 4).
V_{LCD}–GND = 40 V
V_1, V_6 = V_{CC} – {1/20 (V_{LCD}–GND)}
V_5, V_2 = GND + {1/20 (V_{LCD}–GND)}

All voltages must be within ΔV, $V_{LCD} \geq V_1 \geq V_6 \geq V_{LCD} - 7.0$ V, and 7.0 V ≥ $V_5 \geq V_2 \geq$ GND. Note that ΔV depends on the power supply voltage V_{LCD}–GND (figure 6).

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be held at V_{CC} and GND, respectively.

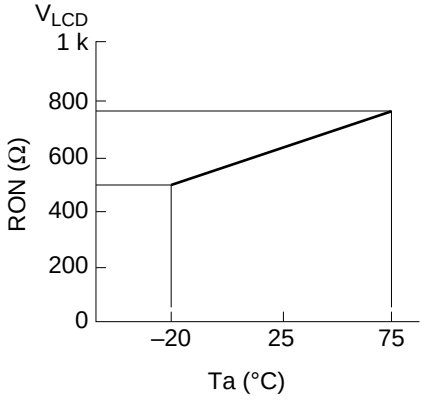


Figure 4 Relation between RON and Ta

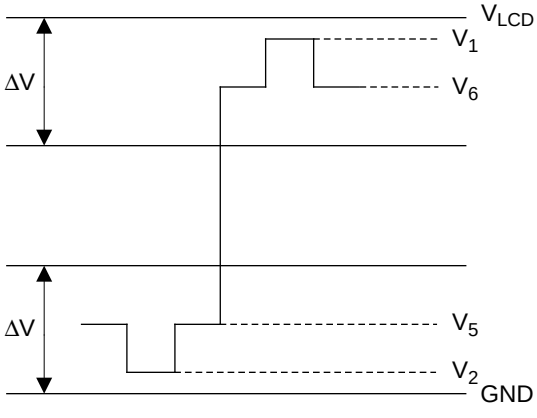


Figure 5 Relation between Driver Output Waveform and Voltage Levels

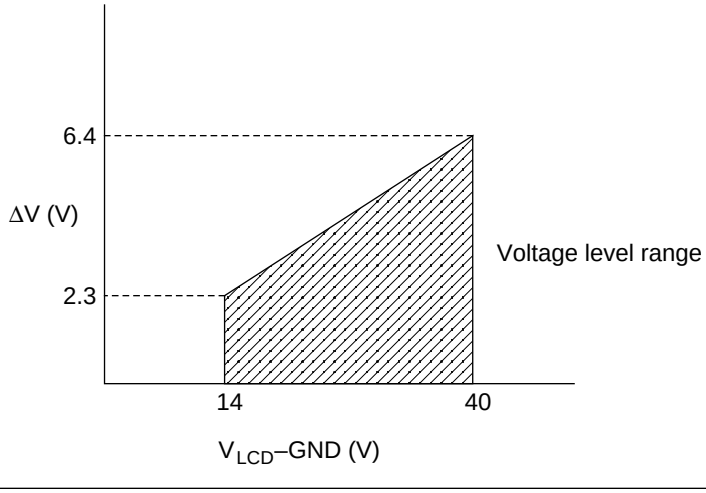


Figure 6 Relation between V_{LCD}–GND and ΔV

AC Characteristics (V_{CC} = 2.5 to 5.5 V, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	350	ns	1
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	1.2	µs	2
Output delay time 2	t_{pd2}	X (n), M	—	1.2	µs	2

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, and T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	
Clock fall time	t_f	CL	—	30	ns	
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	150	ns	1
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	0.7	µs	2
Output delay time 2	t_{pd2}	X (n), M	—	0.7	µs	2

Note: 1, 2 The load circuit shown in figure 6 is connected.

Figure 7 Load Circuit

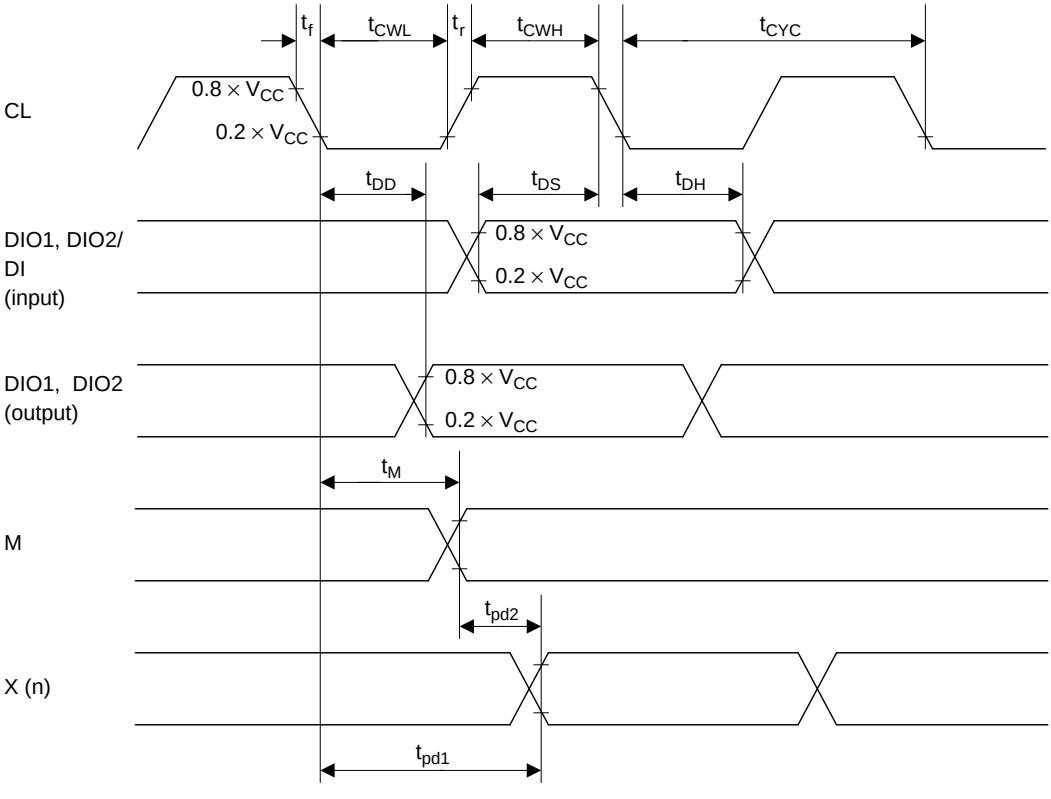
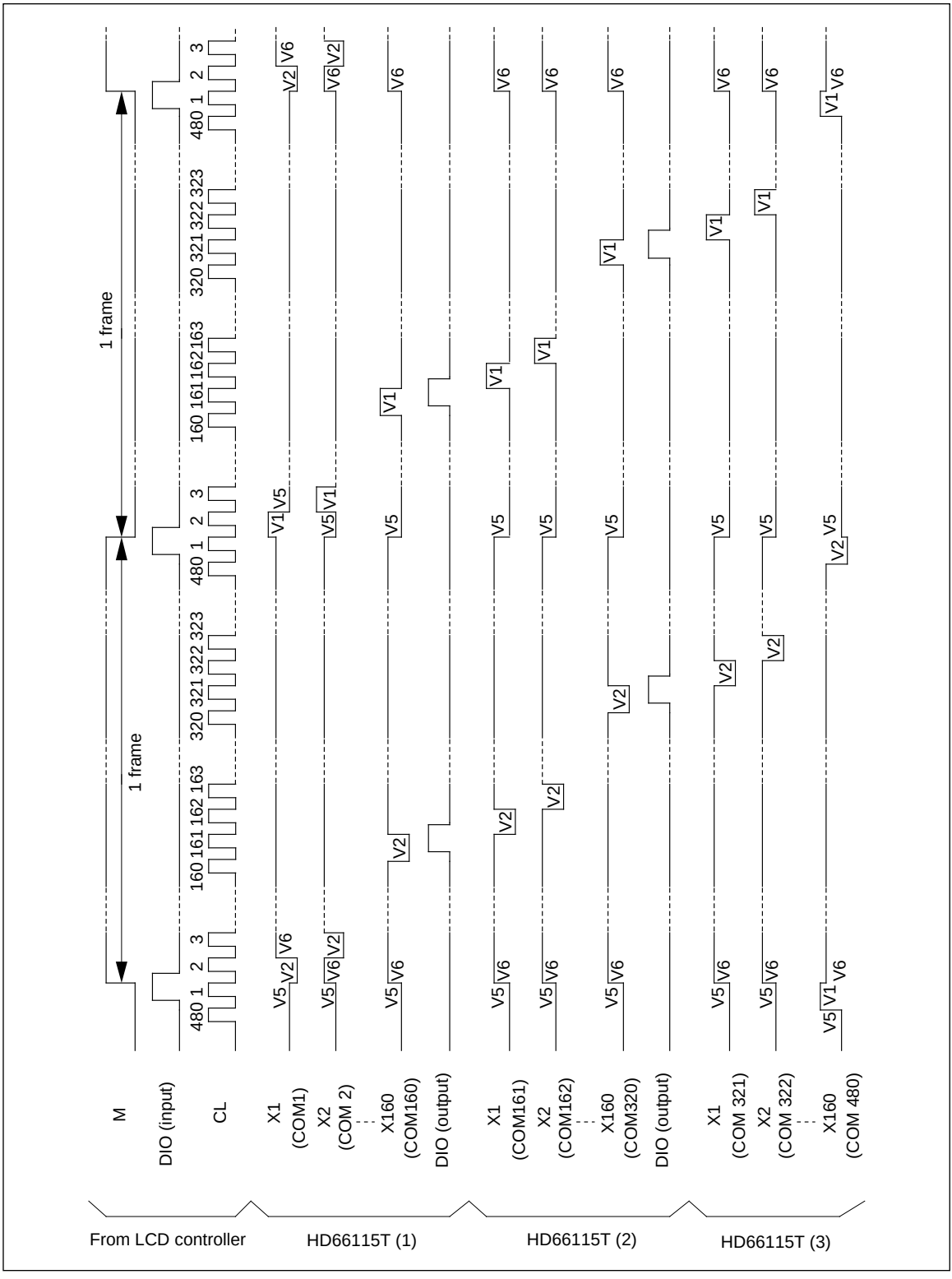


Figure 8 LCD Controller Interface Timing

Operation Timing (1/480 Duty Cycle)



Connection Examples

Figures 8 and 9 show examples of how HD66115Ts can be configured to drive a 480-line LCD panel with a 1/240 duty cycle. Figures 10 and 11 show examples of how HD66115Ts can be configured to drive a 480-line LCD panel with a 1/480 duty cycle. The HD66115T's 160 channels can be divided into two groups of 80 channels, and its data shift direction can be changed by selecting the data output mode pin (CH) and data shift pin (SHL), respectively.

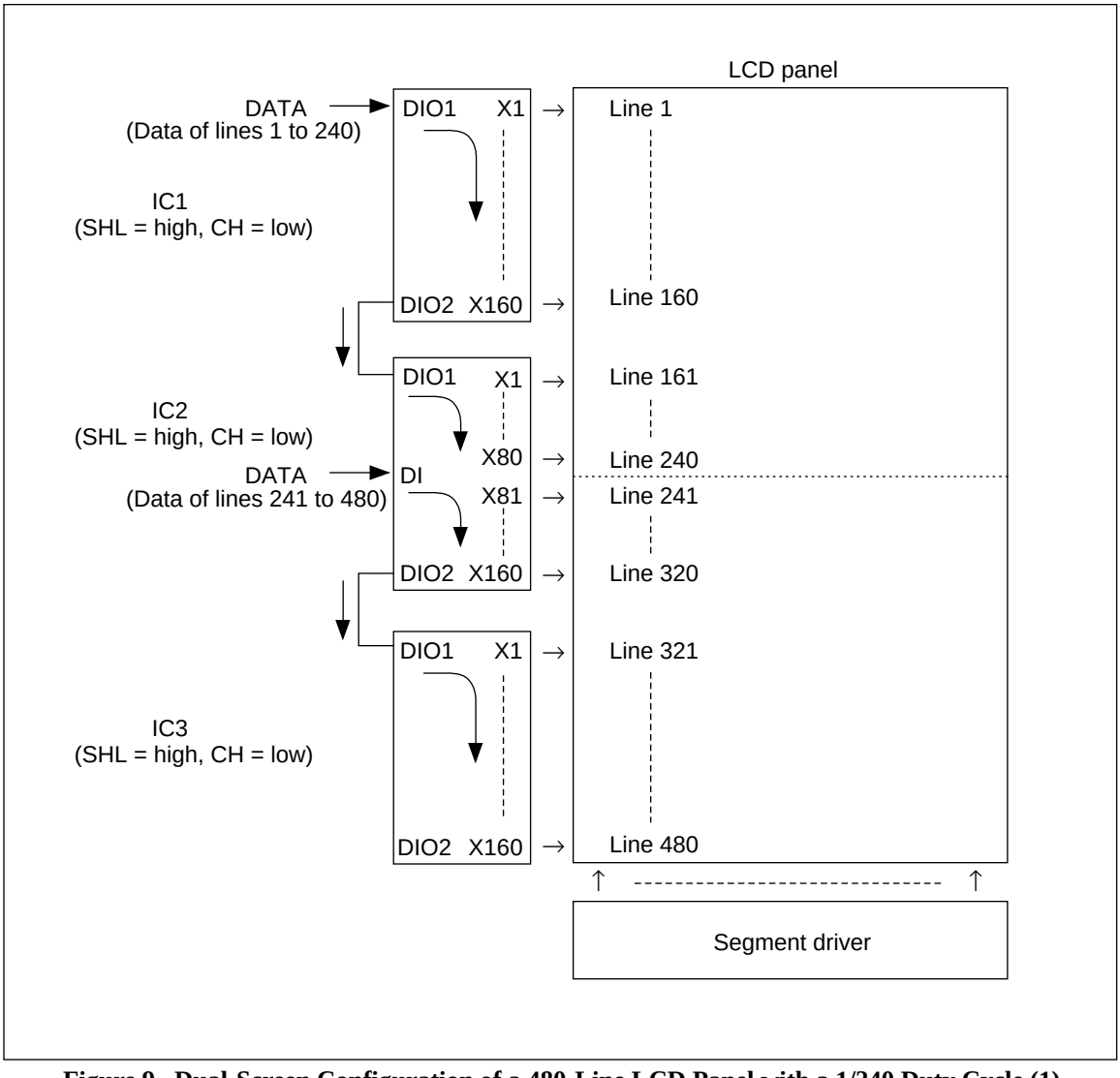


Figure 9 Dual-Screen Configuration of a 480-Line LCD Panel with a 1/240 Duty Cycle (1)

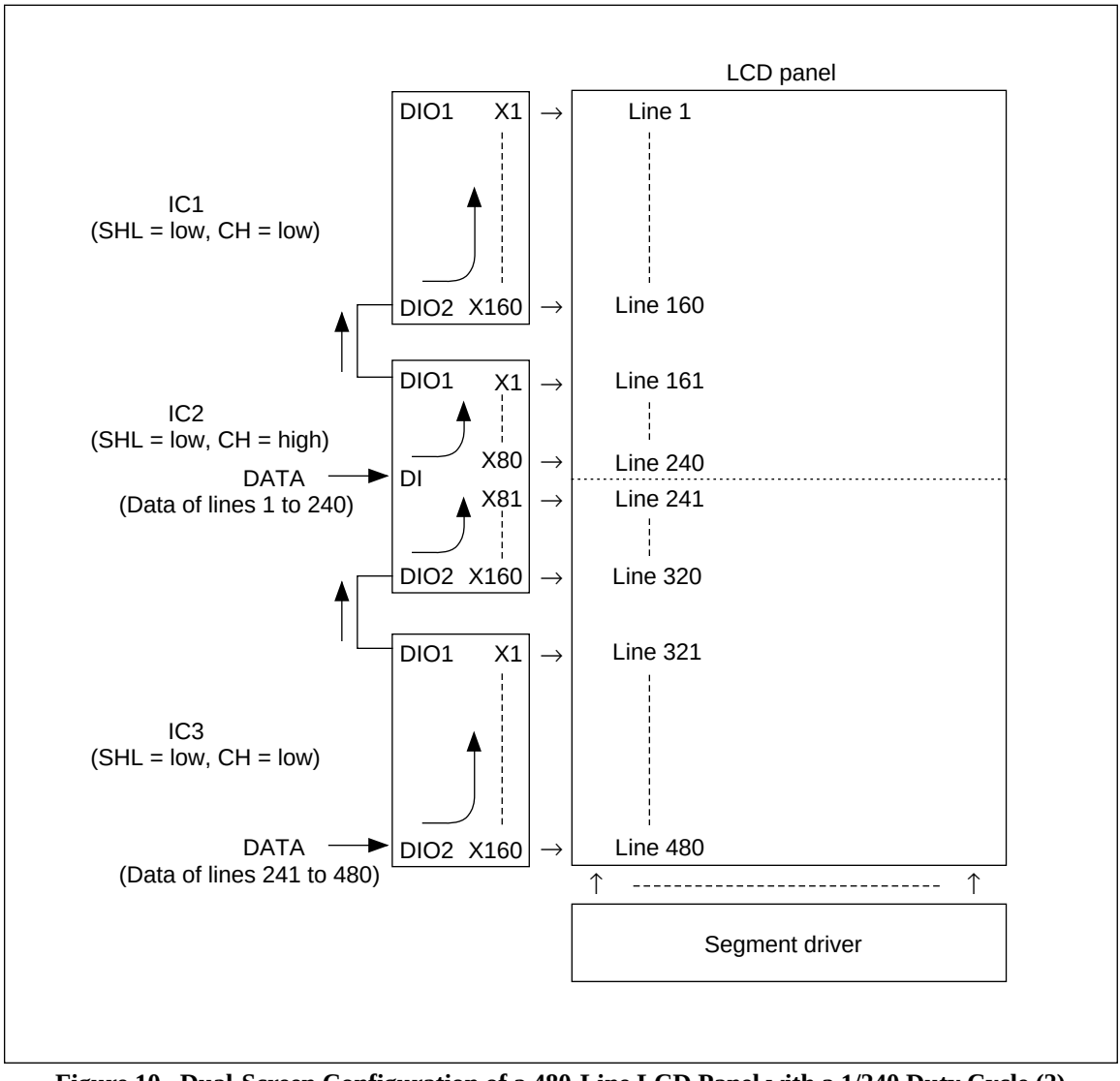


Figure 10 Dual-Screen Configuration of a 480-Line LCD Panel with a 1/240 Duty Cycle (2)

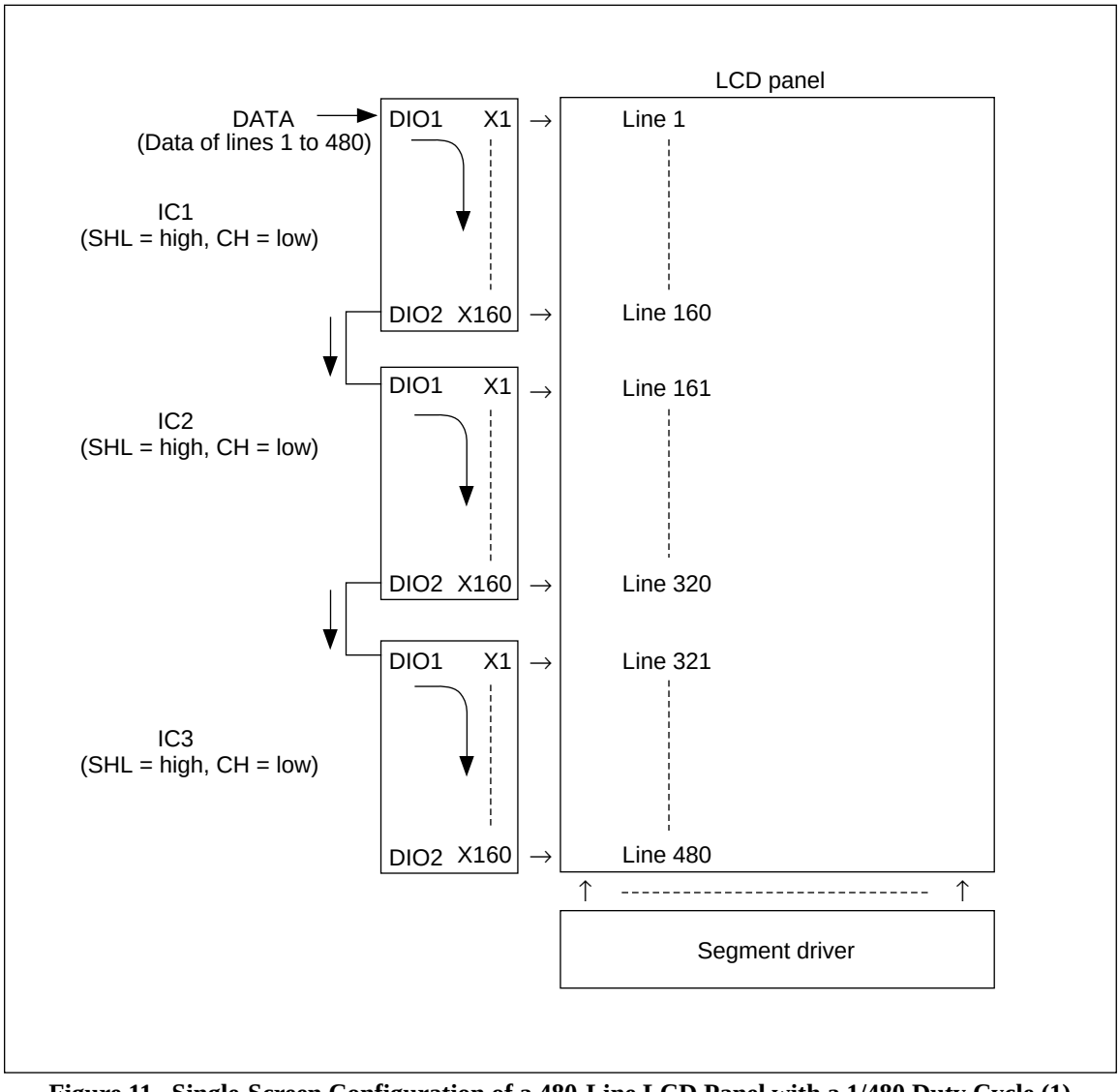


Figure 11 Single-Screen Configuration of a 480-Line LCD Panel with a 1/480 Duty Cycle (1)

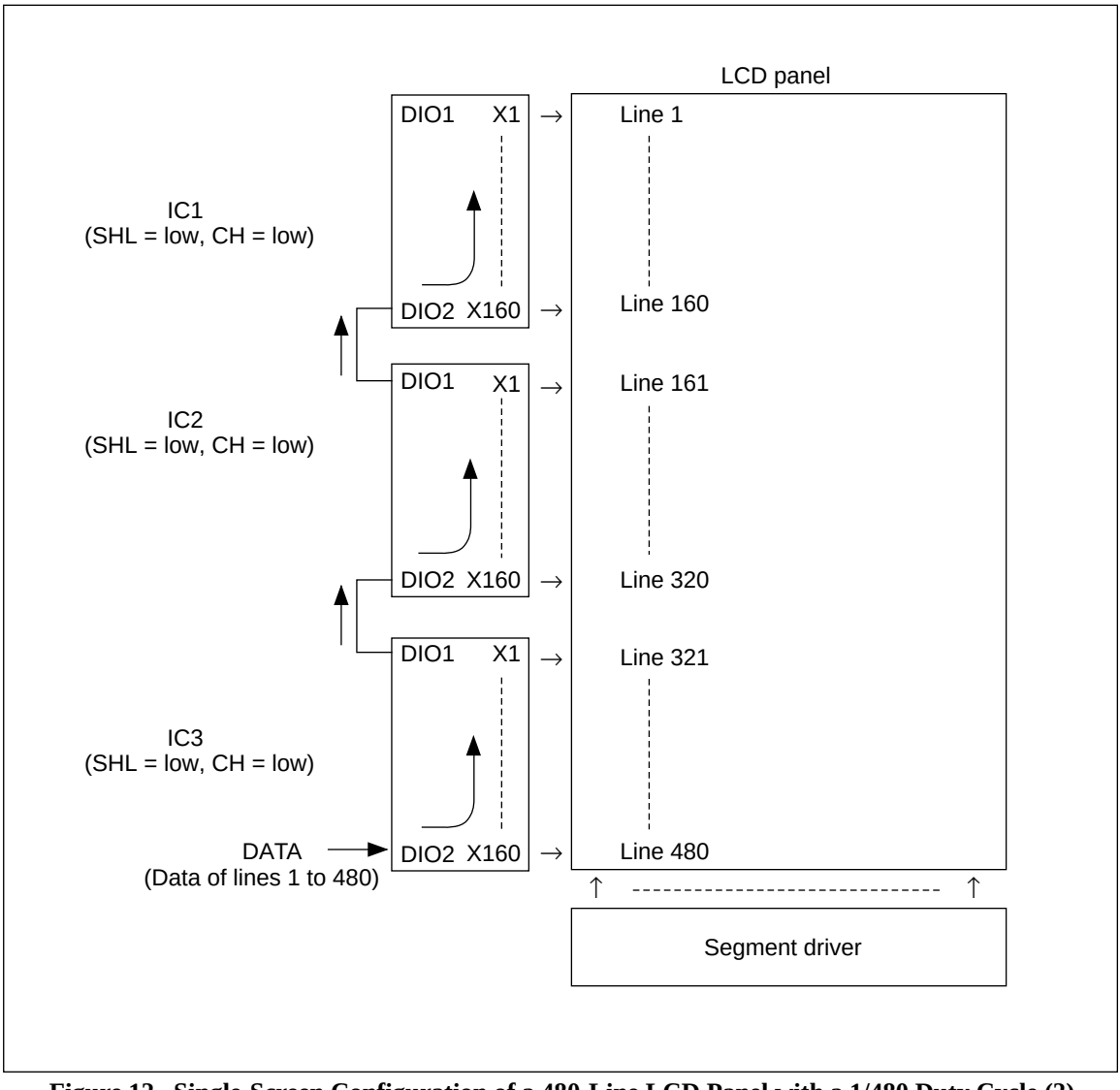


Figure 12 Single-Screen Configuration of a 480-Line LCD Panel with a 1/480 Duty Cycle (2)