PIP PLUS
Analog-Digital-Interface for Inserted Picture

SDA 9187 X

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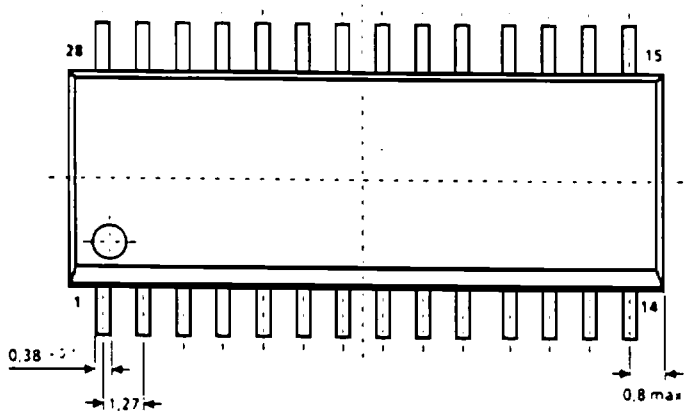
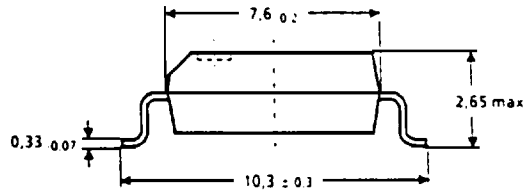
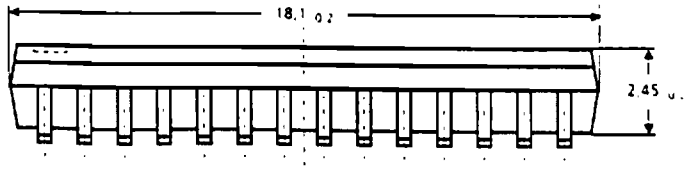
The 9187 X converts the analog output signals Y, U, V of any colour decoder into the digital input signals of the PIP PLUS Processor SDA 9188 X. A clock generator which is synchronized to the sync signals of the insert channel is integrated on this chip.

- 3 separate A/D converters
- 6Bit resolution
- PLL on chip
- Clipping switch for input signals
- Adjustable delay for luminance signals (9 steps)
- Color difference signals (Y, V) can be inverted.

Type	Ordering Code	Package
SDA 9187 X	Q67100-H5076	P-DSO-28







Plastic package, P-DSO-28
20 B 28 DIN 41866
28 pins, DIP

Functional Description and Application

The 9187 X converts the analog output signals Y, U, V of any colour decoders into the digital input signals of the PIP PLUS Processor SDA 9188 X. A clock generator which is synchronized to the sync signals of the insert channel is integrated on this chip.

At the input for the channel of the inset picture an analog CVBS signal is required. An analog operating chroma decoder as well as a sync processor are generating the analog luminance- and chrominance signals Y, U, V and the horizontal and vertical sync signals of the inset picture.

Y, U and V are digitized by 6 bit two step flash converters and output in a format that matches the interface of the PIP processor. Furthermore, with the aid of PLL, the SDA 9187 X generates the line locked clock LL3 (norm 13,5 MHz) and the blanking signal BLN.

Circuit Description

The luminance signal Y and the chrominance signals U, V are fed to the SDA 9187 X by means of coupling capacitors. The colour subcarrier must be filtered out of Y.

The three signals components are digitized by 6-Bit-A/D flash converters; the sampling rate is determined by LL3.

The dynamic range of the converter is given by the two limit values V_{REFL} and V_{REFH}

The black level of Y is clamped to VREFL. The Luminance information is generated as a 6 bit binary offset code.

To compensate the differenttime delay in the luminance and the chrominance processing stages it is possible to delay the digitized luminance information. The time delay can be adjusted in steps of the duration of 2 LL3 periods. The possible range is equal to 0 up to 15 LL3 periods (nominal 0 to 1,11The setting is done using the pins YDO, YD1 and YD2.

The white level of U and V is clamped to 0,5 x (VREFH + VREFL). U, V are then converted into a 6-bit two's complement code

The digitized U, V signals can be inverted via the CNEG control input. A multiplexer selects every fourth U, V sample and applies this 10-bit information in four clock cycles in a nibble format to pins UV (0:3).

The horizontal PLL, consisting of a horizontal timer, phase comparator and VCO, generates the line-locked Picture-in-Picture system clock LL3 and the internal chip timing.

The horizontal timer divides the LL3 clock by 864 (the same for PAL and NTSC) and applies this signal as a horizontal reference signal to the phase comparator. The external horizontal signal is decoded from the sandcastle signal and matched in its pulse width (= 345 LL3 cycles) to the reference signal. The digital phase comparator is frequency- and phase-sensitive and produces current pulses at its output. The up/down pulses of the phase comparator are filtered on pin RC. The filtered signal is the control voltage of the VCO. The horizontal timer also determines the start time and the width of the clamping pulse as well as the location of the blanking signal BLN, which in turn defines the horizontal duration of the picture information on the Y output and should be synchronous with it. BLN is consequently delayed to the same degree as Y.

Maximum Ratings

Maximum ratings are absolute ratings; exceeding just one of these values may cause irreversible damage to the integrated circuit. The proper functioning of the IC cannot be guaranteed for any conditions other than those described under "Operating conditions". Prolonged operation with maximum ratings, i.e. outside the actual operating range, can have an adverse effect on the reliability of the integrated circuit.

(All voltage values relative to V_{PP})

Pos.	Maximum rating for T_{amb} = 0 to 70 °C	Symbol	Min	Max	Dim	Remarks
1	Supply voltage	VDD VDDA	- 0.3 - 0.3	+ 6 + 6	V V	
2	Voltages at I/O pins	Vin	- 0.3	+ 7	V	
3	Voltages differences between Vrefh and Vrefl	DVref	- 4	+ 4	V	
4	Ambient temperature	Tamb	- 20	+ 70	C	
5	Storage temperature	Ts	- 20	+ 125	C	
6	Power dissipation	Ptot		0.8	W	

Range of functions

Within the functional range, the integrated circuit operates as described; deviations from the characteristic data are possible

Pos.	Functional range	Symbol	Min	Max	Dim	Remarks
1	Supply voltage	VDD	4.5	5.5	V	
		VDDA	4.5	5.5	V	
2	Ambient temperature	Tu	0	70	°C	
3	Reference voltge	Vrefh	1.5	2.5	V	
		Vrefl	0.5	1.5	V	
4	Reference voltage difference	Vrefh-Vrefl	0.5	2	V	

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at t_{amb} = 25°C and the listed supply voltage.

All voltage values relative to V_{PP})

Pos.	Parameter	Symbol	Test conditions	Test circuit	Min	Typ	Max	Dim
	Supply voltages							
		VDD			4.5	5	5.5	V
		VDDA			4.5	5	5.5	V
	Current consumption	IDD total				100	120	mA
	Digital outputs YO (0:5), UV (0:3), BLN, LL3							
	Load capacitance	Cl			0		20	pF
	Low level	VQL	IQL = 1.6 mA		0	-	0.4	V
	High level	VQH	IQH = -0.2 mA		2.4		VDD	V
	Delay to the negative transition of LL3							
	Delay	td	LL3 = VQL				14	ns
	LL3 Pulse form							
	Rise Time	tll3r	see Fig. 11		0		7	ns
	Fall Time	tll3f	see Fig. 11		0		5	ns
	H-Pulse width	tll3h	TLL3 = 68 ns		28			ns
	L-Pulse width	tll3l	TLL3 = 68ns		28			ns
	LL3-Period duration	TLL3	see Fig. 11		68<	74	<80.6	ns

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(All voltage values relative to V_{PP})

Pos.	Parameter	Symbol	Test conditions	Test circuits	Min	Typ	Max	Dim
	Digital Inputs							
	CNEG:							
	Low level	VCNL					0.8	V
	High level	VCNH			2.0			V
	Input current	ICN	VCNH = 5V				30	µA
	YD (0,1,2):							
	Low level	VYDL					0.8	V
	High level	VYDH			4.0			V
	Input current	IYD	VYDH = 5V				30	µA

Characteristics

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(All voltage values relative to V_{PP})

Pos.	Parameter	Symbol	Test conditions	Test circuits	Min	Typ	Max	Dim
	<u>Sandcastle Input ISC</u>							
	Switching threshold for VHSC High level				0.6VDD -0.3V	0.6VDD	0.6VDD +0.3V	
	Input current	ISC	VSCH = 5V VSCL = 0V		-1µA		1µA	
	<u>VCO</u>							
	Frequency range:				<12.7	13.5	>14.3	MHz
			VRC = 1.0V VDD = 4.5V Tamb = 0°C		<12.7			MHz
			VRC = 4.3V VDD = 5.5V Tamb = 70°C				>14.3	MHz
	<u>PLL loop filter</u> (recommended value):							
	R 1			see		56		kΩ
	C1			applica-		56		nF
	C 2			tion circuit		1		nF

Design of the loop filter network of the PLL see page 18.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $t_{amb} = 25°C$ and the listed supply voltage.

(All voltage values relative to V_{PP})

Pos.	Parameter	Symbol	Test conditions	Test circuits	Min	Typ	Max	Dim
	Input capacitance	Cin				5		pf
	Leakage current at YIN						100	nA
	UIN, VIN						100	nA
	Start of the clamping pulse refer to the transmission of the horizontal ISC pulse	tk				1.4 *		µs
	Clamping pulse duration	tkd				0.666 **		µs
	Coupling capacitor for YIN, UIN, VIN	Cu, Cv, Cy				10		nF

* (= 19 LL3 period)
** (= 9 LL3 period)

Characteristics

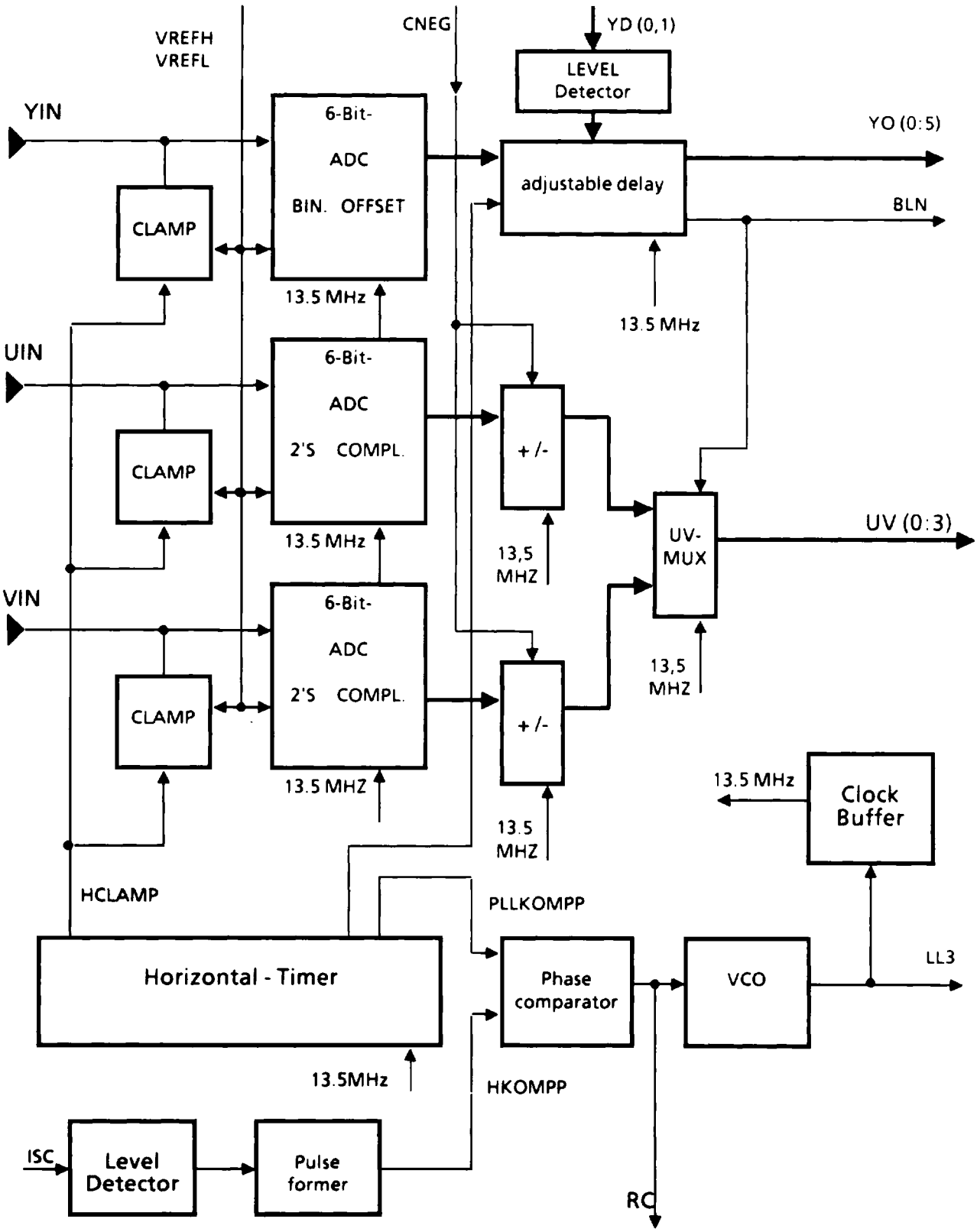
The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at t_{amb} = 25°C and the listed supply voltage.

(All voltage values relative to V_{PP})

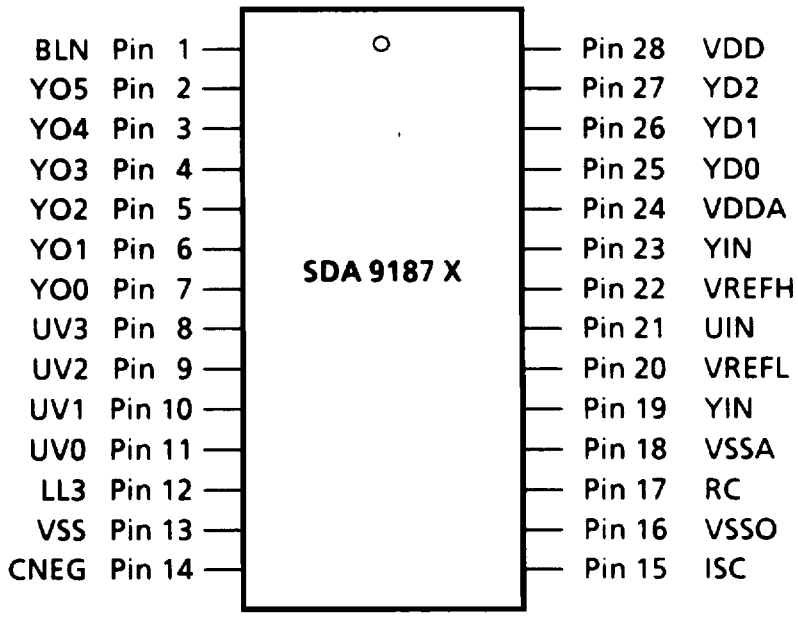
Pos.	Parameter	Symbol	Test condition	Test circuit	Min	Typ	Max	Dim
	Dynamic range of the converter							
	Y - converter				0	...	63	
	U - converter				-31	...	+ 31	
	V - converter				-31	...	+ 31	
	DC-Transfer function of the A/D converter							
	integral non-linearity*		VREFH = 2.0V VREFL = 1.0V			+/-	1 LSB	
	differential non-linearity*					+/-	0.5 LSB	
	Reference Voltage VREFH, VREFL							
	Current consumption	IREFH			4.8	6.0	7.2	mA
		IREFL	VREFH - VREFL = 1V		-4.8	-6.0	-7.2	mA
	VREFH				1.5	2.0	2.5	V
	VREFL				0.5	1.0	1.5	V

* The absolute tolerance of the coupling level and the converter characteristic line are not influenced by the difference VREFH-VREFL (dynamic range of the converter) which lead to big errors by VREFH-VREFL < 1 V.

Block Diagram



Pin Configuration



DSO 28- PACKAGE

Pin Function

Description of the pins

Pin		Function
1	BLN	Blanking-Signal-Output
2 - 7	YQ (5 : 0)	Digital Y output signal (Index 0 = LSB)
8 - 11	UV (3 : 0)	Digital Chrominance signal (Nibble-format nach Bild 10)
12	LL3	Output of the line locked system clock (nom. 13.5 MHz)
13	VSS	Digital ground
14	CNEG	Color negated. By H level the chrominance signals are multiplied by -1 and are output. No wiring = H level
15	ISC	Input for the sandcastle synchronous signal of the gate signal
16	VSSO	VSS connection for the oscillator
17	RC	Pin to the analog loop filter connection of the PLL
18	VSSA	Analog ground
19	VIN	Analog input for the Y signal

20	VREFL	Low reference voltage for the A/D converter
21	UIN	Analog input for the U signal
22	VREFH	High reference voltage for the A/D converter
23	YIN	Analog input for the Y signal
24	VDDA	Analog 5V supply voltage
25, 26,27	YD0,YD1,YD2	To adjust the Y delay no connection = L- level
28	VDD	Digital 5V supply voltage

Reference circuit

For the normal mode - Input signal at Y, U, V = $1V_{SS}$, an internal voltage generator is designed (see Fig. 1).
For all the other modus with input signals bigger or smaller than $1V_{SS}$ the adjustment of the reference range can be done via an external resistor circuit (see Fig. 2,3).

Fig. 1

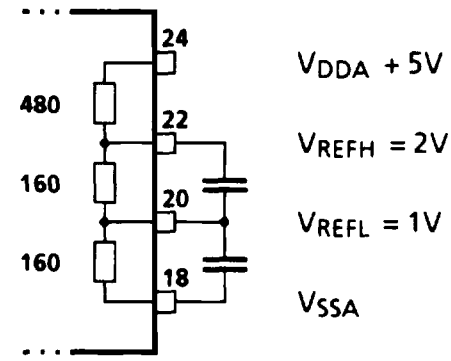
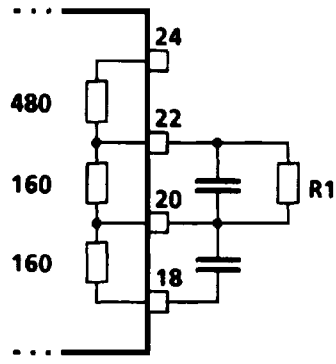
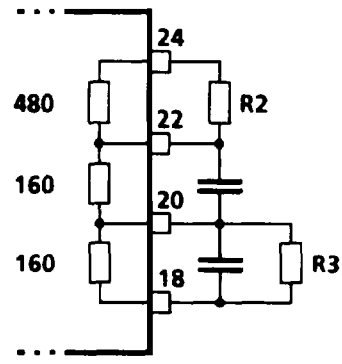


Fig. 2



Example: R1 = 128Ω
$V_{REFH} - V_{REFL} = 0.5V$

Fig. 3



Example: R2 = 342.8Ω
R3 = 53.3Ω
$V_{REFH} - V_{REFL} = 2V$

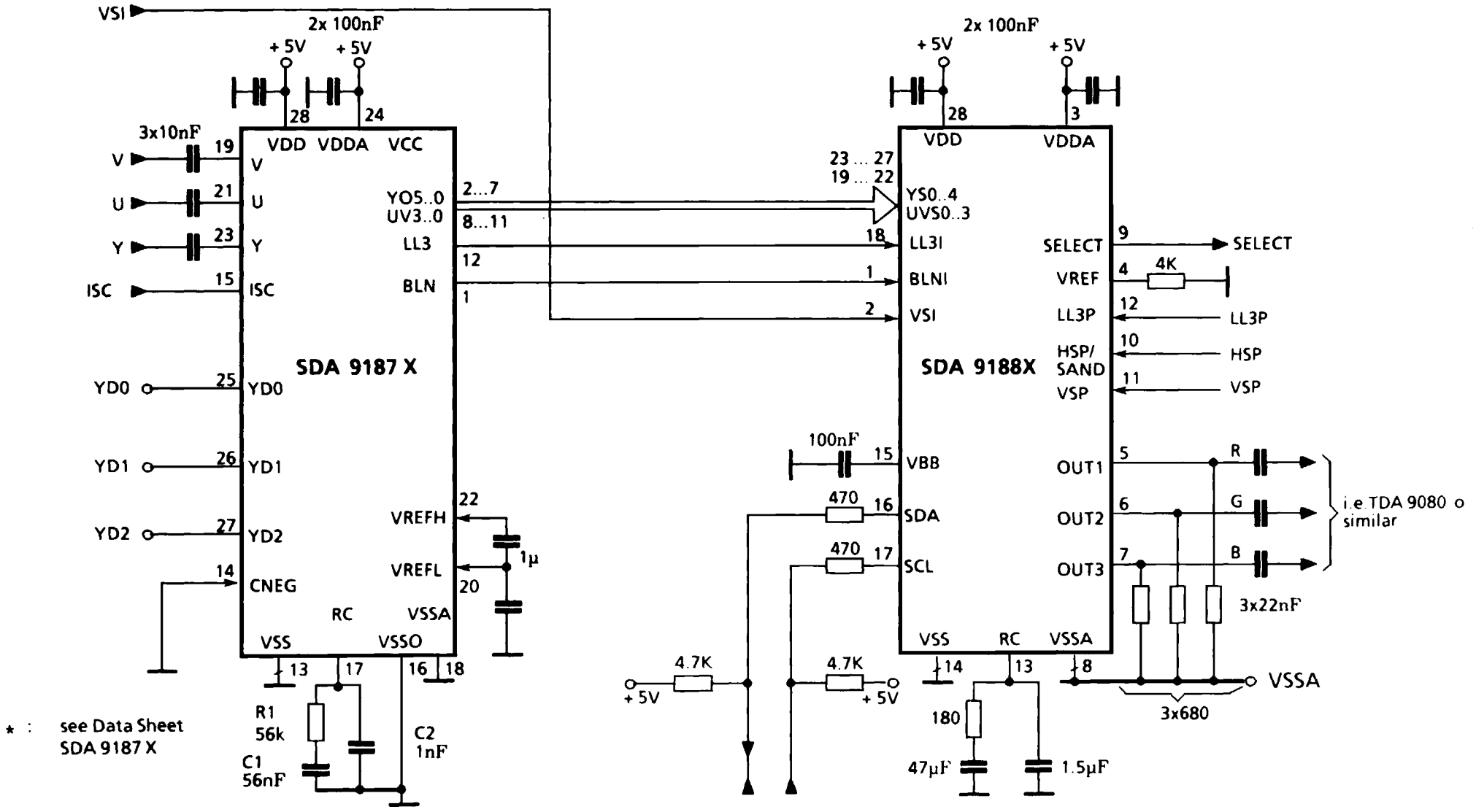
Clamping

Every analog input (YUV) has an internal clamping circuit. The analog inputs YIN, UIN, VIN are clamped to internal generated clamping levels. The required clamping signals are generated internally.

Clamping level

Analog signal	dual Code
Y_{IN}	000000
U_{IN}, V_{IN}	100000

The external clamping capacitor (typ. 10nF) is precharged by means of internal curent sources to the required clamping level. The duration of the charging process is 9 clock cycles in every line of the TV signal.



Application Circuit

Remark regarding the RC Network of the PLL

For the calculation of the control response the following formulas can be used:

Characteristic circuit frequency: $\omega_0 = (K/C1)^{0.5}$
Damping factor: $\zeta = 0{,}5 \cdot R \cdot (K \cdot C1)^{0.5}$

K = 0,46 typical
K = 0,73 maximum

The parallel capacity C2 should not exceed 5% of C1.

Because of the time discrete sampling of the phase differences every 64µs the loading behavior of the PLL is affected by modulation with one half of the line frequency.
In order to clamp this phase modulation sufficiently the extend resistor R1 connected to SDA 9187 X has to fulfill the following equation:

$$1.74 > R1 \times 47 \times 10^{-6} \times 1/\Omega \times (1\text{-}2/(1 + e^{\alpha}))$$

with

$$\alpha = 64\mu s / R1 \times C2$$

or approximately by $R1 \times C2 << 64\mu s$

$$1{,}74 > R1 \times 47 \times 10^{-6} \times 1/\Omega$$

For the layout of the printed board it is important:

a) to connect bypass capacitors close to the supply pins of the IC
b) to have short connections for the capacitor C2

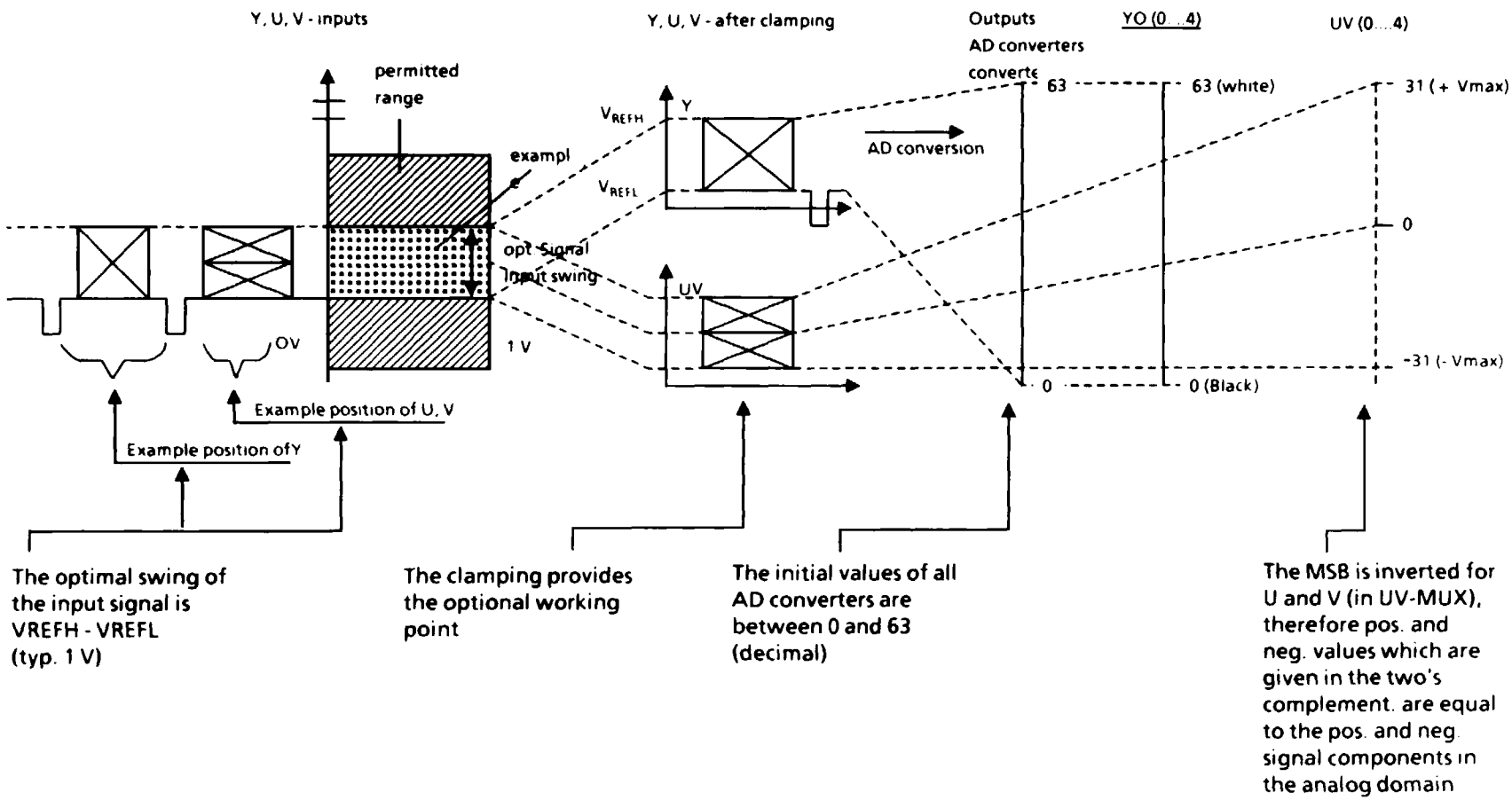
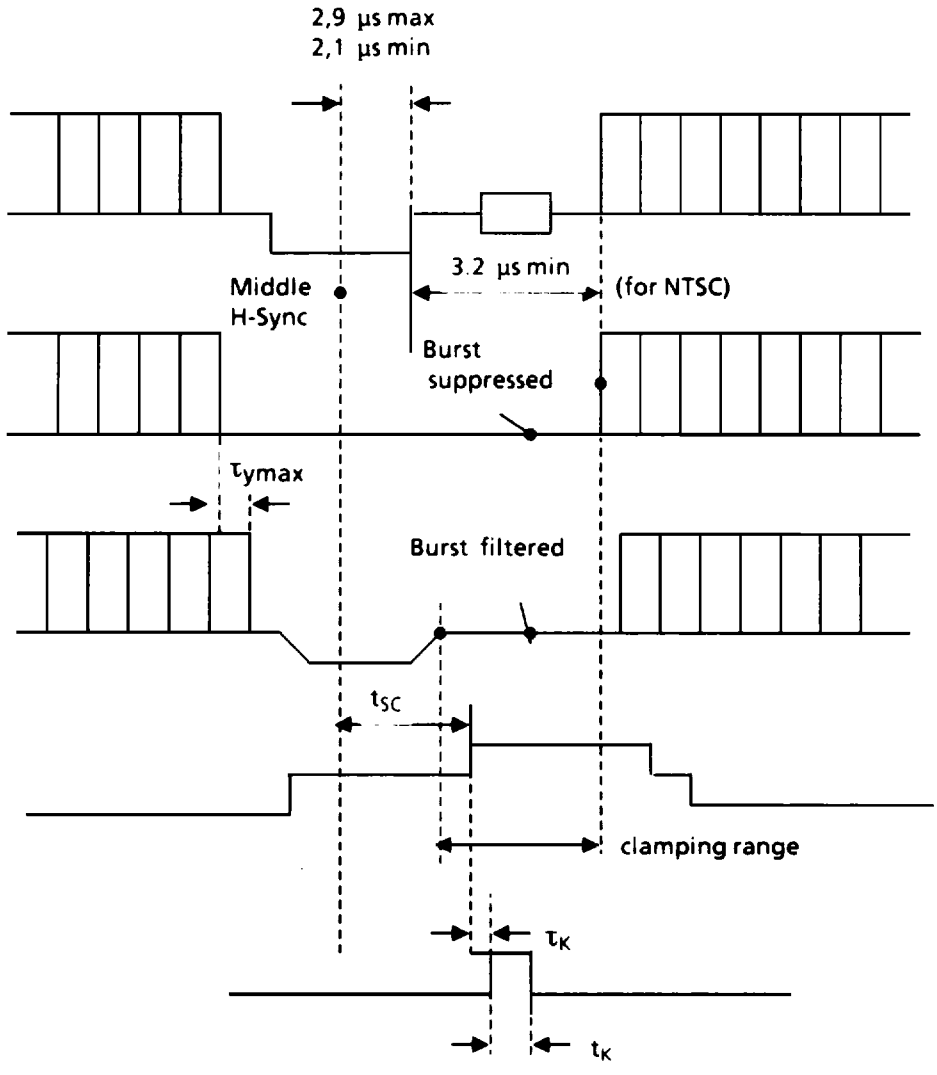


Figure 6: Input voltage range Y, U and V and their translation in initial values ("Digital Values")

Diagrams

Diagrams



Leading edge at clamping pulse:

$t_{SCmin} + \tau_K > 2.9\ \mu s + \tau_K \approx 4{,}3\ \mu s$

chosen: $\tau_K = 1.4\ \mu s$ (19 LL3 clocks)

Tailing edge at clamping pulse

$t_{SC\,max} + \tau_K + t_K < 5.3\ \mu s = 3.2\ \mu s + 2.1\ \mu s$

chosen: $t_K = 0.666\ \mu s$ (9.0 LL3 clocks)

Figure 7: Clamping Pulse Timing

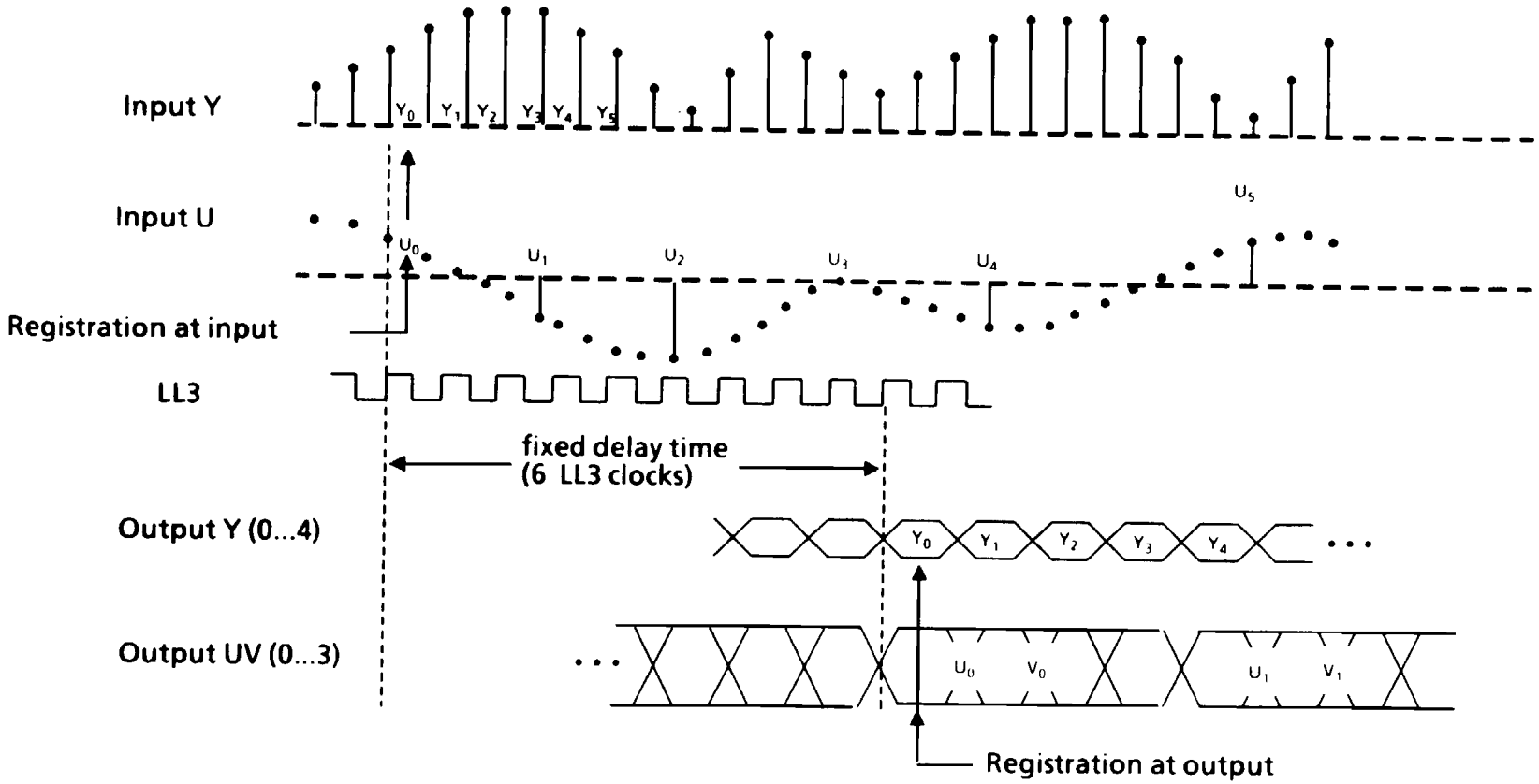
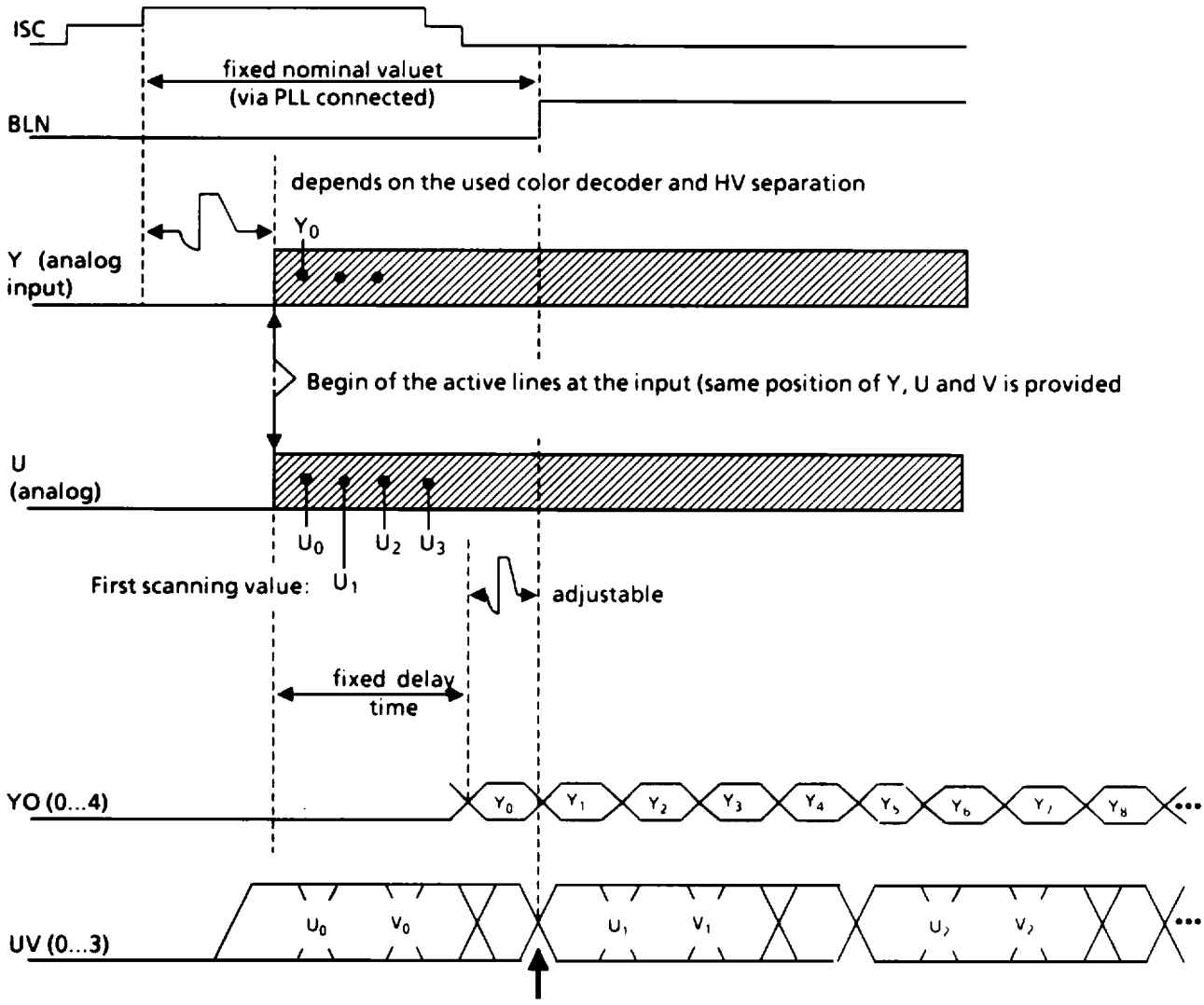


Figure 8: Signal Delay Time for U, V and Y (used indication: number of scanning values). Additionally programmable delay time in DELAY-Block-0.

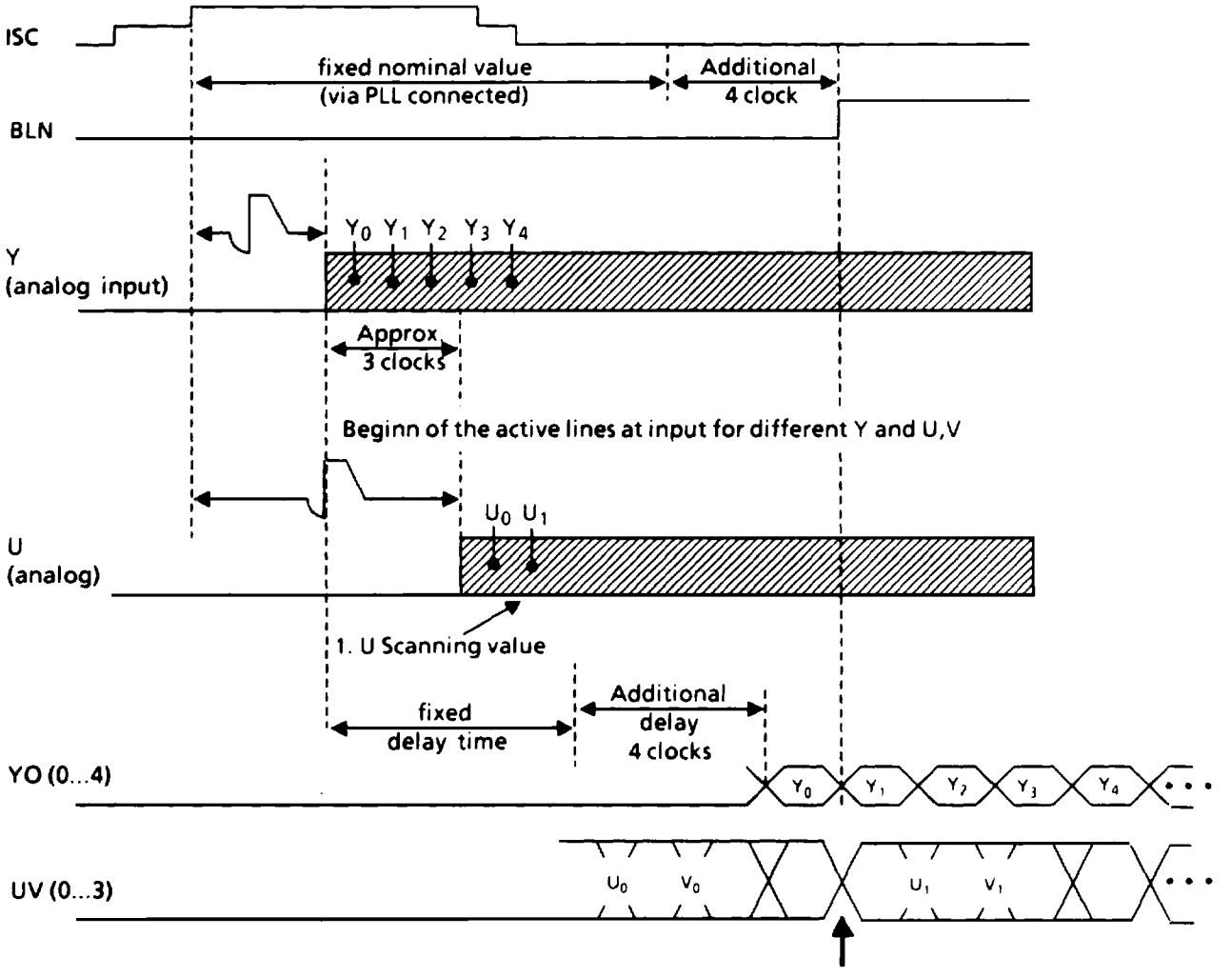
Diagrams



- Y, U, V have no delay time differences
- Delay between SC and Y, U, V is smaller than provided for the optional case.

Figure 9 a: Relation between SC, BLN and Y and UV (used indication: number of pixels)

Diagrams



U,V are delayed approx. 3 LL3 clocks compare to Y;
Compensation through an additional Y-delay of 4 clocks

- BLN edge and raster correspond to each other;
- Begin of the active lines of YO (0...4) and UV (0...3) is moved
- Registration errors still 1 clock (Y-value 1 clock to late, because of 4 clocks delay, U-delay but only 3 clocks

Figure 9 b: Relation between SC, BLN and Y and UV (used indication: number of pixels)

Diagrams

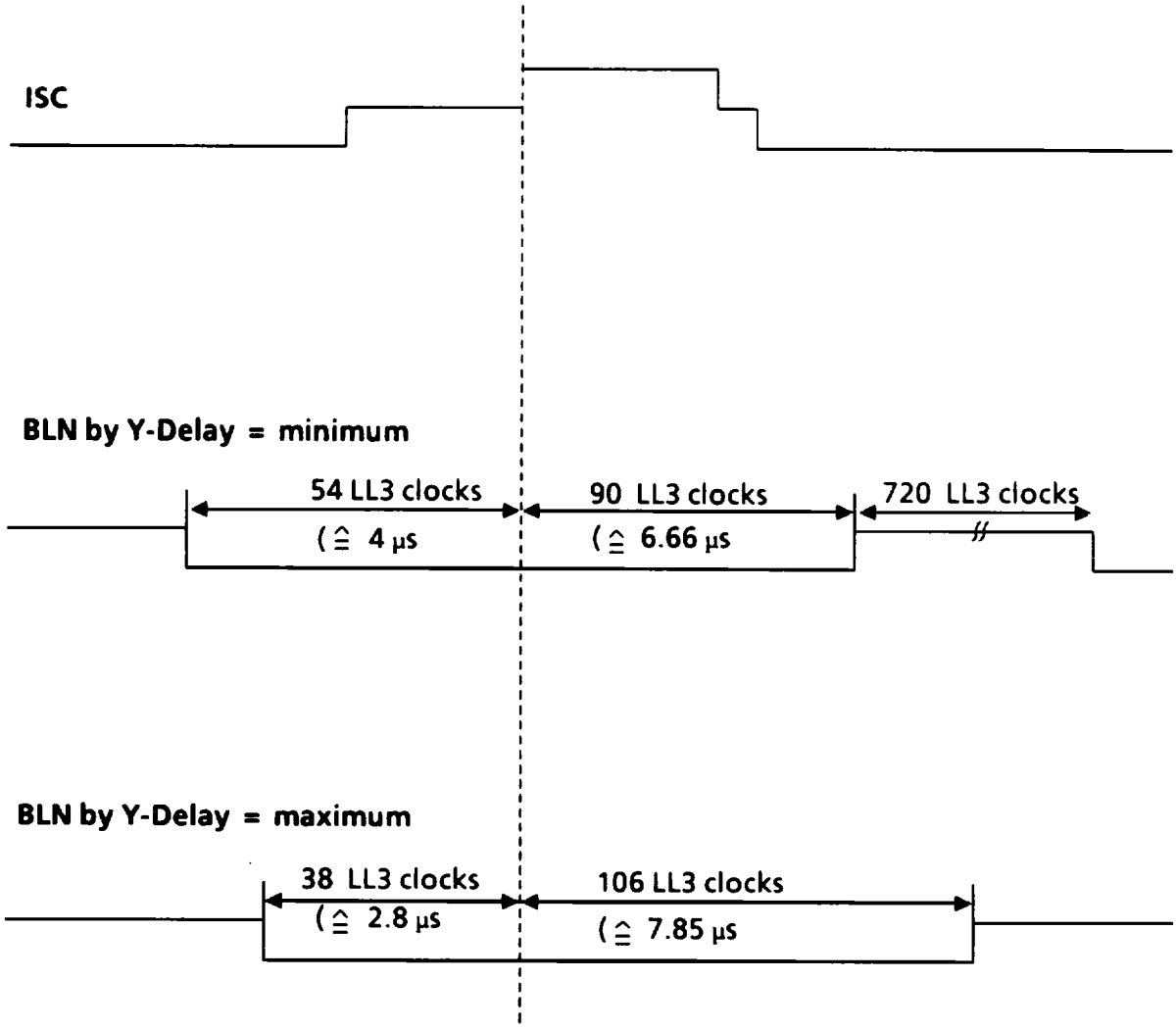


Figure 9 c: **Relation between SC and BLN**

Diagrams

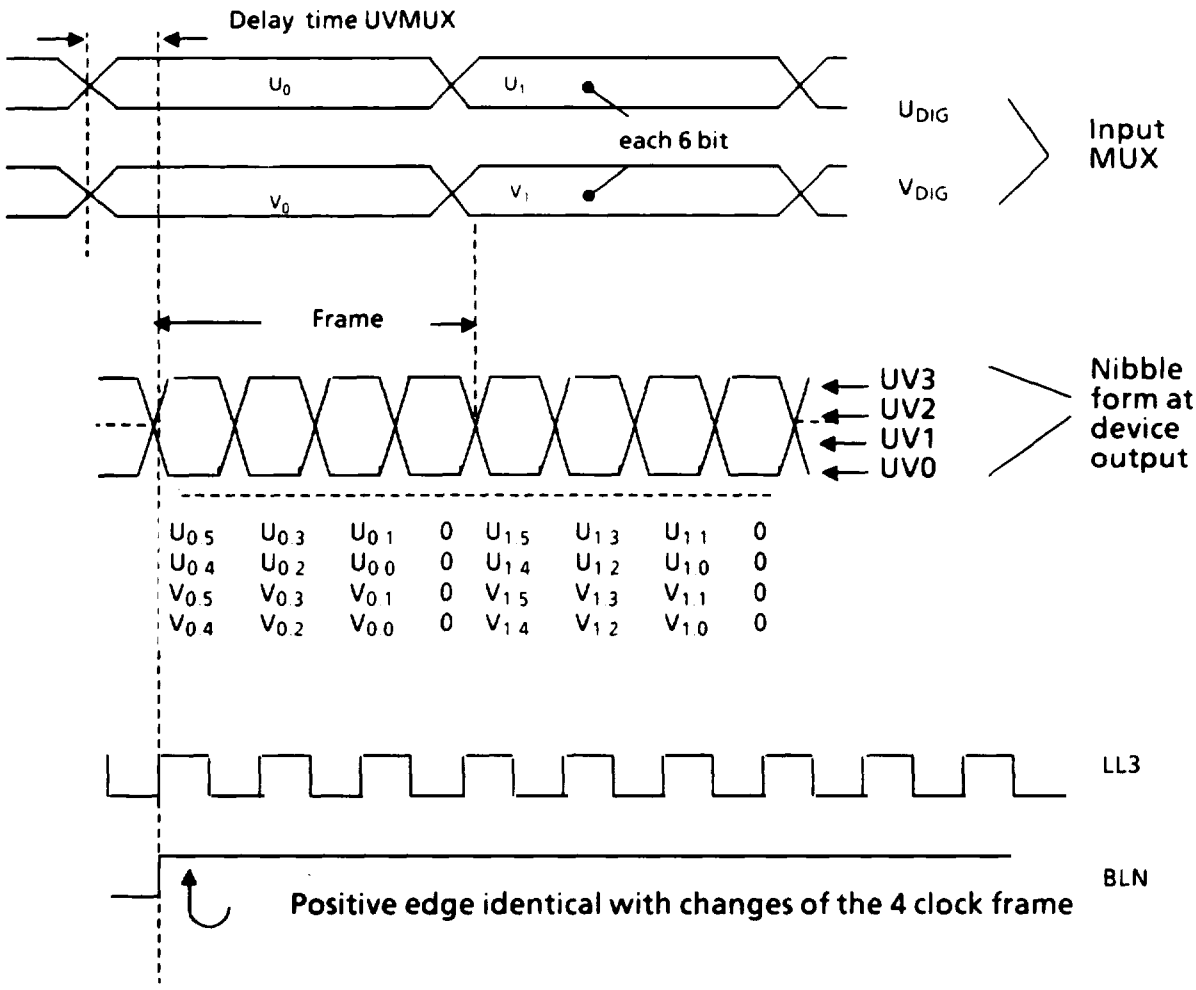


Figure 10

Conversion of U and V in a Nibble Form with 13,5 MHz, 4 bit

it means: 1. Index: number of scanning value (pixels)
2. Index: number of bits; 5 = MSB

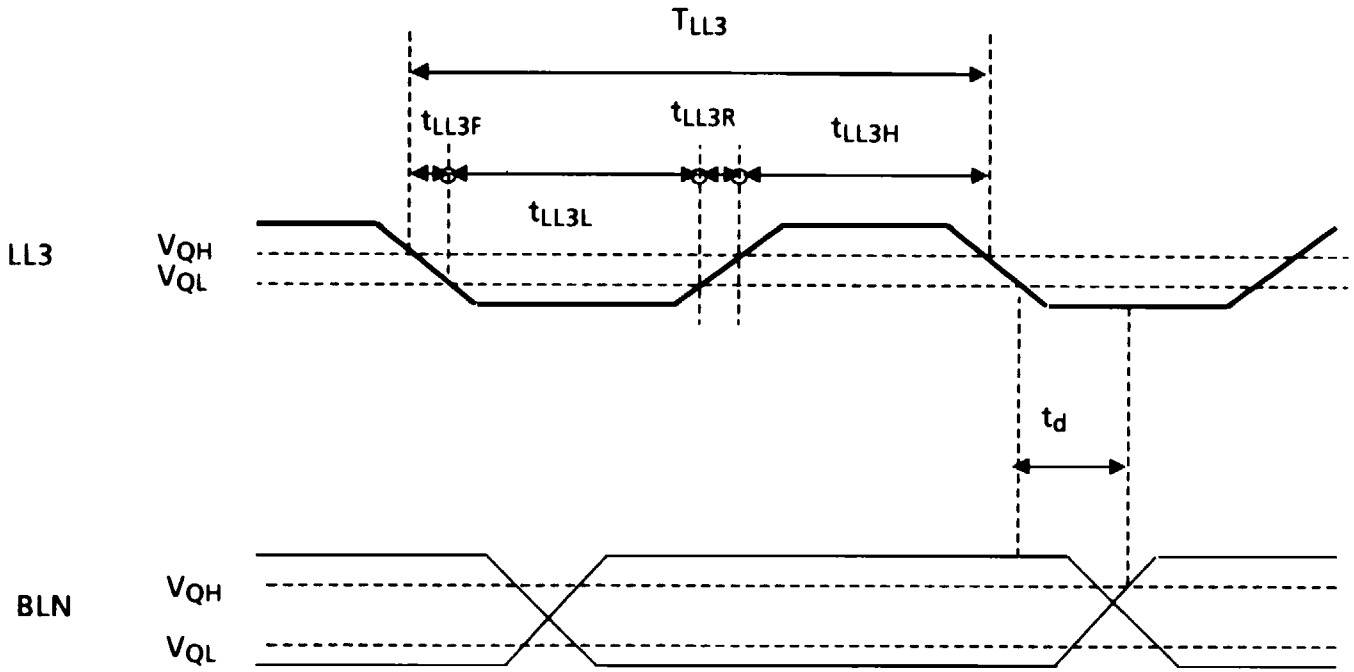


Figure 11 Specification of Edges

Diagram

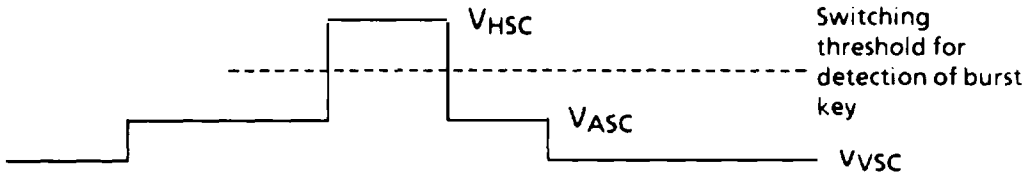


Figure 12:

Sandcastle Pulse

Level Range			Additional Delay for Y and BLN	
Pin YD2	Pin YD1	Pin YD0	LL3 clocks :	typ. value :
0	0	0	0	0
0	0	1	2	148 ns
0	1	0	4	296 ns
0	1	1	6	444 ns
1	0	0	8	592 ns
1	0	1	10	740 ns
1	1	0	12	888 ns
1	1	1	14	1,04 µs

Level range:
0 = VYDL
1 = VYDH

Table 1:

Adjusting od Y-Delay via YD0, YD1,YD2

Diagram

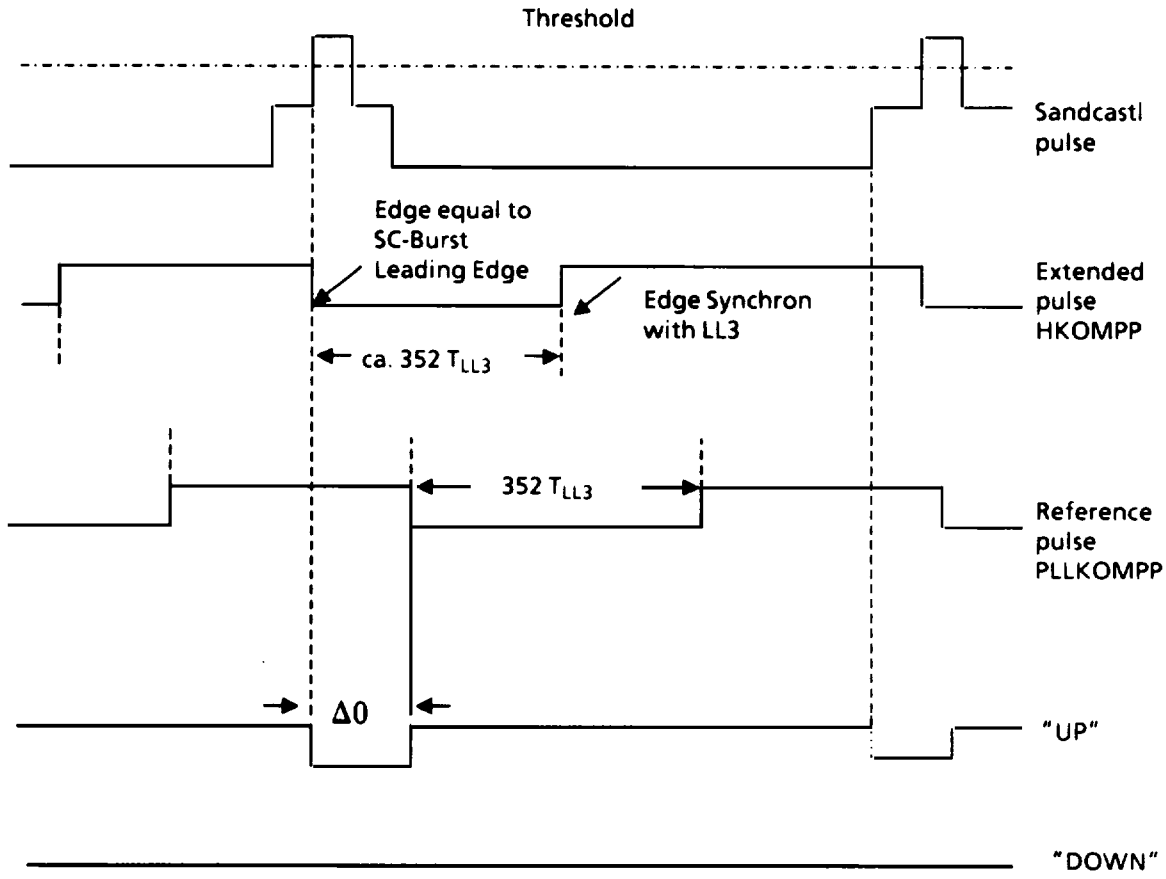


Figure 13

Function of SC Pulse Extention and Phase Comparison (PLL is unlocked, behind the external H phase)