Am6070

Companding D-to-A Converter for Control Systems

Distinctive Characteristics

- Tested to μ-255 companding law
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM, audio, and 8-bit μ-P systems
- Output dynamic range of 72 dB
- 12-bit accuracy and resolution around zero
- Sign plus 12-bit range with sign plus 7-bit coding
- Improved pin-for-pin replacement for DAC-76
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

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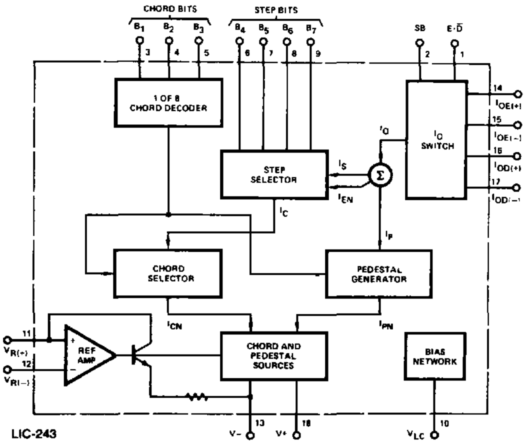
GENERAL DESCRIPTION

The Am6070 monolithic companding D/A converter achieves a 72dB dynamic range which is equivalent to that achieved by a 12-bit converter.

The transfer function of the Am6070 complies with the Bell system μ-255 companding law, and consists of 15 linear segments or chords. A particular chord is identified with the sign bit input, (SB) and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. Accuracy and monotonicity are assured by the internal circuit design and are guaranteed over the full temperature range.

Applications for the Am6070 include digital audio recording, servo-motor controls, electromechanical positioning, voice synthesis, secure communications, microprocessor controlled sound and voice systems, log sweep generators and various data acquisition systems.

FUNCTIONAL BLOCK DIAGRAM



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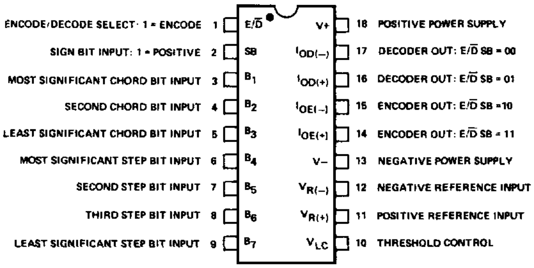
CONNECTION DIAGRAM
D-18-1



Top View
Pin 1 is marked for orientation.

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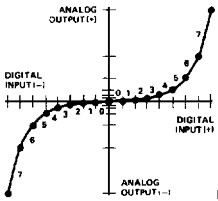
ORDERING INFORMATION*

Part Number	Temperature	Accuracy
Am6070ADM	−55°C to +125°C	±1/2 step
Am6070DM	−55°C to +125°C	±1 step
Am6070ADC	0°C to +70°C	±1/2 step
Am6070DC	0°C to +70°C	±1 step

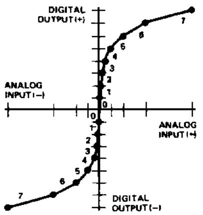
*Also available with burn-in processing. To order add suffix B to part number.

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS

Decoder Characteristic



Encoder Characteristic



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MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leq 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	72 dB, (20 log ($I_{7,15}/I_{0,1}$))

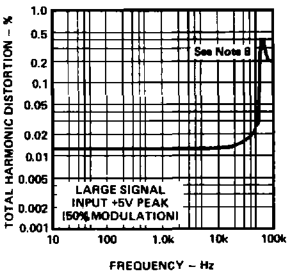
ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = +15V, V− = −15V, I_{REF} = 528μA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, −55°C ≤ T_A ≤ +125C, for the military grade, and for all 4 outputs unless otherwise specified.

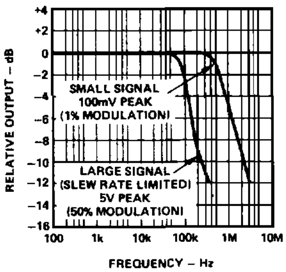
Parameter	Description	Test Conditions	Am6070ADM / Am6070ADC Min.	Typ.	Max.	Am6070DM / Am6070DC Min.	Typ.	Max.	Units
t_s	Settling Time	To within ±1/2 step at T_A = 25°C output switched from I_{ZS} to I_{FS}		300	500		300	500	ns
	Chord Endpoint Accuracy	Guaranteed by output current error specified below.			±1/2			±1	Step
	Step Nonlinearity				±1/2			±1	Step
$I_{FS(D)}$	Full Scale Current Deviation				±1/2			±1	
$I_{FS(E)}$	From Ideal				±1/2			±1	
ΔI_O	Output Current Error	V_{REF} = 10.000V, R_{REF+} = 18.94kΩ, R_{REF-} = 20kΩ, −5.0V ≤ V_{OUT} ≤ +18V, Error referred to nominal values in Table 1.			±1/2			±1	Step
$I_{O(+)}-I_{O(-)}$	Full Scale Symmetry Error	V_{REF} = 10.000V, R_{REF+} = 18.94kΩ, R_{REF} = 20kΩ, −5.0V ≤ V_{OUT} ≤ +18V, Error referred to nominal values in Table 1		1/40 1/40	1/8 1/8		1/20 1/20	1/4 1/4	Step Step
I_{EN}	Encode Current	Additional output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
I_{ZS}	Zero Scale Current	Measured at selected output with 000 0000 input		1/40	1/4		1/20	1/2	Step
ΔI_{FS}	Full Scale Drift	Operating temperature range		±1/20	±1/4		±1/10	±1/2	Step
V_{OC}	Output Voltage Compliance	Full scale current change ≤1/2 step	−5.0		+18	−5.0		+18	Volts
I_{DIS}	Disable Current	Output leakage Output disabled by E/$\overline{D}$ and SB		5.0	50		5.0	50	nA
I_{FSR}	Output Current Range		0	2.0	4.2	0	2.0	4.2	mA
V_{IL}	Logic Input Levels, Logic "0"	V_{LC} = 0V			0.8			0.8	Volts
V_{IH}	Logic Input Levels, Logic "1"	V_{LC} = 0V	2.0			2.0			Volts
I_{IN}	Logic Input Current	V_{IN} = −5.0V to +18V			40			40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5.0		+18	−5.0		+18	Volts
$I_{B\ REF-}$	Reference Bias Current			−1.0	−4.0		−1.0	−4.0	μA
di/dt	Reference Input Slew Rate		0.12	0.25		0.12	0.25		mA/μs
$PSSI_{FS+}$ $PSSI_{FS-}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	V+ = 4.5 to 18V, V− = −15V V− = 10.8 + −18V, V+ = 15V		±1/20 ±1/10	±1/2 ±1/2		±1/20 ±1/10	±1/2 ±1/2	Step Step
I+ I−	Power Supply Current	V+ = +5.0 to +15V, V− = −15V I_{FS} = 2.0mA		2.7 −6.7	4.0 −8.8		2.7 −6.7	4.0 −8.8	mA
P_D	Power Dissipation	V− = −15V, V_{OUT} = 0, I_{FS} = 2.0mA; V+ = 5.0V V+ = +15V		114 141	152 192		114 141	152 192	mW

TYPICAL PERFORMANCE CURVES

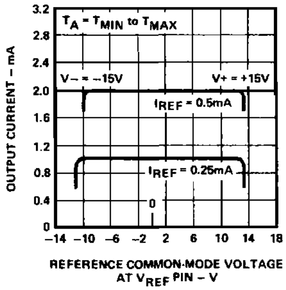
Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)



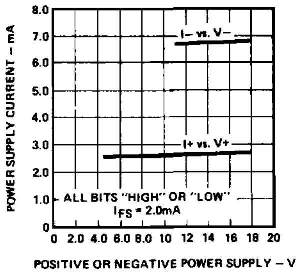
Reference Amplifier Input Frequency Response



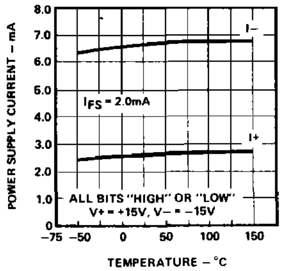
Reference Amplifier Input Common-Mode Range (Note 9)



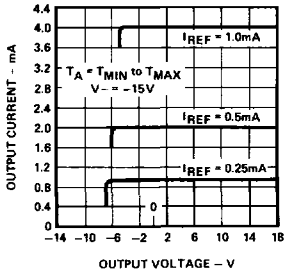
Power Supply Currents Versus Power Supply Voltages



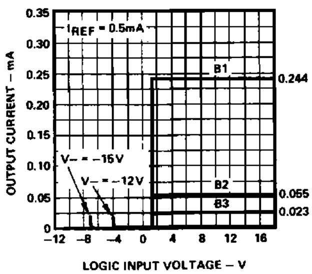
Power Supply Currents Versus Temperature



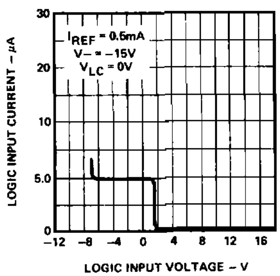
Output Current Versus Output Voltage (Output Voltage Compliance)



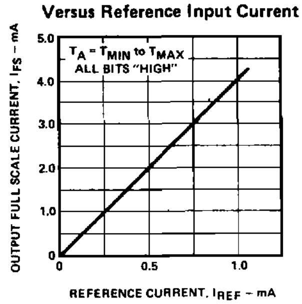
Bit Transfer Characteristics (Note 10)



Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)



Output Full Scale Current Versus Reference Input Current



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Notes:
6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) –1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE 1
NOMINAL DECODER OUTPUT CURRENT LEVELS IN μA

	CHORD							
STEP	0	1	2	3	4	5	6	7
0	.000	8.250	24.750	57.750	123.75	255.75	519.75	1047.75
1	.500	9.250	26.750	61.750	131.75	271.75	551.75	1111.75
2	1.000	10.250	28.750	65.750	139.75	287.75	583.75	1175.75
3	1.500	11.250	30.750	69.750	147.75	303.75	615.75	1239.75
4	2.000	12.250	32.750	73.750	155.75	319.75	647.75	1303.75
5	2.500	13.250	34.750	77.750	163.75	335.75	679.75	1367.75
6	3.000	14.250	36.750	81.750	171.75	351.75	711.75	1431.75
7	3.500	15.250	38.750	85.750	179.75	367.75	743.75	1495.75
8	4.000	16.250	40.750	89.750	187.75	383.75	775.75	1559.75
9	4.500	17.250	42.750	93.750	195.75	399.75	807.75	1623.75
10	5.000	18.250	44.750	97.750	203.75	415.75	839.75	1687.75
11	5.500	19.250	46.750	101.750	211.75	431.75	871.75	1751.75
12	6.000	20.250	48.750	105.750	219.75	447.75	903.75	1815.75
13	6.500	21.250	50.750	109.750	227.75	463.75	935.75	1879.75
14	7.000	22.250	52.750	113.750	235.75	479.75	967.75	1943.75
15	7.500	23.250	54.750	117.750	243.75	495.75	999.75	2007.75
STEP SIZE	.5	1	2	4	8	16	32	64

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM FULL SCALE

	CHORD							
STEP	0	1	2	3	4	5	6	7
0	–	−47.73	−38.18	−30.82	−24.20	−17.90	−11.74	−5.65
1	−72.07	−46.73	−37.51	−30.24	−23.66	−17.37	−11.22	−5.13
2	−66.05	−45.84	−36.88	−29.70	−23.15	−16.87	−10.73	−4.65
3	−62.53	−45.03	−36.30	−29.18	−22.66	−16.40	−10.27	−4.19
4	−60.03	−44.29	−35.75	−28.70	−22.21	−15.96	−9.83	−3.75
5	−58.10	−43.61	−35.24	−28.24	−21.77	−15.53	−9.41	−3.33
6	−56.51	−42.98	−34.75	−27.80	−21.36	−15.13	−9.01	−2.94
7	−55.17	−42.39	−34.29	−27.39	−20.96	−14.74	−8.63	−2.56
8	−54.01	−41.84	−33.85	−26.99	−20.58	−14.37	−8.26	−2.19
9	−52.99	−41.32	−33.44	−26.61	−20.22	−14.02	−7.91	−1.84
10	−52.07	−40.83	−33.04	−26.25	−19.87	−13.68	−7.57	−1.51
11	−51.25	−40.37	−32.66	−25.90	−19.54	−13.35	−7.25	−1.18
12	−50.49	−39.93	−32.29	−25.57	−19.22	−13.03	−6.93	−0.87
13	−49.80	−39.51	−31.95	−25.25	−18.91	−12.73	−6.63	−0.57
14	−49.15	−39.11	−31.61	−24.94	−18.61	−12.43	−6.34	−0.28
15	−48.55	−38.73	−31.29	−24.63	−18.32	−12.15	−6.06	0.00

THEORY OF OPERATION

Functional Description

The Am6070 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, (E/$\overline{D}$), input signal. A logic 1 applied to the E/$\overline{D}$ input places the Am6072 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the E/$\overline{D}$ input places the Am6070 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the Bell System μ-225 logarithmic law which can be written as follows:

$$Y = 0.18 \ln (1 + \mu \ |X|) \ \mathrm{sgn}\ (X)$$

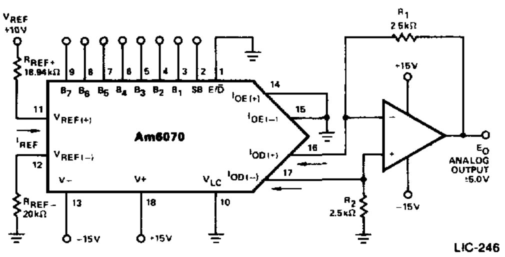
where: X = analog signal level normalized to unity (encoder input or decoder output)
Y = digital signal level normalized to unity (encoder output or decoder input)
μ = 255

The current flows from the external circuit into one of four possible analog outputs determined by the SB and E/$\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of 0.5μA found in the first chord near zero output current, and the largest step of 64μA found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels near zero output current. The accuracy for signal amplitudes corresponding to chord 0 is equivalent to that of a 12-bit linear, binary D/A converter. However, the ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over most of the dynamic range. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at approximately 6dB over most of the dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 72dB output dynamic range for the Am6070 corresponds to the dynamic range of a sign plus 12-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 72dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The E/$\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the E/$\overline{D}$ input is high, (a logic 1), the converter will assume the encode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current,

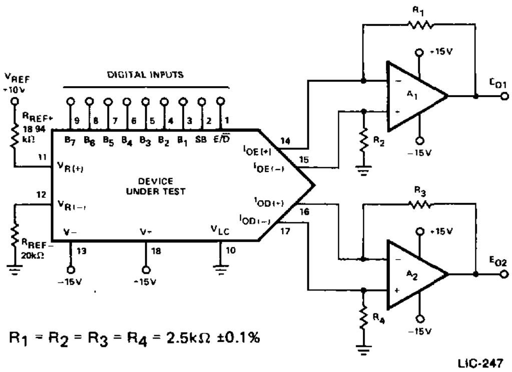


$I_{REF} = V_{REF}/R_{REF}$

IDEAL VALUES: $I_{REF} \approx 528\mu A$, $I_{FS} = 2007.75\mu A$

	E/$\overline{D}$	SB	B_1	B_2	B_3	B_4	B_5	B_6	B_7	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(–) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(–) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	–0.0012V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	–5.019V

Figure 1. Detailed Decoder Connections.



$R_1 = R_2 = R_3 = R_4 = 2.5k\Omega \pm 0.1\%$

LINE SELECTION TABLE

TEST GROUP	E/$\overline{D}$	SB	OUTPUT MEASUREMENT	
1	1	1	I_{OE} (+)	(E_{01}/R_1)
2	1	0	I_{OE} (–)	(E_{01}/R_2)
3	0	1	I_{OD} (+)	(E_{02}/R_3)
4	0	0	I_{OD} (–)	(E_{02}/R_4)

Figure 2. Output Current DC Test Circuit.

I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by 32μA. Similarly, the current levels in the first chord near the origin will be offset by 0.25μA, which will bring the ideal encode current value for step 0 on chord 0 to ±0.25μA with respect to the corresponding decode current value of 0.0μA. This additional encode half step of current can be used for extension of the output dynamic range from 72dB to 78dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the E/$\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6070 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper Start, $\overline{S}$, and Conversion Complete, $\overline{CC}$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the E/$\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the E/$\overline{D}$ input back to a logic 1 level because the $\overline{CC}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6070. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6070.

Nine total clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6070 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6070 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6070. The resulting operational amplifier's output in Figure 1 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6070 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately 2μA at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA, respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of

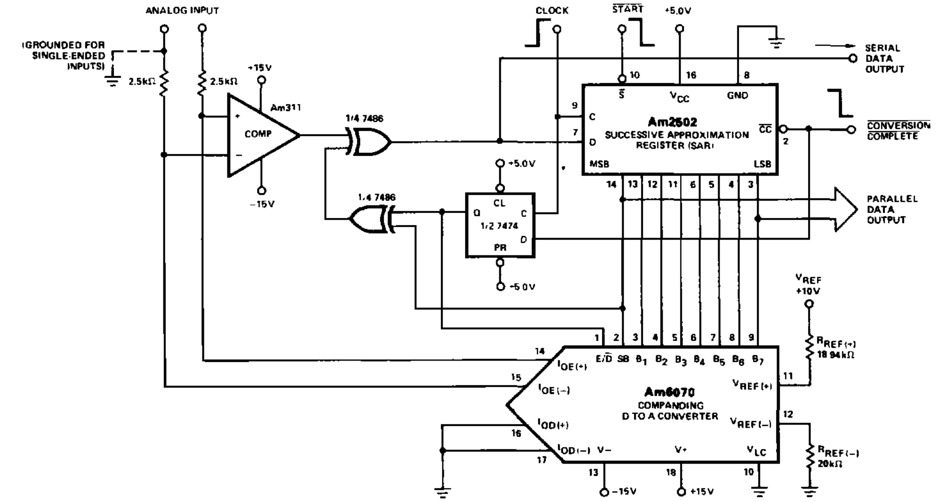


Figure 3. Detailed Encoder Connections.

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2.5kΩ, also contribute to the output measurement error by a factor of 400nA for every mV of offset at the A1 and A2 outputs. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.8\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistors values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, (I−), and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is 528µA. The corresponding ideal full scale decode and encode current values are 2007.75µA and 2039.75µA, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, V+, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of 0.01µF. The total resistor value should provide the reference current I_{REF} = 528µA. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6070 has a wide output voltage compliance suitable for driving a variety of loads. With I_{REF} = 528µA and V− = −15V, positive voltage compliance is +18V and negative voltage compliance is −5.0V. For other values of I_{REF} and V−, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + (2 \cdot I_{REF} \cdot 1.5k\Omega) + 8.4V.$$

The following table contains $V_{OC(-)}$ values for some specific V−, I_{REF}, and I_{FS} values.

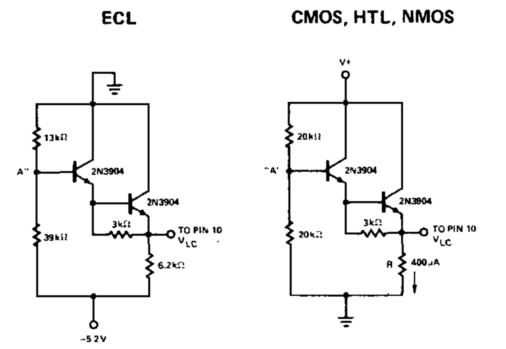
Negative Output Voltage Compliance $V_{OC(-)}$

V− \ I_{REF} (I_{FS})	264µA (1mA)	528µA (2mA)	1056µA (4mA)
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6070 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen V− value and +10V.

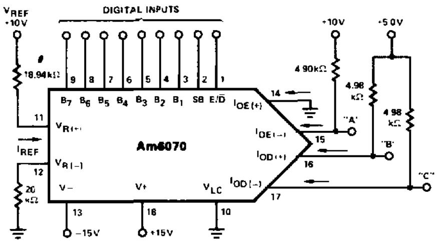
With a V− value chosen between −15V and −11V, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− value chosen.

With a V+ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the V+ value chosen.



(See Notes 2 and 3)

Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs. LIC-249



INPUT CODE (E/$\bar{D}$, SB, B_1, . . ., B_7)	OUTPUT VOLTAGE (V) "A"	"B"	"C"	DIFF
10 111 1111	0	N/A	N/A	N/A
10 110 1111	−5.02			
10 000 0000	+10.00			
01 111 1111	N/A	−5.00	+5.00	−10.00
01 110 1111		+0.02	+5.00	−4.98
01 000 0000		+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections. LIC-250

Notes: 2. Set the voltage "A" to the desired logic input switching threshold.
3. Allowable range of logic threshold is typically −5V to +13.5V when operating the companding DAC on ±15V supplies.

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

Step (S)	Chord (C)	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
Step Size		2	4	8	16	32	64	128	256

The normalized decode current, ($I_{C,S}$), is calculated using:

$$I_{C,S} = 2(2^C(S + 16.5) - 16.5)$$

where C = chord number; S = step number. The ideal decode current, (I_{OD}), in μA is calculated using:

$$I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \cdot I_{FS}\ (\mu A)$$

where $I_{C,S}$ is the corresponding normalized current. To obtain normalized encode current values the corresponding normalized half-step value should be added to all entries in Table 3.

Table 4
Normalized Encode Level (Sign Bit Excluded)

STEP	CHORD	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
Step Size		2	4	8	16	32	64	128	256

$$I_{C,S} = 2[2^C(S+17) - 16.5]$$

C = chord no. (0 through 7)
S = step no. (0 through 15)

ADDITIONAL DECODE OUTPUT CURRENT TABLES (Cont.)

Table 5
Decoder Step Size Summary

Chord	Step Size Normalized to Full Scale	Step Size in μA with 2007.75μA FS	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	0.5	0.025%	0.60	6.67%	Sign + 12 Bits
1	4	1.0	0.05%	0.38	4.30%	Sign + 11 Bits
2	8	2.0	0.1%	0.32	3.65%	Sign + 10 Bits
3	16	4.0	0.2%	0.31	3.40%	Sign + 9 Bits
4	32	8.0	0.4%	0.29	3.28%	Sign + 8 Bits
5	64	16.0	0.8%	0.28	3.23%	Sign + 7 Bits
6	128	32.0	1.6%	0.28	3.20%	Sign + 6 Bits
7	256	64.0	3.2%	0.28	3.19%	Sign + 5 Bits

Table 6
Decoder Chord Size Summary

Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2007.75μA FS	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	30	7.5	0.37%	−48.55
1	93	23.25	1.16%	−38.73
2	219	54.75	2.73%	−31.29
3	471	117.75	5.86%	−24.63
4	975	243.75	12.1%	−18.32
5	1983	495.75	24.7%	−12.15
6	3999	999.75	49.8%	−6.06
7	8031	2007.75	100%	0

APPLICATIONS

The companding D/A converter is particularly suited for applications requiring a wide dynamic range.

Systems requiring fine control resulting in a constant rate of change or set point controls are economically achieved using these devices.

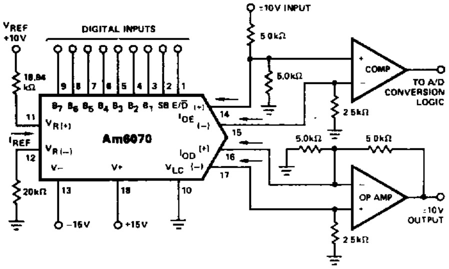
Instrumentation, Control and μ-Processor based applications include:
- Digital data recording
- PCM telemetry systems
- Servo systems
- Function generation
- Data acquisition systems

Telecommunications applications include:
- PCM Codec telephone systems
- Intercom systems
- Military voice communication systems
- Radar systems
- Voice Encryption

Audio Applications:
- Recording
- Multiplexing of analog signals
- Voice synthesis

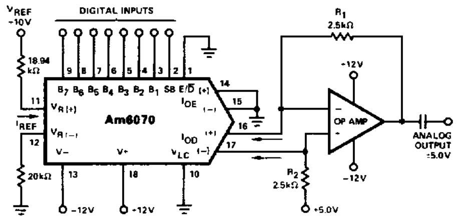
BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS



LIC-251

COMPLIANCE EXTENSION USING AC COUPLED OUTPUT



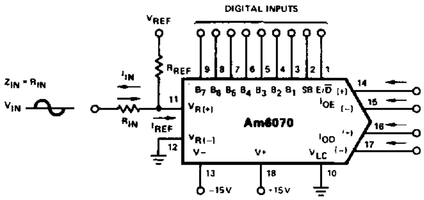
IDEAL VALUES:

$I_{REF} = 528\mu A$

$I_{FS} = 2007.75\mu A$

LIC-252

LOW INPUT IMPEDANCE CONNECTION

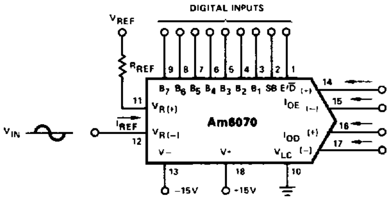


$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

LIC-253

HIGH INPUT IMPEDANCE CONNECTION

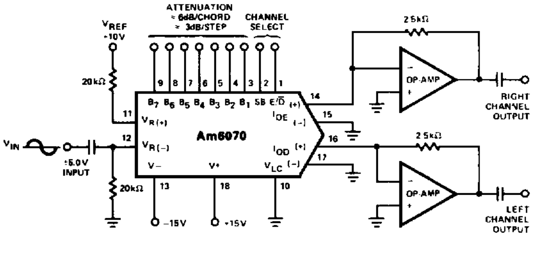


$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$

$I_{FS} \approx 4 \bullet I_{REF}$

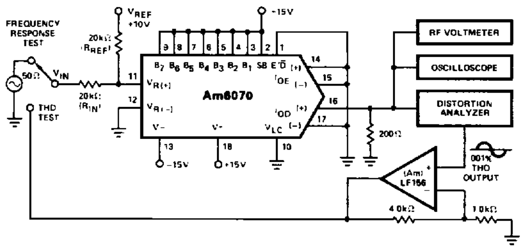
LIC-254

LOGARITHMIC DIGITAL GAIN CONTROL (Notes 4 & 5)



LIC-255

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT



LIC-256

Notes: 4. Low distortion outputs are provided over a 72dB range.
5. Up to 4 channels of output may be selected by E/D̄ and SB logic inputs.