Contents

S-29X94A Series

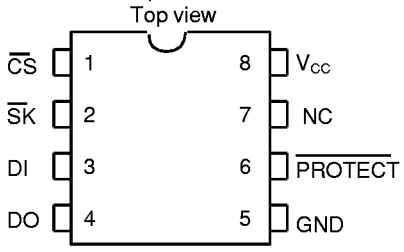
The S-29X94A Series is high speed, low power 1K/2K/4K-bit serial E²PROM with a wide operating voltage range. They are organized as 64-word × 16-bit, 128-word × 16-bit and 256-word × 16-bit, respectively. Each is capable of sequential read, where addresses are automatically incremented in 16-bit blocks.
The S-29X94A Series is capable of protecting the memory, 50% of which can be protected starting from address 00.
Interface is structured so that this IC can be directly connected to the CPU with serial ports. 8-bit instructions make it easy to prepare your own software.

■ Features

- Low power consumption
  - Standby : 1.0 μA Max. (V_{CC}=6.5 V)
  - Operating : 0.8 mA Max. (V_{CC}=5.5 V)
  - 0.4 mA Max. (V_{CC}=2.5 V)
- Wide operating voltage range
  - Write :2.5 to 6.5 V
  - Read :1.8 to 6.5 V
- Can be easily connected to the serial port
- CS Active "L"
- Endurance : 10^5 cycles/word
- Data retention : 10 years
- S-29194A : 1 Kbits
- S-29294A : 2 Kbits
- S-29394A : 4 Kbits

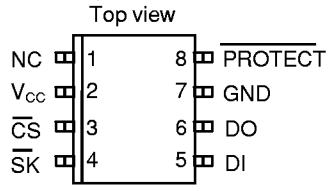
■ Pin Assignment

8-pin DIP
Top view



S-29194ADPX
S-29294ADPX
S-29394ADPX

8-pin SOP1
Top view



S-29194AFJX
S-29294AFJX
S-29394AFJX

* X differs depending on the package type :
A : A type, (blank) : B type
See ■ Dimensions.

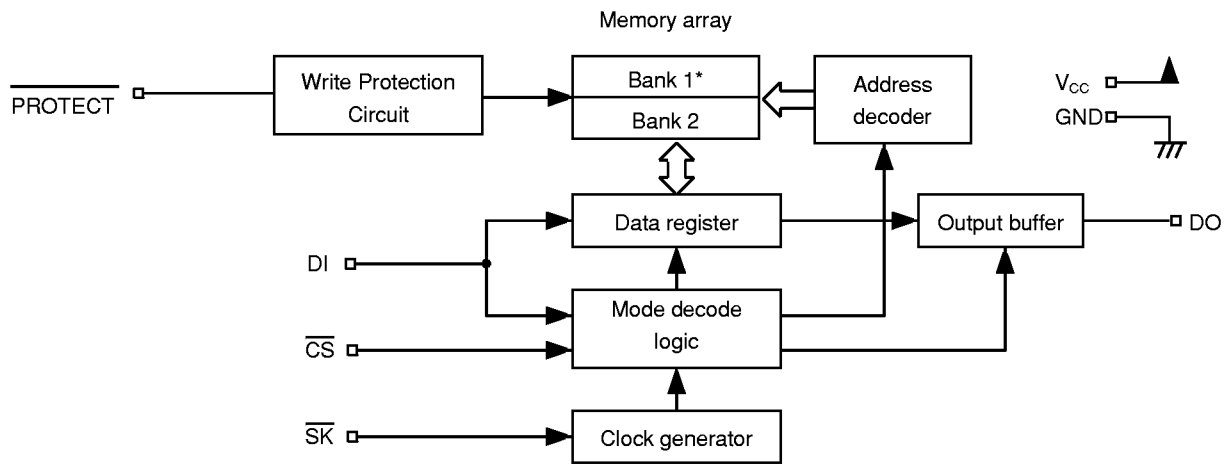
Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	DIP	SOP1	
$\overline{CS}$	1	3	Chip select input
$\overline{SK}$	2	4	Serial clock input
DI	3	5	Serial data input
DO	4	6	Serial data output
GND	5	7	Ground
$\overline{PROTECT}$	6	8	Memory Protection Control Input Connected to GND or Open : Protection Valid Connected to Vcc : Protection Invalid
NC	7	1	No Connection
V_{CC}	8	2	Power supply

■ Block Diagram



*50% of the memory can be protected starting from address 00.

Figure 2

■ Instruction Set

Table 2

Instruction	Start Bit	Ope code	Address			Data
			S-29194A	S-29294A	S-29394A	
READ (Read data)	1	1000xxx	xx A5toA0	x A6toA0	A7toA0	D_{15} to D_0 Output*
PROGRAM (Program data)	1	x100xxx	xx A5toA0	x A6toA0	A7toA0	D_{15} to D_0 Input
WRAL (Write all)	1	0001xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	D_{15} to D_0 Input
ERAL (Erase all)	1	0010xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—
PEN (Program enable)	1	0011xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—
PDS (Program disable)	1	0000xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—

x: Doesn't matter.

*: When 16-bit data of the specified address is output, the data of the next address is output.

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	- 0.3 to +7.0	V
Input voltage	V_{IN}	- 0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	- 0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	- 50 to +95	°C
Storage temperature	T_{stg}	- 65 to +150	°C

■ Recommended Operating Conditions

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation Write Enable/Disable	1.8	—	6.5	V
		Write Operation	2.5	—	6.5	V
High level input voltage	V_{IH}	V_{CC}=5.5 to 6.5 V	0.8×Vcc	—	Vcc	V
		V_{CC}=4.5 to 5.5 V	2.0	—	Vcc	V
		V_{CC}=2.7 to 4.5 V	0.8×Vcc	—	Vcc	V
		V_{CC}=1.8 to 2.7 V	0.8×Vcc	—	Vcc	V
Low level input voltage	V_{IL}	V_{CC}=5.5 to 6.5 V	0.0	—	0.2×Vcc	V
		V_{CC}=4.5 to 5.5 V	0.0	—	0.8	V
		V_{CC}=2.7 to 4.5 V	0.0	—	0.2×Vcc	V
		V_{CC}=1.8 to 2.7 V	0.0	—	0.15×Vcc	V
Operating temperature	T_{opr}		-40	—	+85	°C

■ Pin Capacitance

Table 5

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0 V	—	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT}=0 V	—	—	10	pF

■ Endurance

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^5	—	—	cycles/word

■ DC Characteristics

Table 7

Parameter	Smbl	Conditions	V_{CC}=5.5 V to 6.5 V			V_{CC}=4.5 V to 5.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO unloaded	—	—	1.0	—	—	0.8	—	—	0.6	—	—	0.4	mA
Current consumption (PROGRAM)	I_{CC2}	DO unloaded	—	—	2.5	—	—	2.0	—	—	1.5				mA

Table 8

Parameter	Smbl	Conditions	V_{CC}=4.5 V to 6.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	$\overline{CS}$=GND DO=Open Other input: Connected to V_{CC} or GND	—	—	1.0	—	—	0.6	—	—	0.4	µA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Low level output voltag	V_{OL}	I_{OL}=2.1 mA	—	—	0.45							V
		I_{OL}=100 µA	—	—	0.1	—	—	0.1	—	—	0.1	V
High level output voltag	V_{OH}	I_{OH}=-400 µA	2.4	—	—							V
		I_{OH}=-100 µA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—				V
		I_{OH}=-10 µA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—	V_{CC} -0.3	—	—	V
Write enable latch data hold voltage	V_{DH}	Only when program disable mode	1.5	—	—	1.5	—	—	1.5	—	—	V
Pull-down current	I_{PD}	$\overline{PROTECT}$ terminal = Vcc	15	—	100	3	—	50	1	—	10	µA

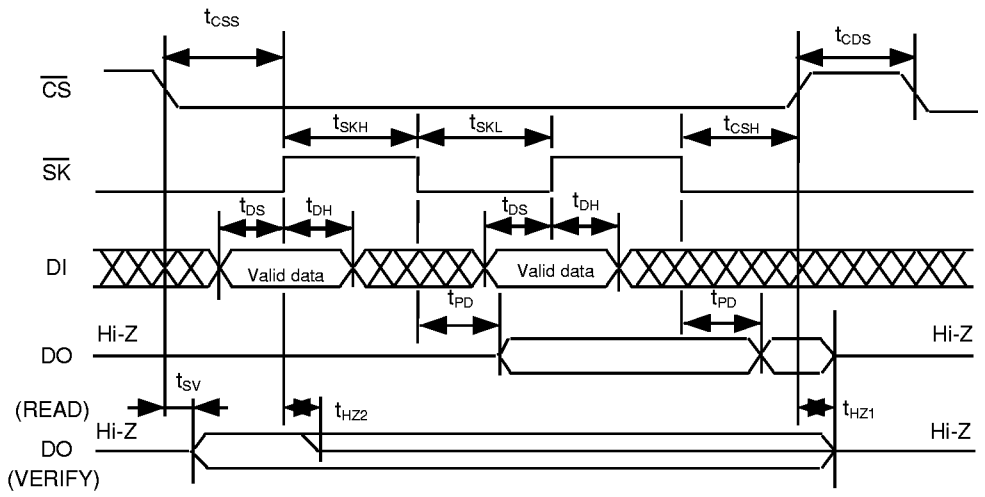
■ AC Characteristics

Table 9 Measuring conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100pF

Table 10

Parameter	Smbl	V_{CC}=4.5 to 6.5V			V_{CC}=2.5 to 4.5 V			V_{CC}=1.8 to 2.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	t_{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	µs
CS hold time	t_{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	µs
CS deselect time	t_{CDS}	0.2	—	—	0.2	—	—	0.4	—	—	µs
Data setup time	t_{DS}	0.2	—	—	0.4	—	—	0.8	—	—	µs
Data hold time	t_{DH}	0.2	—	—	0.4	—	—	0.8	—	—	µs
Output delay time	t_{PD}	—	—	0.4	—	—	1.0	—	—	2.0	µs
Clock frequency	f_{SK}	0	—	2.0	0	—	0.5	—	—	0.25	MHz
Clock pulse width	t_{SKH} t_{SKL}	0.25	—	—	1.0	—	—	2.0	—	—	µs
Output disable time	t_{HZ1} t_{HZ2}	0	—	0.15	0	—	0.5	0	—	1.0	µs
Output enable time	t_{SV}	0	—	0.15	0	—	0.5	0	—	1.0	µs
Programming time	t_{PR}	—	4.0	10.0	—	4.0	10.0				ms



Input data is retrieved on the rising edge of $\overline{SK}$.
Output data is triggered on the falling edge of $\overline{SK}$.

Figure 3 Timing Chart

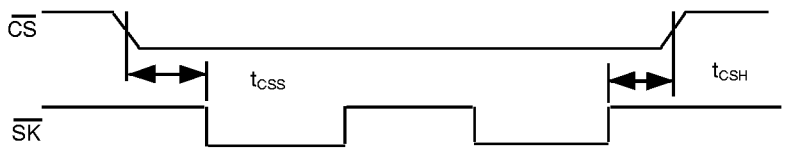


Figure 4 Timing Chart for t_{CSS} and t_{CSH} when $\overline{SK}$ is "H"

■ Operation

Instructions (in the order of start-bit, instruction, address, and data) are latched to DI in synchronization with the rising edge of $\overline{SK}$ after $\overline{CS}$ goes low. A start-bit can only be recognized when the high of DI is latched at the rising edge of $\overline{SK}$ after changing $\overline{CS}$ to low, it is impossible for it to be recognized as long as DI is low, even if there are $\overline{SK}$ pulses after $\overline{CS}$ goes low. Instruction finishes when $\overline{CS}$ goes high, where it must be high between commands during t_{CDS}.

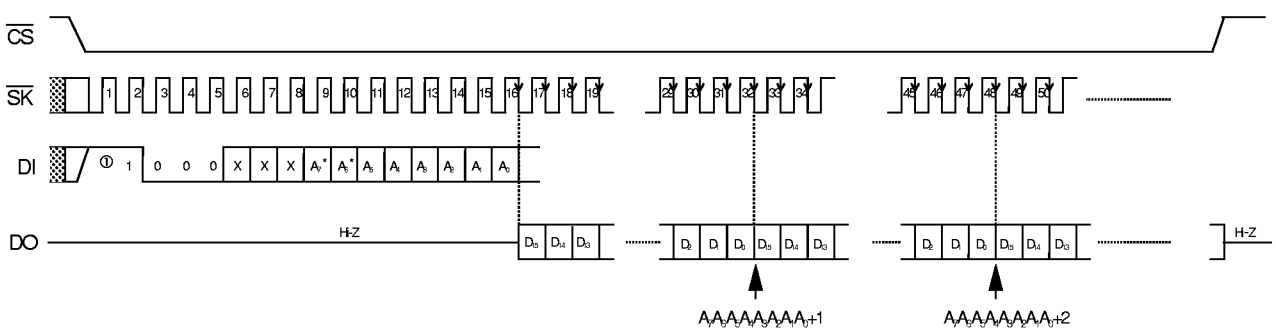
All input, including DI and $\overline{SK}$ signals, is ignored while $\overline{CS}$ is high, which is stand-by mode. The start bit + instruction, address, and data are 8-bit instructions. This makes it easy to prepare your own software using a serial interface incorporated into the CPU.

1. READ

The READ instruction reads data from a specified address. After A0 is latched at the risig edge of $\overline{SK}$, 16-bit data is continuously output in synchronization with the falling edge of $\overline{SK}$.

When all of the data (D_{15} to D_0) in the specified address has been read, data in the next address can be read with the input of another $\overline{SK}$ clock. Thus, the data over whole area of the memory can be read by continuously inputting $\overline{SK}$ clocks as long as $\overline{CS}$ is low.

The last address (An ··· A1 A0 = 1 ··· 11) rolls over to the top address (An ··· A1 A0 = 0 ··· 00).



* On the S-29194A, A_7 and A_6 are optional.
On the S-29294A, A_7 is optional.

FIgure 5 Read Timing (S-29394A)