Philips Components–Signetics

Document No.	
ECN No.	
Date of Issue	November 8, 1990
Status	Preliminary Specification
Data Communication Products	

SC26C562/SC68C562

Dual universal serial communications controller (DUSCC)

Preliminary Features and Additions between NMOS and CMOS devices.
Familiarity with the DUSCC users guide is assumed.

DESCRIPTION

The Signetics Dual Universal Serial Communications Controller (DUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The new CMOS device (SC26C562/SC68C562) will be pin hardware and software compatible with the present SCN26562 and SCN68562. All design variances in the NMOS device had been corrected. However after power up the CMOS DUSCC will be configured to operate as the NMOS DUSCC.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4.0Mbits per second are supported.

The transmitter and receiver each contain a sixteen characters FIFOs with appended transmitter command and receiver status bits. This permits reading and writing of up to sixteen characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

Two versions of the DUSCC are available. The SC26C562 is optimized to interface with processors using a synchronous bus interface, such as the 8086, 80186 and 80286. The SC68C562 is optimized to interface with processors using an asynchronous bus interface, such as the 68000 and 68010. Both versions are capable of program-polled, interrupt-driven, block-move or DMA data transfers. The contents of this manual apply to both versions of the DUSCC, unless explicitly noted otherwise.

FEATURES

General Features

- Multi-protocol operation
- Sixteen character receiver and transmitter FIFOs. Nine status bits fifoed with each byte received.
- 0 to 10Mbit/sec. data rate
- Programmable bit rate for each receiver and transmitter
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- or half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- Single- or dual-address DMA transfers
- Two multi-function programmable 16-bit counter/timers
- On-chip oscillator for crystal

Asynchronous Mode

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit up to 4.0Mbps and receive up to 2.0Mbps data rates

FEATURES (Continued)

Character-Oriented Protocols

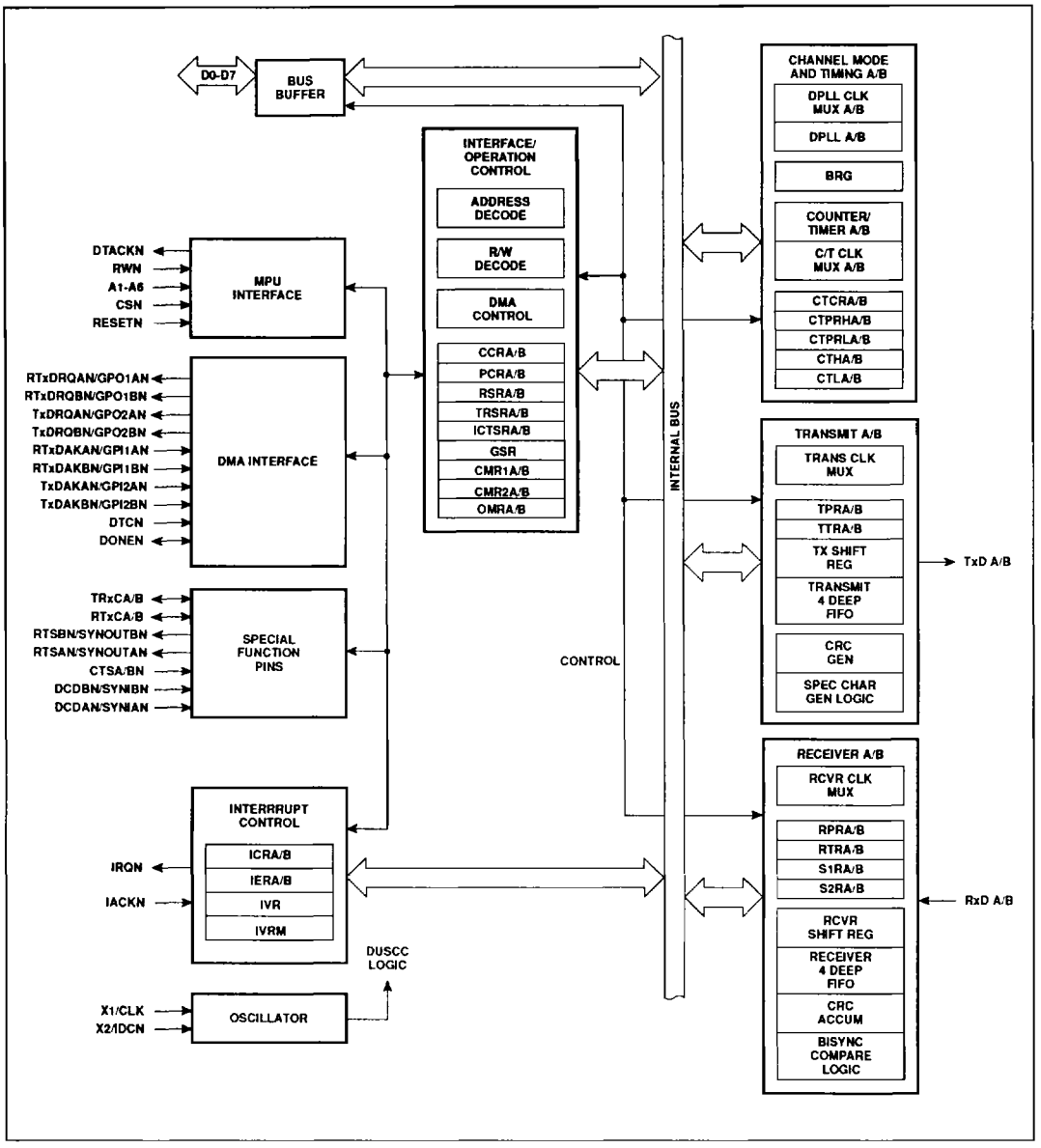
- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- SYN detection and optional stripping
- SYN or MARK linefill or underrun
- Idle in MARK or SYNs
- BISYNC submode

Bit-Oriented Protocol

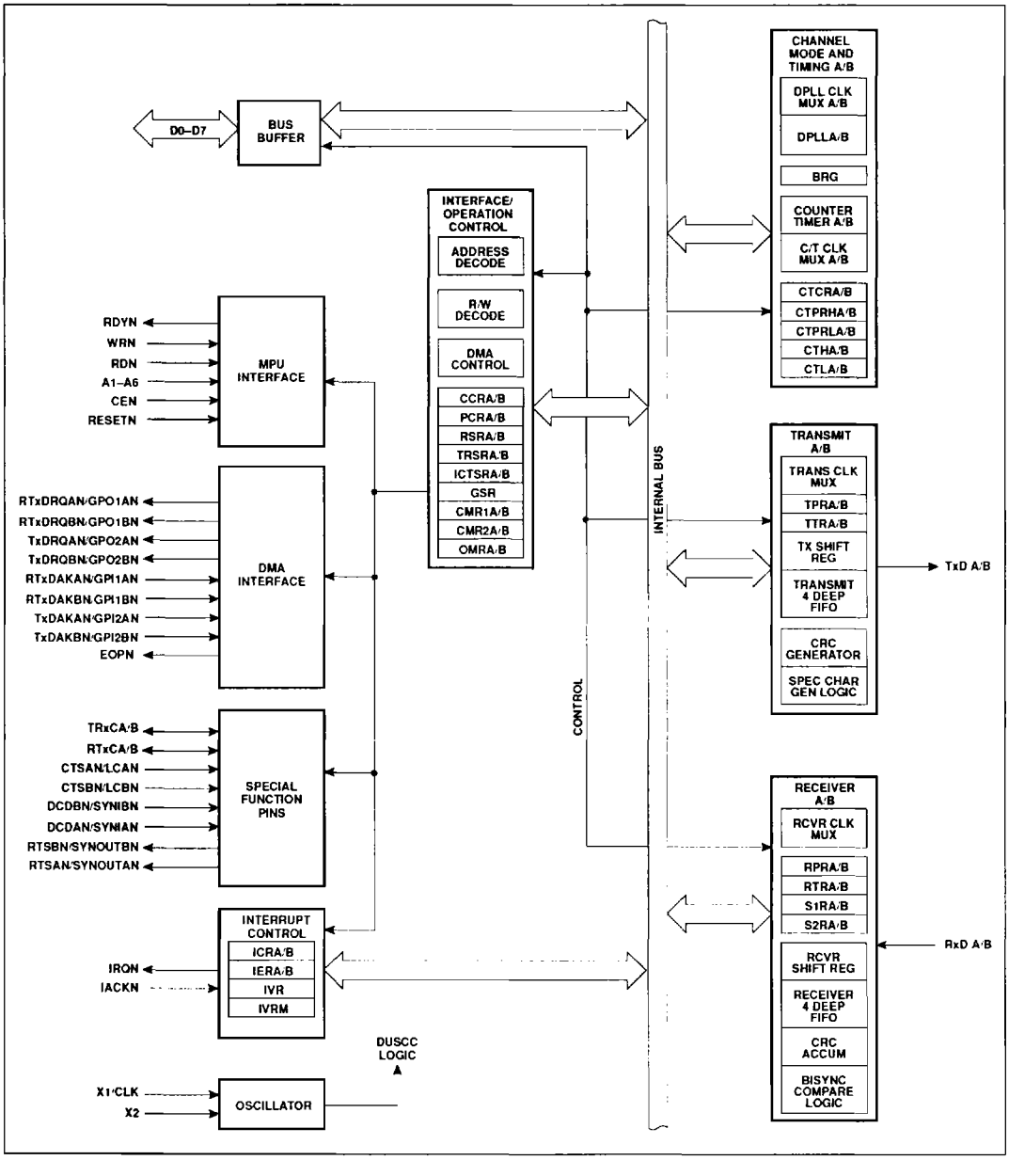
- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- ABORT, ABORT-FLAGs, or FCS-FLAGs linefill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- CRC generation and checking
- SDLC loop mode capability

Dual universal serial communications controller (DUSCC) — SC26C562/SC68C562

BLOCK DIAGRAM — SC68C562

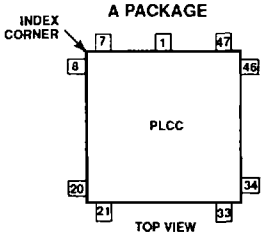


BLOCK DIAGRAM — SC26C562



Dual universal serial communications controller (DUSCC) — SC26C562/SC68C562

PIN CONFIGURATIONS — SC68C562

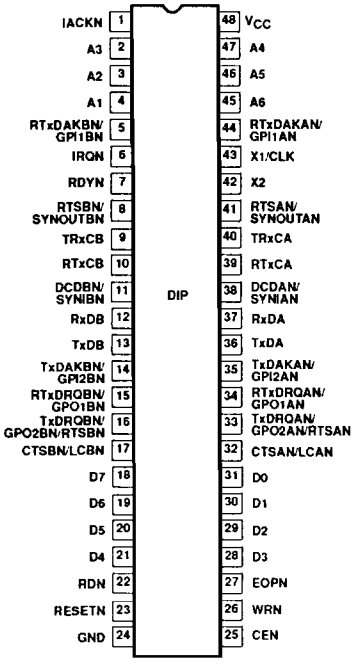


Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
6	IRQN	32	D1
7	NC	33	D0
8	RESETN	34	NC
9	RTSBN/ SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/ GPO2AN/RTSAN
11	RTxCB	37	RTxDRQAN/ GPO1AN
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
18	TxDRQBN/ GPO2BN/RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/ SYNOUTAN
20	D7	46	X2/IDCN
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/ GPI1AN
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	VDD

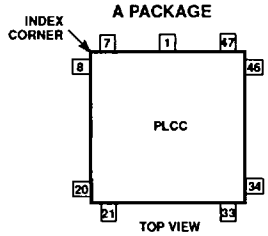
Dual universal serial communications controller (DUSCC) — SC26C562/SC68C562

PIN CONFIGURATIONS — SC26C562

N PACKAGE



A PACKAGE



PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RDYN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5	49	A6
23	D4	50	A5
24	RDN	51	A4
25	RESETN	52	VCC
26	GND		

PIN DESCRIPTION

In this document, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is Active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the Active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels; these are designated by either an underline or by A/B after the name.

MNEMONIC	APPLIES TO		TYPE	NAME AND FUNCTION
	26C562	68C562		
A1–A6	X	X	I	**Address Lines:** Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	X	X	I/O	**Bidirectional Data Bus:** Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN (CEN) is low and during interrupt acknowledge cycles and single address DMA acknowledge cycles.
R/WN		X	I	**Read/Write:** A high input indicates a read cycle and a low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN		X	I	**Chip Select:** Active-low input. When low, data transfers between the CPU and the DUSCC are enabled on D0–D7 as controlled by the R/WN and A1–A6 inputs. When CSN is high, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single address DMA transfers) and D0–D7 are placed in the 3-State condition.
DTACKN		X	O	**Data Transfer Acknowledge:** Active-low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. In a write bus cycle, input data is latched by the assertion (falling edge) of DTACKN or by the negation (rising edge) of CSN, whichever occurs first. The signal is negated when completion of the cycle is indicated by negation of CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, input data is latched by the assertion (falling edge) of DTCN or by the negation (rising edge) of the DMA acknowledge input, whichever occurs first. DTACK is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated When inactive, DTACKN requires an external pull-up resistor.
RDN	X		I	**Read Strobe:** Active-low input When active and CEN is also active, causes the content of the addressed register to be present on the data bus RDN is ignored unless CEN is active.
WRN	X		I	**Write Strobe:** Active-low input. When active and CEN is also active, the content of the data bus is loaded into the addressed register The transfer occurs on the rising edge of WRN. WRN is ignored unless CEN is active.
CEN	X		I	**Chip Enable:** Active-low input When active, data transfers between the CPU and the DUSCC are enabled on D7–D0 as controlled by RDN or WRN, and A6–A1. When CEN is high, the data lines are placed in the 3-State condition (except if IACKN is asserted or during a ddMA acknowledge cycle).
RDYN	X		O	**Ready:** Active-low, open drain Used to synchronize data transfers between the master and the DUSCC. It is valid only during read and write cycles where the DUSCC is configured in 'wait on Rx', 'wait on Tx' or 'wait on Tx or Rx' modes, otherwise it is always inactive. RDYN becomes active o n the leading edge of RDN and WRN if the requested operation cannot be performed (viz, no data in RxFIFO in the case of a read or no room in the TxFIFO in the case of a write).
IRQN	X	X	O	**Interrupt Request:** Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition The CPU can read the general status register to determine the interrupting conditon(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN		X	I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
IACKN	X		I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the DUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	X	X	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2 If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals When a crystal is used, a capacitor must be connected from this pin to ground.

PIN DESCRIPTION (Continued)

MNEMONIC	APPLIES TO		TYPE	NAME AND FUNCTION
	26C562	68C562		
X2/IDCN		X	I/O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide an interrupt daisy chain active-low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2 is not used as an interrupt daisy chain output. When a crystal is used, a capacitor must be connected from this pin to ground.
X2	X		I	**Crystal 2:** Connection for other side of crystal When a crystal is used, a capacitor must be connected from this pin to ground. If an external clock is used on X1, this pin must be grounded.
RESETN	X	X	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	X	X	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	X	X	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is in the marking condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	X	X	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	X	X	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X) or the internal system clock (X1/2)
CTSA/BN, LCA/BN	X	X	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop
DCDA/BN, SYNIA/BN	X	X	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input For the DCD function, the DUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character This mode can be used in disc or tape controller applications
RTxDRQA/BN, GPO1A/BN	X	X	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-low For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	X	X	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/BN, GPI1A/BN	X	X	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-low For half-duplex single address operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.

PIN DESCRIPTION (Continued)

MNEMONIC	APPLIES TO		TYPE	NAME AND FUNCTION
	26C562	68C562		
TxDAKA/BN, GPI2A/BN	X	X	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN		X	I	**Device Transfer Complete:** Active-low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN		X	I/O	**Done:** Active-low, open-drain. DONEN can be used and is active in both DMA and non-DMA modes. See Detailed Operation for a description of the function of this pin.
EOPN	X		I/O	**Done (EOP):** Active-low, open-drain. EOPN can be used and is active in both DMA and non-DMA modes. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA/BN	X	X	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	X	X	I	**+5V Power Input**
GND	X	X	I	**Signal and Power Ground Input**

Table 1. DUSCC Register Address Map (Present NMOS DUSCC and new CMOS DUSCC)

ADDRESS BITS[1]						ACRONYMS	REGISTER NAME	MODE	AFFECTED BY RESET
6	5	4	3	2	1				
c	0	0	0	0	0	CMR1	Channel mode register 1	R/W	Yes – 00
c	0	0	0	0	1	CMR2	Channel mode register 2	R/W	Yes – 00
c	0	0	0	1	0	S1R	SYN 1/secondary address 1 register	R/W	No
c	0	0	0	1	1	S2R	SYN 2/secondary address 2 register	R/W	No
c	0	0	1	0	0	TPR	Transmitter parameter register	R/W	Yes – 00
c	0	0	1	0	1	TTR	Transmitter timing register	R/W	No
c	0	0	1	1	0	RPR	Receiver parameter register	R/W	Yes – 00
c	0	0	1	1	1	RTR	Receiver timing register	R/W	No
c	0	1	0	0	0	CTPRH	Counter/timer preset register high	R/W	No
c	0	1	0	0	1	CTPRL	Counter/timer preset register low	R/W	No
c	0	1	0	1	0	CTCR	Counter/timer control register	R/W	Yes – 00
c	0	1	0	1	1	OMR **	Output and miscellaneous register	R/W	Yes – 00
c	0	1	1	0	0	CTH	Counter/timer high	R	No
c	0	1	1	0	1	CTL	Counter/timer low	R	No
c	0	1	1	1	0	PCR	Pin configuration register	R/W	Yes – 00
c	0	1	1	1	1	CCR **	Channel command register	R/W	No
c	1	0	0	X	X	TxFIFO	Transmitter FIFO	W	No
c	1	0	1	X	X	RxFIFO	Receiver FIFO	R	No
c	1	1	0	0	0	RSR **	Receiver status register	R/W[2]	Yes – 00
c	1	1	0	0	1	TRSR **	Transmitter and receiver status register	R/W[2]	Yes – 00
c	1	1	0	1	0	ICTSR **	Input and counter/timer status register	R/W[2]	Yes
d	1	1	0	1	1	GSR	General status register	R/W[2]	Yes – 00
c	1	1	1	0	0	IER	Interrupt enable register	R/W	Yes – 00
c	1	1	1	0	1		Not used		
0	1	1	1	1	0	IVR	Interrupt vector register – unmodified	R/W	Yes – 0F
1	1	1	1	1	0	IVRM	Interrupt vector register – modified	R	Yes – FF
0	1	1	1	1	1	ICR **	Interrupt control register	R/W	Yes – 00
1	1	1	1	1	1[3]	MRR	Master reset register	R/W	Yes[3]

NOTES:
1. c = 0 for channel A, c = 1 for channel B
   d = don't care — register may be accessed as either channel.
   x = don't care — FIFOs are addressable at any of four adjacent addresses to allow them to be addressed as byte/word/long word
2. A write to this register can perform a status resetting operation
3. SC26C562 only. See Master Reset Register section for description of operation. Not used for SC68C562.
4. n/a = Not applicable
5. ** These registers are EDGE TRIGGERED. Others are read only or level triggered. Level triggered registers should not be changed while channel is active. NOTE: ICTSR for bits 6, 5, 4 only.

REGISTERS

The addressable registers of the DUSCC are shown in Table 1. The following rules apply to all registers:

1. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle without a write being performed.
2. Unused bits of a defined register are read as zeros, unless ones have been loaded after master reset.
3. Bits that are unused in the chosen mode but are used in others are readable and writable but their contents are ignored in the chosen mode.
4. All registers are addressable as 8-bit quantities. Addresses are ordered such that certain sets of registers may also be accessed as words or long words.

The operation of the DUSCC is programmmed by writing control words into the appropriate registers Operational feedback is provided via status registers which can be read by the CPU The contents of certain control registers are initialized on RESET. Care should be exercised if the contents of a register are changed during

Dual universal serial communications controller (DUSCC) — SC26C562/SC68C562

operation, since certain changes may cause operational problems, e.g., changing the channel mode at an inappropriate time may cause the reception or transmission of an incorrect character. In general, the contents of registers which control transmitter or receiver operation, or the counter/timer, should be changed only when they are not enabled.

The DUSCC registers can be separated into five groups to describe their usage

1. Channel mode configuration and pin description registers.
2. Transmitter and receiver parameter and timing registers.
3. Counter/timer control and value registers
4. Interrupt control and status registers.
5. Command register.

CMOS DUSCC OBJECTIVE SPEC

The CMOS DUSCC is a single-chip communication device that is a fully software compatible with Signetics' DUSCC chip with 16 deep FIFO, individual interrupt enable bits. It is implemented using high speed CMOS process and faster data bus timing.

Key Features

- Fully software and hardware compatible with NMOS DUSCC
- 8 bit data bus with 160ns bus cycle
- 0 to 10Mbit per second
- Rx FIFO
  - 16 x 8 data FIFO
  - RxRDY triggered by programmable filled level of FIFO
  - Watch dog timer
  - Status bits for the filled level of Rx FIFO
  - FIFO all of the error status bits
  - Provide DMA frame status byte
- Tx FIFO
  - 16 x 8 data FIFO
  - TxRDY triggered by programmable filled level of FIFO
  - Status bits for the empty level of Tx FIFO
- Baud Rate Generator—from 50bps up to 64Kbps
- Interrupt control
  - Individual interrupt enable bits
  - Support interrupt Daisy Chain—RDYN (DTACKN) is provided
- Support X.21 pattern recognition
- Lower power consumption

CMOS DUSCC Register Address Map (New registers available by setting internal A7 bit.)

ADDRESS BITS							ACRONYM	REGISTER NAME	MODE	AFFECTED BY RESET
7	6	5	4	3	2	1				
1	c	0	0	0	1	0	IER1	Interrupt enable register 1	R/W	Yes – 00
1	c	0	0	0	1	1	IER2	Interrupt enable register 2	R/W	Yes – 00
1	c	0	0	1	0	1	IER3	Interrupt enable register 3	R/W	Yes – 00
1	c	0	0	1	1	1	RCR	Rx command register	R/W	Yes – 00
1	c	0	1	1	1	0	RFLR	RxFIFO filled level register	R	Yes – 00
1	c	1	1	1	0	0	FTLR	FIFO threshold level register	R/W	Yes – C3
1	c	1	1	1	1	0	TRMR	Tx/Rx misc register	R/W	Yes – 00
1	c	1	1	1	1	1	TFLR	TxFIFO filled level register	R	Yes – 10
x	0	1	1	1	0	1	REA	Reset internal A7 to 0	W	A7 = 0
x	1	1	1	1	0	1	SEA	Set internal A7 to 1	W	A7 = 0
x	0	1	1	1	0	1	CID	Chip identification	R	A7 = 0

Register map — The internal A7 affects the following registers and all other registers are not affected by A7.

A7 = 0	A7 = 1
S1R	IER1
S2R	IER2
TTR	IER3
RTR	RCR
PCR	RFLR
IER	FTLR
IVR/IVRM	TRMR
ICR/MRR	TELR

TTR — Transmitter Timing Register

[3210] – This field selects an output from bit rate generator to be used by the transmitter circuits. Three extra bit rate are provided if new bit rates is chosen by RCR.

[3210] – Bit Rates

0000 50/14.4K. If RCR[1] is set, TTR[3:0] = [0000] chooses 14 4Kbps. If RCR[1] is reset, then it will switch back to default value, 50bps

0001 75/56K. If RCR[1] is set, TTR[3:0] = [0001] chooses 56Kbps. If RCR[1] is reset, then it will switch back to default value, 75bps

0010 110/64K. If RCR[1] is set, TTR[3:0] = [0010] chooses 64Kbps. If RCR[1] is reset, then it will switch back to default value, 110bps.

IER1 — Interrupt Enable Register 1. This register is active only when individual interrupt enable mode is selected.

In ASYNC mode:

[7] Character Comparison

[6] RTS Negated

[5] Overrun

[4] Reserved

[3] BRK End

[2] BRK Start

[1] Frame Error

[0] Parity Error

In COP mode:

[7] EOM Detect

[6] PAD error

[5] Overrun

[4] Reserved

[3] Reserved

[2] SYN detect

[1] CRC/LRC Error

[0] Parity Error

In BOP/BOP LOOP modes:

[7] *EOM Detect*

[6] ABORT/EOP detect

[5] Overrun

[4] Short frame

[3] Idle/Turnaround Detect

[2] Flag detect

[1] CRC Error

[0] RCL not zero

IER2 — Interrupt Enable Register 2.
This register is active only when individual interrupt enable mode is selected.

In ASYNC mode:

[7] Tx path empty

[6] Reserved

[5] Tx Underrun

[4] CTS Underrun

[3] Send BRK ACK

[2] DPLL error

[1] Delta CTS detect

[0] Delta DCD detect

In COP mode:

[7] Tx path empty

[6] Tx Frame complete

[5] Tx Underrun

[4] CTS underrun

[3] Send SOM ACK

[2] DPLL error

[1] Delta CTS detect/LC detect

[0] Delta DCD detect

In BOP and BOP LOOP modes:

[7] Tx path empty

[6] Tx Frame Complete

[5] *Tx Underrun*

[4] CTS Underrun/Loop Sending

[3] Send SOM ACK

[2] DPLL error

[1] *Delta CTS/LC detect*

[0] Delta DCD detect

IER3 — Interrupt Enable Register 3.
This register is active only when individual interrupt enable mode is selected.

[7] Channel Master Interrupt Enable Bit.
This bit is used as ICR[1] or ICR[0] while A7 = 1. This bit is ignored when A7 = 0

[6] TxRDY Interrupt Enable Bit.
This bit is ignored while original IER is being used.

0 Interrupt not enabled

1 Interrupt generated if TxRDY is asserted.

[5] RxRDY Interrupt Enable Bit.
This bit is ignored while original IER is being used.

0 Interrupt not enabled

1 Interrupt generated if RxRDY is asserted.

[4] Watch Dog Timer Interrupt Enable Bit.
Interrupt generated if no data is loaded into RxFIFO within 128 consecutive bit times after command is issued.

[3] Pattern Recognition Interrupt Enable Bit.
Interrupt generated if any of the pattern recognitions is set.

[2] Reserved

[1] Reserved

[0] Reserved

TRMR — Transmitter/Receiver Misc. Register. This register provides pattern recognition status bits and Tx path empty status bit

[7:5] Reserved

[4] Tx Path Empty Status Bit.
This bit is set when the last bit of the data is being shifted out of TxD while no more character in the FIFO or in the whole transmitter data path. A '1' written to this bit can clear the status bit. This bit is also cleared if the Tx RESET or Master RESET is issued

[3] Pattern 0 Status Bit.
This bit is set when Rx receives 16 contiguous 0's after pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

[2] Pattern 1 Status Bit.
This bit is set when Rx receives 16 contiguous 1's after pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master *RESET is issued.*

[1] Pattern Alternating 01 Status Bit.
This bit is set when Rx receives 16 contiguous alternating 01 or 10 after pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

[0] WTD Status Bit.
This bit is set whenever the WTD is time out This bit is ORed together with RxRDY status bit in the GSR. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

RCR — Rx Command Register.

[7] – 0 Disable Watch Dog Timer.

1 Enable Watch Dog Timer. WTD status is set if no data is loaded into RxFIFO within 128 consecutive bit times after command is issued.

[6] – 0 Disable DMA status byte. See detail in DFSB.

1 Enable DMA status byte. The status byte for the whole frame is fifoed following last byte of frame while DMA is in progress

[5] – 0 Disable Pattern Recognition all 0's.

1 Enable Pattern Recognition all 0's. This command will have the receiver start to hunt 16 consecutive 0's

[4] – 0 Disable Pattern Recognition all 1's.

1 Enable Pattern Recognition all 1's. This command will have the receiver start to hunt 16 consecutive 1's The status bit is shown in TRMR

[3] – 0 Disable Pattern Recognition alternating 01.

1 Enable Pattern Recognition alternating 01. This command will have the receiver start to hunt 16 contiguous alternating 01 or 10 The status bit is shown in TRMR.

[2] – 0 Default mode. No individual interrupt enable mode

1 Enable individual interrupt enable mode. In this mode, IER1 and IER2 are used and original IER is ignored

[1] – 0 Default mode. No new bit rates can be selected.

1 Three additional new bit rates, 14.4k 56k, and 64k can be chosen through TTR[3:0]. See TTR[3:0] for further information

[0] Reserved

TELR — TxFIFO Empty Level Register.
This register indicates the TxFIFO empty level A read from this register can tell the current available space(s) for the TxFIFO.

[7:5] Reserved

[4:0] This field selects the available location(s) for the TxFIFO.

00000 – 0 bytes empty (implies TxFIFO full)

00001 – 1 byte empty

00010 – 2 bytes empty
00011 – 3 bytes empty
00100 – 4 bytes empty
00101 – 5 bytes empty
00110 – 6 bytes empty
00111 – 7 bytes empty
01000 – 8 bytes empty
01001 – 9 bytes empty
01010 – 10 bytes empty
01011 – 11 bytes empty
01100 – 12 bytes empty
01101 – 13 bytes empty
01110 – 14 bytes empty
01111 – 15 bytes empty
10000 – 16 bytes empty (implies TxFIFO empty)

RFLR — RxFIFO Filled Level Register.
This register indicates the RxFIFO filled level. Nine status bits are fifoed with each byte received. A read from this register can tell the current FIFO filled level.

[7:5] Reserved

[4:0] This field selects the RxFIFO filled level

00000 – 0 byte filled (implies RxFIFO empty)
00001 – 1 bytes filled
00010 – 2 bytes filled
00011 – 3 bytes filled
00100 – 4 bytes filled
00101 – 5 bytes filled
00110 – 6 bytes filled
00111 – 7 bytes filled
01000 – 8 bytes filled
01001 – 9 bytes filled
01010 – 10 bytes filled
01011 – 11 bytes filled
01100 – 12 bytes filled
01101 – 13 bytes filled
01110 – 14 bytes filled
01111 – 15 bytes filled
10000 – 16 bytes filled (implies RxFIFO full)

FTLR — FIFO Threshold Level Register.
This register indicates both TxFIFO and RxFIFO interrupt threshold level.

[7:5] This field selects the TxFIFO Threshold Level. To use threshold level to generate interrupt request, TxRDY activate bit on OMR could be set to '1' (FIFO empty). The default threshold level is 4 byte locations available TxRDY does not clear until the TxFIFO is full or transmitter is disabled.

0000 – 1 byte empty (only one space available)
0001 – 2 bytes empty
0010 – 3 bytes empty
0011 – 4 bytes empty (default mode)
0100 – 5 bytes empty
0101 – 6 bytes empty
0110 – 7 bytes empty
0111 – 8 bytes empty
1000 – 9 bytes empty
1001 – 10 bytes empty
1010 – 11 bytes empty
1011 – 12 bytes empty
1100 – 13 bytes empty
1101 – 14 bytes empty
1110 – 15 bytes empty
1111 – 16 bytes empty (TxFIFO empty)

[4:0] This field selects the RxFIFO threshold level. To generate RxRDY interrupt or DMA request, the RxFIFO filled level must be equal or greater than the threshold level.

To use the threshold level to generate interrupt request, RxRDY activate bit on OMR could be set to '1' (FIFO full). The default threshold level is 4 characters RxRDY is set when more than one byte is in the FIFO. It resets when the receiver FIFO is ready or the receiver is disabled.

0000 – 1 byte filled
0001 – 2 bytes filled
0010 – 3 bytes filled
0011 – 4 bytes filled (default mode)
0100 – 5 bytes filled
0101 – 6 bytes filled
0110 – 7 bytes filled
0111 – 8 bytes filled
1000 – 9 bytes filled
1001 – 10 bytes filled
1010 – 11 bytes filled
1011 – 12 bytes filled
1100 – 13 bytes filled
1101 – 14 bytes filled
1110 – 15 bytes filled
1111 – 16 bytes filled (Rx FIFO full)

REA — Reset Internal A7 to 0.
A write to this address set the address bit to 6 bits. This is the default mode. No new registers can be accessed Data is ignored during the write cycle.

SEA — Set Internal A7 to 1.
A write to this register automatically extend address bit to 7 bits. Therefore all the new registers can be accessed. Data is ignored during the write cycle.

CID — Chip Identification.
A read operation provides software signature which can tell the part version.

DATA OUTPUT	PART VERSION
FFH	NMOS DUSCC
EFH	CMOS DUSCC Rev. A

DFSB — DMA Frame Status Byte.
In RxDMA cycle, this status byte can be attached to the FIFO following last byte of frame (last byte means data with EOM status bit set) This byte is updated frame by frame by logical 'OR-ing' of prior status bytes with the present status byte of the frame and only used for COP or BOP/BOPL modes while DMA transfers are in progress. The DONEN (EOPN) will not be set until this byte pops to the top of the FIFO.

To enable this mode user has to send the command through CCR. (**ABORT does NOT reset DFSB but RxReset does**)

COP mode

[7] Reserved

[6] Reserved

[5] Reserved

[4] PAD ERROR

[3] DPLL error

[2] Overrun

[1] BCC ERROR

[0] Parity error

BOP/BOPL mode

[7:5] Residual character length Same as TRSR[2:0]

[4] ABORT

[3] DPLL error

[2] Overrun

[1] CRC error

[0] Short Frame

CCR — Channel Command Register.

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01xx0100 Default mode. Disable new fifoed status bits.
01xx0101 Enable new fifoed status bits In this mode all of the following status bits in RSR/TRSR reflect the status of the current character at the top of the RxFIFO.

ASYNC:	#	RSR[7]	—	Character Compare
		RSR[5]	—	Overrun
		RSR[2]	—	BRK Start
	#	RSR[1]	—	FE
	#	RSR[0]	—	PE
COP :	#	RSR[7]	—	EOM
		RSR[6]	—	Pad Error
		RSR[5]	—	Overrun
	#	RSR[1]	—	LRC/CRC error
	#	RSR[0]	—	PE
BOP/BOPL	#	RSR[7]	—	EOM
		RSR[6]	—	ABORT/EOP
		RSR[5]	—	Overrun
		RSR[4]	—	Short frame
	#	RSR[1]	—	CRC CRC error
	#	RSR[0]	—	RCL not zero

: Fifoed status bits in NMOS DUSCC.

Since abort detect and short frame may not have data byte to attach, a dummy byte is provided for status attachment. This dummy byte includes the current data in the shift register. Therefore, whenever the abort or short frame occurs, the status bit is always attached to this dummy byte.

"NOTE" In BOP/BOPL mode, TRSR[2:0] is always fifoed no matter what kind of command is issued.

GSR — General Status Register.
This register remain almost same as NMOS DUSCC's GSR except RxRDY and Rx/Tx status bits. For RxRDY status bit, it combines Rx WDT status bit with original Rx Ready together if Rx WDT is enabled. For the Tx/Rx status bit, it combines original Receiver/transmitter status bits with pattern recognition status bits and Tx path empty bit together if those functions are individually enabled.

[7] CH.B External or C/T status

[6] CH.B Rx/Tx status. This bit is set whenever one of the following status bits is set. RSR[7:0], TRSR[7:3], Tx path empty, Pattern recognitions. The Tx path empty and Pattern recognitions can affect GSR[6] only if those functions are enabled individually.

[5] CH.B TxRDY

[4] CH.B RxRDY. This bit is set either when Receiver Ready is active or when WDT status bit is set if the WDT is enabled.

[3] CH.A External or C/T status.

[2] CH.A Rx/Tx status. This bit is set whenever one of the following status bits is set. RSR[7:0], TRSR[7:3], Tx path empty, Pattern recognitions. The Tx path empty and Pattern recognitions can affect GSR[6] only if those functions are enabled individually.

[1] CH. A TxRDY.

[0] CH.A RxRDY. This bit is set either when Receiver Ready is active or when WDT status bit is set if the WDT is enabled.

BISYNC control:

CMR1 [5]	CMR [4:3]	
0	00	EBCDIC, NO parity, 8 bit data, 8 bit CTRL character.
1	00	ASCII, NO parity, 8 bit data, 8 bit CTRL character. Odd parity bit is generated by users. It's same as NMOS DUSCC. Receiver check the parity bit by loop-up table. If an LRC BCC is selected in CMR[2:0] then LRC-8 is used (the MSB of the LRC is the logical XOR of all MSBs in the frame.)
1	01	ASCII, No parity, 8 bit data, 8 bit CTRL character. The receiver only check 7 bits for the CTRL character and ignore the MSB of each character. If an LRC BCC is selected in CMR[2:0] then LRC-7 is used (the MSB of the LRC is 0).
1	10	ASCII, ODD parity, 7 bit data + 1 odd parity bit, 7 bit CTRL char + 1 odd parity bit. Parity bit is generated/checked by DUSCC. Any CTRL character as parity error will not be treated as a CTRL character. If an LRC BCC is selected in CMR[2:0] then LRC-7 is used. The MSB of the LRC will be the ODD PARITY value computed from the 7 other bits that comprise the LRC.
1	11	ASCII, EVEN parity. Similar to CMR[4.3] = 10 except parity bit is even