



ISD33120/150/180/240 Products

Single-Chip Voice Record/Playback Devices

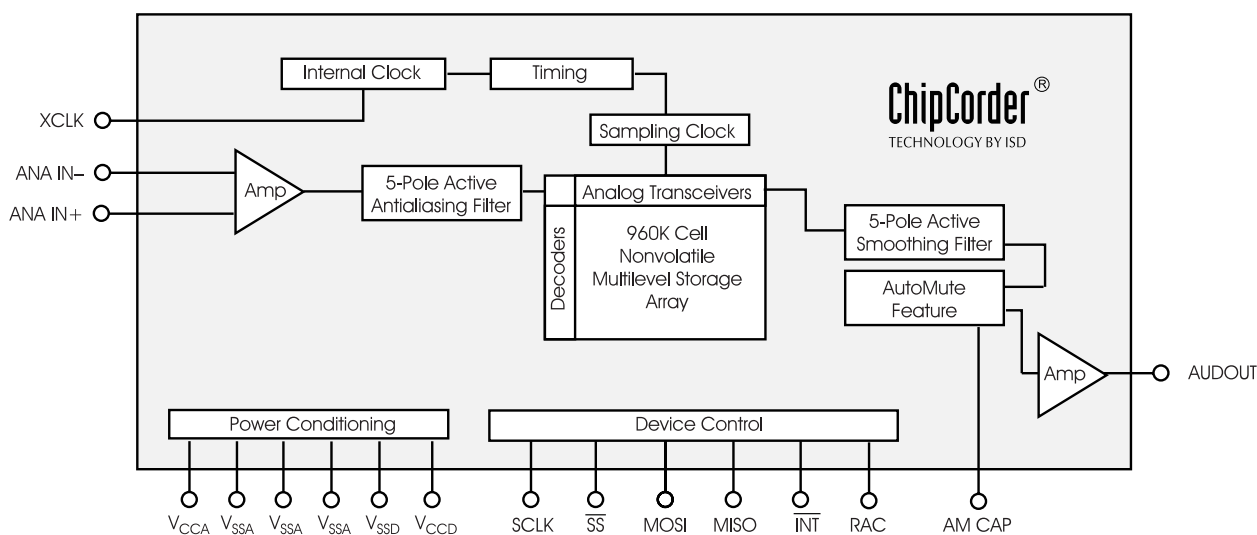
2-, 2.5-, 3-, and 4-Minute Durations

GENERAL DESCRIPTION

The ISD33120/150/180/240 ChipCorder® Products provide high-quality, 3-volt, single-chip record/playback solutions for 2- to 4-minute messaging applications which are ideal for cellular phones and other portable products. The CMOS devices include an on-chip oscillator, antialiasing filter, smoothing filter, AutoMute™ feature, audio amplifier, and high density, multilevel storage array. The ISD33000 series is designed to be used in a microprocessor- or microcontroller-based system. Address and control are accomplished through a Serial Peripheral Interface (SPI) or Microwire Serial Interface to minimize pin count.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure: ISD33000 Series Block Diagram



FEATURES

- Single-chip voice record/playback solution
 - Single +3 volt supply
 - Low-power consumption
 - Operating current:
 I_{CC} Play = 25 mA (typical)
 I_{CC} Rec = 30 mA (typical)
 - Standby current: 1 μ A (typical)
 - Single-chip durations of 2 to 4 minutes
 - High-quality, natural voice/audio reproduction
 - AutoMute™ feature provides background noise attenuation during periods of silence
 - No algorithm development required
 - Microcontroller SPI or Microwire™ Serial Interface
 - Fully addressable to handle multiple messages
 - Nonvolatile message storage
 - Power consumption controlled by SPI or microwire control register
 - 100-year message retention (typical)
 - 100,000 record cycles (typical)
 - On-chip clock source
 - Available in die form, PDIP, SOIC, and TSOP packaging
 - Extended temperature (–20°C to +70°C) and industrial temperature (–40°C to +85°C) versions available
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Table: ISD33120/150/180/240 Product Summary

Part Number	Duration	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD33120	2.0 Min.	8.0	3.4
ISD33150	2.5 Min.	6.4	2.7
ISD33180	3.0 Min.	5.3	2.3
ISD33240	4.0 Min.	4.0	1.7

Table of Contents

ISD33120/150/180/240 Products

Single-Chip Voice Record/Playback Devices
2-, 2.5-, 3-, and 4-Minute Durations

DETAILED DESCRIPTION	1
Speech/Sound Quality	1
Duration	1
EEPROM Storage	1
Microcontroller Interface	1
Programming	1
PIN DESCRIPTIONS	2
Voltage Inputs (V_{CCA} , V_{CCD})	2
Ground Inputs (V_{SSA} , V_{SSD})	2
Non-Inverting Analog Input (ANA IN+)	3
Inverting Analog Input (ANA IN-)	3
Audio Output (AUD OUT)	3
Slave Select ($\overline{SS}$)	4
Master Out Slave In (MOSI)	4
Master In Slave Out (MISO)	4
Serial Clock (SCLK)	4
Interrupt ($\overline{INT}$)	4
Row Address Clock (RAC)	4
External Clock Input (XCLK)	5
AutoMute™ Feature (AM CAP)	5
SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION	5
Message Cueing	6
Power-Up Sequence	7
SPI Port	8
SPI Control Register	8
TIMING DIAGRAMS	17
DEVICE PHYSICAL DIMENSIONS	21
ORDERING INFORMATION	26

FIGURES, CHARTS, AND TABLES IN THE ISD33120/150/180/240 PRODUCTS DATASHEET

Figure 1:	ISD33000 TSOP and DIP/SOIC Pinouts	2
Figure 2:	ISD33000 Series ANA IN Modes	3
Figure 3:	SPI Port	7
Figure 4:	SPI Interface Simplified Block Diagram	8
Figure 5:	Timing Diagram	17
Figure 6:	8-Bit Command Format	17
Figure 7:	16-Bit Command Format	18
Figure 8:	Playback/Record and Stop Cycle	18
Figure 9:	Application Example Using SPI	19
Figure 10:	Application Example Using Microwire	20
Figure 11:	Application Example Using SPI Port on Microcontroller	20
Figure 12:	28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type I (E)	21
Figure 13:	28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)	22
Figure 14:	28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)	23
Figure 15:	ISD33120/150/180/240 Products Bonding Physical Layout (Unpackaged Die)	24
Table 1:	External Clock Input Precision Power Regulation	5
Table 2:	Opcode Summary	6
Table 3:	SPI Control Register	8
Table 4:	Absolute Maximum Ratings (Packaged Parts)	9
Table 5:	Operating Conditions (Packaged Parts)	9
Table 6:	DC Parameters (Packaged Parts)	9
Table 7:	AC Parameters (Packaged Parts)	10
Table 8:	Absolute Maximum Ratings (Die)	13
Table 9:	Operating Conditions (Die)	13
Table 10:	DC Parameters (Die)	13
Table 11:	AC Parameters (Die)	14
Table 12:	SPI AC Parameters	16
Table 13:	Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions	21
Table 14:	Plastic Dual Inline Package (PDIP) (P) Dimensions	22
Table 15:	Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions	23
Table 16:	ISD33120/150/180/240 Devices PIN/PAD Designations,	25

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD33000 ChipCorder series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD33120/150/180/240 Product Summary table on page ii to compare filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state solutions.

DURATION

To meet end system requirements, the ISD33120/150/180/240 Products are single-chip solutions at 2, 2.5, 3, and 4 minutes. One- to two-minute durations are addressed in the ISD33060/075/090/120-4 Products datasheet. More than one device can be controlled by one microcontroller for longer durations.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

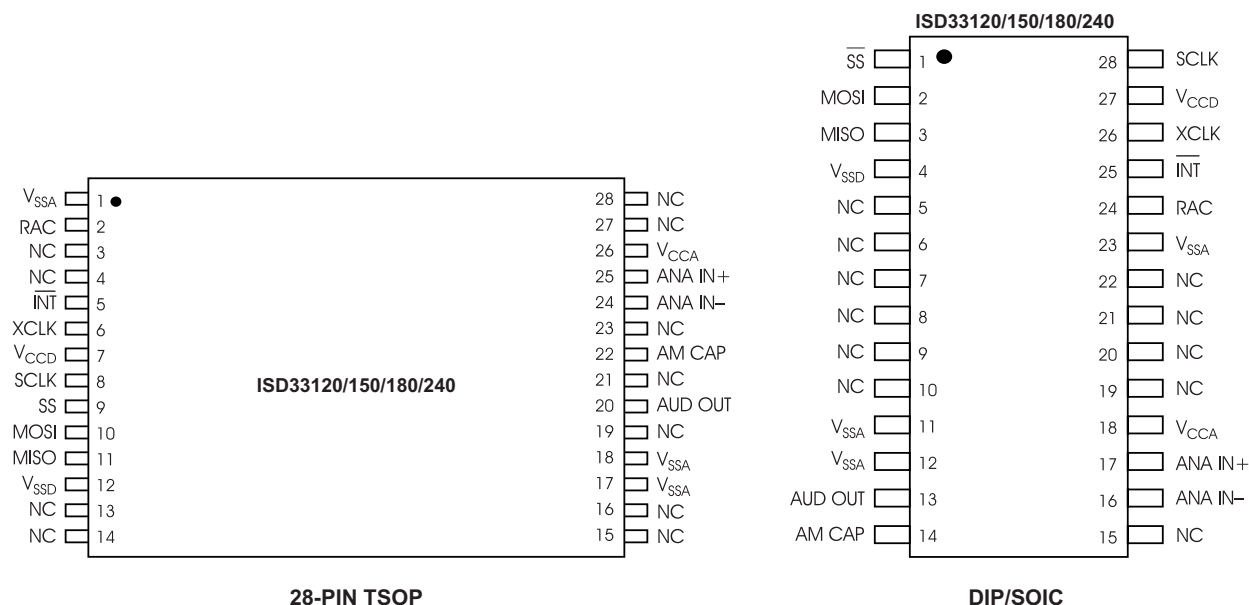
MICROCONTROLLER INTERFACE

A four-wire (SCLK, MOSI, MISO, $\overline{SS}$) SPI interface is provided for ISD33000 control and addressing functions. The ISD33000 is configured to operate as a peripheral slave device, with a microcontroller-based SPI bus interface. Read/Write access to all the internal registers is provided through this SPI interface. An interrupt signal ($\overline{INT}$) and internal read-only Status Register are provided for handshake purposes.

PROGRAMMING

The ISD33000 series is also ideal for playback-only applications, where single or multiple message playback is controlled through the SPI port. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

Figure 1: ISD33000 TSOP and DIP/SOIC Pinouts



PIN DESCRIPTIONS

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD33000 devices use separate power busses. These +3 V busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

GROUND INPUTS (V_{SSA}, V_{SSD})

The ISD33000 series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low-impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3 ohms. The backside of the die is connected to V_{SS} through the substrate resistance. In a chip-on-board design the die attach area must be connected to V_{SS} or left floating.

NON-INVERTING ANALOG INPUT (ANA IN+)

This pin is the non-inverting analog input that transfers the signal to the device for recording. The analog input amplifier can be driven single ended or differentially. In the single-ended input mode, a 32 mVp-p for optional sound quality (peak-to-peak) maximum signal should be capacitively connected to this pin for optimal signal quality. This capacitor value, together with the 3 K Ω input impedance of ANA IN+, is selected to give cutoff at the low frequency end of the voice passband. In the differential-input mode, the maximum input signal at ANA IN+ should be 16 mVp-p for optional sound quality. The circuit connections for the two modes are shown in the ISD33000 series ANA IN Modes figures below.

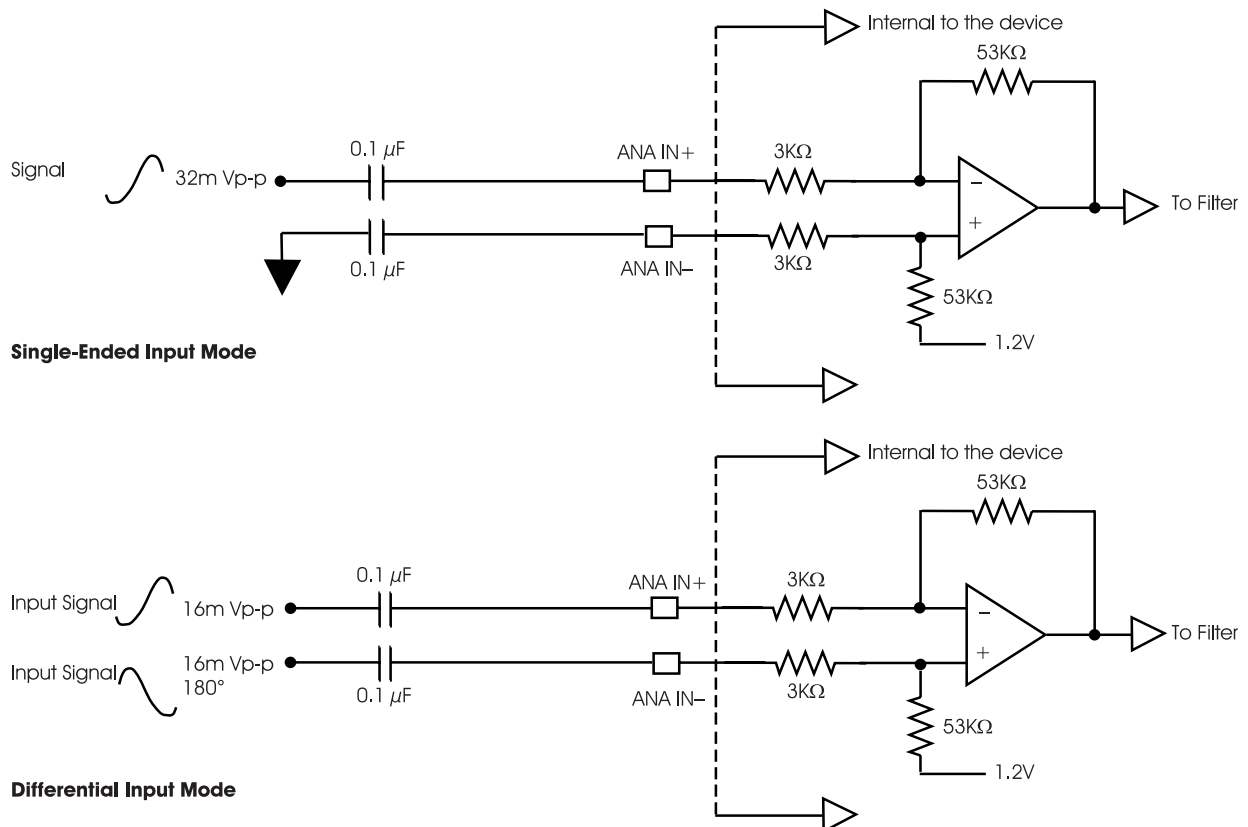
INVERTING ANALOG INPUT (ANA IN-)

This pin is the inverting analog input that transfers the signal to the device for recording in the differential-input mode. In this differential-input mode, a 16 mVp-p maximum input signal at ANA IN- should be capacitively coupled to this pin for optimal sound quality (as shown in the ISD33000 series ANA IN Modes figure). This capacitor value should be equal to the coupling capacitor used on the ANA IN+ pin. The input impedance at ANA IN- is nominally 56 K Ω . In the single-ended mode, ANA IN- should be capacitively coupled to V_{SSA} through a capacitor equal to that used on the ANA IN+ input.

AUDIO OUTPUT (AUD OUT)

This pin provides the audio output to the user. It is capable of driving a 5 K Ω impedance.

Figure 2: ISD33000 Series ANA IN Modes



NOTE The AUD OUT pin is biased up to approximately 1.2 volts unless the ISD33000 is actively recording or the device is in the power-down state. When the device is actively recording or powered down, the pin is in a high-impedance state. This means that there is a transition from high-impedance to 1.2 volts under the following conditions:

- When a SPI cycle is executed to initially set the PU bit and thus power-up the device.
- When a SPI cycle is executed to clear the RUN bit during a RECORD operation, and thus stop recording.
- When the device goes into OVERFLOW during a RECORD operation both ending the recording and setting the OVF interrupt.

There is a transition from 1.2 volts to high-impedance under the following condition:

- When a SPI cycle is executed to begin a RECORD operation and in power-down mode.

SLAVE SELECT ($\overline{SS}$)

This input, when LOW, will select the ISD33000 device.

MASTER OUT SLAVE IN (MOSI)

This is the serial input to the ISD33000 device. The master microcontroller places data on the MOSI line one half-cycle before the rising clock edge to be clocked in by the ISD33000 device.

MASTER IN SLAVE OUT (MISO)

This is the serial output of the ISD33000 device. This output goes into a high-impedance state if the device is not selected.

SERIAL CLOCK (SCLK)

This is the clock input to the ISD33000. It is generated by the master device (microcontroller) and is used to synchronize data transfers in and out of the device through the MISO and MOSI lines. Data is latched into the ISD33000 on the rising edge of SCLK and shifted out of the device on the falling edge of SCLK.

INTERRUPT ($\overline{INT}$)

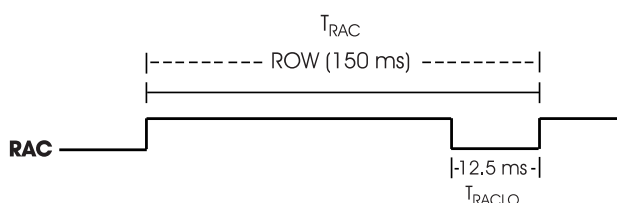
The ISD33000 interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. This is an open drain output pin. Each operation that ends in an EOM or Overflow will generate an interrupt including the message cueing cycles. The interrupt will be cleared the next time an SPI cycle is initiated. The interrupt status can be read by an RINT instruction.

Overflow Flag (OVF)—The Overflow flag indicates that the end of the ISD33000's analog memory has been reached during a record or playback operation.

End of Message (EOM)—The End-of-Message flag is set only during playback operation when an EOM is found. There are six EOM flag position options per row.

ROW ADDRESS CLOCK (RAC)

This is an open drain output pin that provides a signal with a 150 ms period at the 8 KHz sampling frequency. (This represents a single row of memory and there are 800 rows of memory in the ISD33120/150/180/240 devices. This signal stays HIGH for 137.5 ms and stays LOW for 12.5 ms when it reaches the end of a row. When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACLO} period. This is due to the need to load the sample and hold circuits internal to the device.



The RAC pin stays HIGH for 172 μ sec and stays LOW for 15.62 μ sec in Message Cueing mode (see "Message Cueing" on page 6). Refer to the AC Parameters table for RAC timing information on other sample rate products. The RAC pin can be used for message management techniques.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD33000 products has an internal pull-down device. These products are configured at the factory with an internal sampling clock frequency centered to ± 1 percent of specification. The frequency is then maintained to a variation over the entire commercial temperature and operating voltage ranges as defined by the minimum/maximum limits in the AC Parameters tables. The internal clock has a wider tolerance over the extended temperature, industrial temperature, and voltage ranges as defined by the minimum/maximum limits in the applicable AC Parameters tables. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 1: External Clock Input Precision Power Regulation

Part Number	Sample Rate	Required Clock
ISD33120	8.0 KHz	1024 KHz
ISD33150	6.4 KHz	819.2 KHz
ISD33180	5.3 KHz	682.7 KHz
ISD33240	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed. Thus, aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. ***If the XCLK is not used, this input should be connected to ground.***

AUTOMUTE™ FEATURE (AM CAP)

This pin is used in controlling the AutoMute feature. The AutoMute feature attenuates the signal when it drops below an internally set threshold. This helps to eliminate noise (with 6 dB of attenuation) when there is no signal (i.e., during periods of silence). A 1 μ F capacitor to ground should be connected to the AMCAP pin. This capacitor becomes a part of an internal peak detect circuit which senses the signal level. This peak level is compared to an internally set threshold to determine the AutoMute trip point. For large signals the AutoMute attenuation is set to 0 dB while 6 dB of attenuation occurs for silence. The 1 μ F capacitor also affects the rate at which the AutoMute feature changes with the signal amplitude. The AutoMute feature can be disabled by connecting the AMCAP pin to V_{CCA} .

SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION

The ISD33000 series operates from an SPI serial interface. The SPI interface operates with the following protocol.

The data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on the falling edge of the SCLK. With the ISD33000, data is clocked in on the MOSI pin on the rising clock edge. Data is clocked out on the MISO pin on the falling clock edge.

1. All serial data transfers begin with the falling edge of $\overline{SS}$ pin.
2. $\overline{SS}$ is held LOW during all serial communications and held HIGH between instructions.
3. Data is clocked in on the rising clock edge and data is clocked out on the falling clock edge.
4. Play and record operations are initiated by enabling the device by asserting the $\overline{SS}$ pin LOW, shifting in an opcode and an address field to the ISD33000 device (refer to the Opcode Summary table on the next page).

5. The opcodes and address fields are as follows: <5 control bits> and <11 address bits>. It should be noted that the ISD33120/150/180/240 devices only need 10 bits of address but the 11th bit is reserved for longer duration products. For clarity, the control bits and the address bits will be displayed in binary and "X" means Don't Care.
6. Each operation that ends in an EOM or Overflow will generate an interrupt, including the Message Cueing cycles. The Interrupt will be cleared the next time an SPI cycle is initiated.
7. As Interrupt data is shifted out of the ISD33000 MISO pin, control and address data is simultaneously being shifted into the MOSI pin. Care should be taken such that the data shifted in is compatible with

current system operation. It is possible to read interrupt data and start a new operation within the same SPI cycle.

8. An operation begins with the RUN bit set and ends with the RUN bit reset.
9. All operations begin with the rising edge of $\overline{SS}$.

MESSAGE CUEING

Message cueing allows the user to skip through messages, without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 800 times faster than in normal playback mode. It will stop when an EOM (end of message) marker is reached. Then, the internal address counter will point to the next message.

Table 2: Opcode Summary

Instruction	Opcode <5 bits> Address <10 bits>	Operational Summary
POWERUP	00100 <XXXXXXXXXX>	Power-Up: Device will be ready for an operation after T_{PUD} .
SETPLAY	11100 <X A9-A0>	Initiates playback from address <A9-A0>. Must be followed by a PLAY command to continue playback.
PLAY	11110 <XXXXXXXXXX>	Play back from the current address (until EOM or OVF).
SETREC	10100 <X A9-A0>	Initiates a record operation from address <A9-A0>. Must be followed by a REC command to continue recording.
REC	10110 <XXXXXXXXXX>	Records from current address until recording is stopped or OVF is reached.
SETMC	11101 <X A9-A0>	Initiates Message Cueing (MC) from address <A9-A0>. Must be followed by a MC command to continue Message Cueing.
MC ⁽¹⁾	11111 <XXXXXXXXXX>	Performs a Message Cue. Proceeds to the end of the current message (EOM) or enters OVF condition if no more messages are present.
STOP	0X110 <XXXXXXXXXX>	Stops current operation.
STOPPWRDN	0X01X <XXXXXXXXXX>	Stops current Operation and enters stand-by (power-down) mode.
RINT ⁽²⁾	0X110 <XXXXXXXXXX>	Read Interrupt status bits: Overflow and EOM.

1. Message Cueing can be selected only at the beginning of a play operation.
2. As the Interrupt data is shifted out of the ISD33000, control and address data is being shifted in. Care should be taken such that the data shifted in is compatible with current system

operation. It is possible to read interrupt data and start a new operation at the same time. See "Timing Diagrams" on page 17 for Opcode format.

POWER-UP SEQUENCE

The ISD33000 will be ready for an operation after T_{PUD} (25 ms approx. for 8 KHz sample rate). The user needs to wait T_{PUD} before issuing an operational command. For example, to play from address 00 the following programming cycle should be used.

Playback Mode

1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Send SETPLAY command with address 00.
4. Send PLAY command.

The device will start playback at address 00 and it will generate an interrupt when an EOM is reached. It will then stop playback.

Record Mode

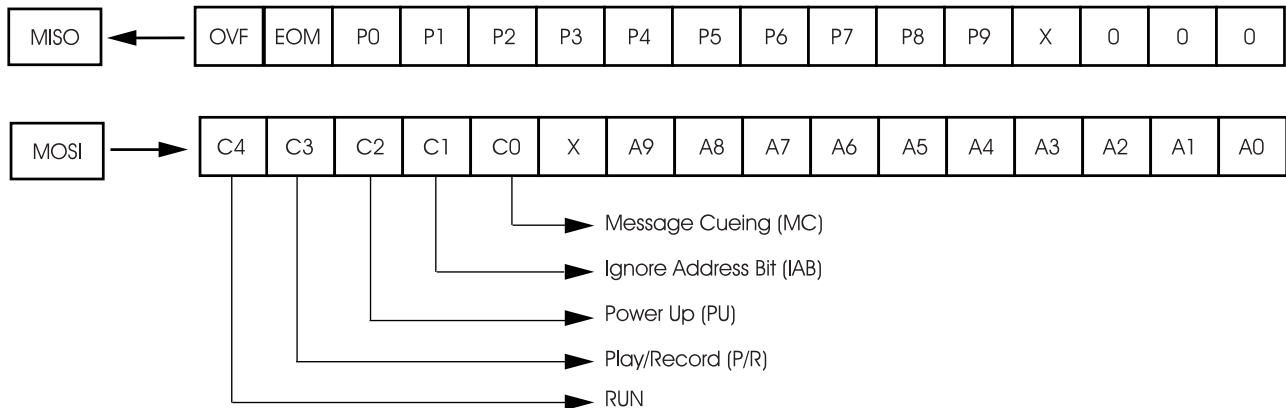
1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Send POWERUP command.
4. Wait $2 \times T_{PUD}$ (power-up delay).
5. Send SETREC command with address 00.
6. Send REC command.

The device will start recording at address 00 and it will generate an interrupt when an overflow is reached (end of memory array). It will then stop recording.

SPI PORT

The following diagram describes the SPI port and the control bits associated with it.

Figure 3: SPI Port



SPI CONTROL REGISTER

the spi control register provides control of individual device functions such as play, record, message cueing, power-up and power-down, start and stop operations, and Ignore Address pointers.

Table 3: SPI Control Register

Control Register	Bit	Device Function	Control Register	Bit	Device Function
RUN		Enable or Disable an operation	PU		Master power control
=	1	Start	=	1	Power-Up
=	0	Stop	=	0	Power-Down
P/ $\bar{R}$		Selects Play or Record operation	IAB ⁽¹⁾		Ignore address control bit
=	1	Play	=	1	Ignore input address register (A9–A0)
=	0	Record	=	0	Use the input address register contents for an operation (A9–A0)
MC		Enable or Disable Message Cueing	P9–P0		Output of the row pointer register
=	1	Enable Message Cueing	A9–A0		Input address register
=	0	Disable Message Cueing			

1. When IAB (Ignore Address Bit) is set to 0, a playback or record operation starts from address (A9–A0). For consecutive playback or record, IAB should be changed to a 1 before the end of that row (see RAC timing). Otherwise the ISD33000 will repeat the operation from the same row address. For memory management, the Row Address Clock (RAC) pin and IAB can be used to move around the memory segments.

Figure 4: SPI Interface Simplified Block Diagram

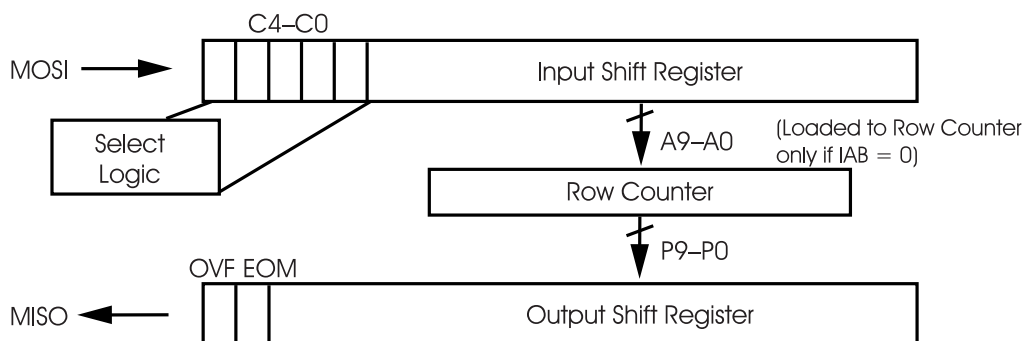


Table 4: Absolute Maximum Ratings
(Packaged Parts)⁽¹⁾

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V _{SS} – 0.3 V) to (V _{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V _{SS} – 1.0 V) to (V _{CC} + 1.0 V)
Voltage applied to MOSI, SLK, INT, RAC and SS pins (Input current limited to ±20 mA)	(V _{SS} – 1.0 V) to 5.5 V
Lead temperature (soldering – 10 seconds)	300°C
V _{CC} – V _{SS}	–0.3 V to +7.0 V

1. Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

Table 5: Operating Conditions
(Packaged Parts)

Condition	Value
Commercial operating temperature range ⁽¹⁾	0°C to +70°C
Extended operating temperature ⁽¹⁾	–20°C to +70°C
Industrial operating temperature ⁽¹⁾	–40°C to +85°C
Supply voltage (V _{CC}) ⁽²⁾	+2.7 V to +3.3 V
Ground voltage (V _{SS}) ⁽³⁾	0 V

1. Case temperature.

2. V_{CC} = V_{CCA} = V_{CCD}.

3. V_{SS} = V_{SSA} = V_{SSD}.

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
V _{IL}	Input Low Voltage			V _{CC} × 0.2	V	
V _{IH}	Input High Voltage	V _{CC} × 0.8		3.3 ⁽³⁾	V	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 10 μA
V _{OL1}	RAC, INT Output Low Voltage			0.4	V	I _{OL} = 1 mA
V _{OH}	Output High Voltage	V _{CC} – 0.4			V	I _{OH} = –10 μA
I _{CC}	V _{CC} Current (Operating) Playback Record		25 30	30 40	mA mA	R _{EXT} = ∞ ⁽⁴⁾ R _{EXT} = ∞ ⁽⁴⁾
I _{SB}	V _{CC} Current (Standby)		1	10	μA	(4) (5)
I _{IL}	Input Leakage Current			±1	μA	
I _{HZ}	MISO Tristate Current		1	10	μA	
R _{EXT}	Output Load Impedance	5			KΩ	
R _{ANA IN+}	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
R _{ANA IN-}	ANA IN- Input Resistance	40	55.8	71	K Ω	
A _{ARP}	ANA IN+ or ANA IN- to AUD OUT Gain		25		dB	⁽⁶⁾

1. Typical values @ $T_A = 25^\circ\text{C}$ and 3.0 V.
2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. When driven by a 5-volt microcontroller, the maximum V_{IH} for the MOSI, SCLK, and $\overline{SS}$ pins is 5.5 volts.
4. V_{CCA} and V_{CCD} connected together.
5. $\overline{SS} = V_{CCA} = V_{CCD}$, XCLK = MOSI = $V_{SSA} = V_{SSD}$ and all other pins floating.
6. Measured with AutoMute feature disabled.

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
F _S	Sampling Frequency	ISD33120		8.0		KHz	⁽⁵⁾
		ISD33120D		8.0		KHz	⁽⁵⁾
		ISD33120I		8.0		KHz	⁽⁵⁾
		ISD33150		6.4		KHz	⁽⁵⁾
		ISD33150D		6.4		KHz	⁽⁵⁾
		ISD33150I		6.4		KHz	⁽⁵⁾
		ISD33180		5.3		KHz	⁽⁵⁾
		ISD33180D		5.3		KHz	⁽⁵⁾
		ISD33180I		5.3		KHz	⁽⁵⁾
		ISD33240		4.0		KHz	⁽⁵⁾
		ISD33240D		4.0		KHz	⁽⁵⁾
		ISD33240I		4.0		KHz	⁽⁵⁾
F _{CF}	Filter Pass Band	ISD33120		3.4		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33120D		3.4		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33120I		3.4		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33150		2.7		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33150D		2.7		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33150I		2.7		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33180		2.3		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33180D		2.3		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33180I		2.3		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33240		1.7		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33240D		1.7		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾
		ISD33240I		1.7		KHz	3-dB Roll-Off Point ⁽³⁾⁽⁷⁾

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
T _{REC}	Record Duration	ISD33120	114.9	124.5	sec	Commercial ⁽⁶⁾
		ISD33120D	114.9	125.7	sec	Extended ⁽⁶⁾
		ISD33120I	111.8	129.6	sec	Industrial ⁽⁶⁾
		ISD33150	143.7	155.6	sec	Commercial ⁽⁶⁾
		ISD33150D	143.7	157.1	sec	Extended ⁽⁶⁾
		ISD33150I	139.8	162.0	sec	Industrial ⁽⁶⁾
		ISD33180	172.4	186.7	sec	Commercial ⁽⁶⁾
		ISD33180D	172.4	188.5	sec	Extended ⁽⁶⁾
		ISD33180I	167.8	194.5	sec	Industrial ⁽⁶⁾
		ISD33240	229.9	248.9	sec	Commercial ⁽⁶⁾
		ISD33240D	229.9	251.3	sec	Extended ⁽⁶⁾
		ISD33240I	223.7	259.3	sec	Industrial ⁽⁶⁾
T _{PLAY}	Playback Duration	ISD33120	114.9	124.5	sec	Commercial ⁽⁶⁾
		ISD33120D	114.9	125.7	sec	Extended ⁽⁶⁾
		ISD33120I	111.8	129.6	sec	Industrial ⁽⁶⁾
		ISD33150	143.7	155.6	sec	Commercial ⁽⁶⁾
		ISD33150D	143.7	157.1	sec	Extended ⁽⁶⁾
		ISD33150I	139.8	162.0	sec	Industrial ⁽⁶⁾
		ISD33180	172.4	186.7	sec	Commercial ⁽⁶⁾
		ISD33180D	172.4	188.5	sec	Extended ⁽⁶⁾
		ISD33180I	167.8	194.5	sec	Industrial ⁽⁶⁾
		ISD33240	229.9	248.9	sec	Commercial ⁽⁶⁾
		ISD33240D	229.9	251.3	sec	Extended ⁽⁶⁾
		ISD33240I	223.7	259.3	sec	Industrial ⁽⁶⁾
T _{PUD}	Power-Up Delay	ISD33120	23.9	26.0	msec	Commercial
		ISD33120D	23.9	26.2	msec	Extended
		ISD33120I	23.3	27.0	msec	Industrial
		ISD33150	29.9	32.4	msec	Commercial
		ISD33150D	29.9	32.7	msec	Extended
		ISD33150I	29.1	33.8	msec	Industrial
		ISD33180	35.9	38.9	msec	Commercial
		ISD33180D	35.9	39.3	msec	Extended
		ISD33180I	34.9	40.5	msec	Industrial
		ISD33240	47.9	51.9	msec	Commercial
		ISD33240D	47.9	52.4	msec	Extended
		ISD33240I	46.6	54.0	msec	Industrial
T _{STOP} OR T _{PAUSE}	Stop or Pause in Record or Play	ISD33120		25.0	msec	
		ISD33150		31.25	msec	
		ISD33180		37.5	msec	
		ISD33240		50.0	msec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
T _{RAC}	RAC Clock Period	ISD33120	143.7		155.6	msec	Commercial ⁽¹⁰⁾
		ISD33120D	143.7		157.1	msec	Extended ⁽¹⁰⁾
		ISD33120I	139.8		162.0	msec	Industrial ⁽¹⁰⁾
		ISD33150	179.6		194.5	msec	Commercial ⁽¹⁰⁾
		ISD33150D	179.6		196.3	msec	Extended ⁽¹⁰⁾
		ISD33150I	174.7		202.6	msec	Industrial ⁽¹⁰⁾
		ISD33180	215.5		233.3	msec	Commercial ⁽¹⁰⁾
		ISD33180D	215.5		235.6	msec	Extended ⁽¹⁰⁾
		ISD33180I	209.7		243.1	msec	Industrial ⁽¹⁰⁾
		ISD33240	287.3		311.1	msec	Commercial ⁽¹⁰⁾
		ISD33240D	287.3		314.1	msec	Extended ⁽¹⁰⁾
		ISD33240I	279.6		324.1	msec	Industrial ⁽¹⁰⁾
T _{RACLO}	RAC Clock Low Time	ISD33120	11.9		13.0	msec	Commercial
		ISD33120D	11.9		13.1	msec	Extended
		ISD33120I	11.6		13.5	msec	Industrial
		ISD33150	14.9		16.2	msec	Commercial
		ISD33150D	14.9		16.4	msec	Extended
		ISD33150I	14.5		16.9	msec	Industrial
		ISD33180	17.9		19.5	msec	Commercial
		ISD33180D	17.9		19.7	msec	Extended
		ISD33180I	17.4		20.3	msec	Industrial
		ISD33240	23.9		26.0	msec	Commercial
		ISD33240D	23.9		26.2	msec	Extended
		ISD33240I	23.3		27.0	msec	Industrial
T _{RACM}	RAC Clock Period in Message Cueing Mode	ISD33120		187.50		μsec	
		ISD33150		234.40		μsec	
		ISD33180		281.25		μsec	
		ISD33240		375.00		μsec	
T _{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD33120		15.62		μsec	
		ISD33150		19.56		μsec	
		ISD33180		23.42		μsec	
		ISD33240		31.34		μsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
V _{IN}	ANA IN Input Voltage				32	mV	Peak-to-Peak ^{(4) (8) (9)}

1. Typical values @ T_A = 25°C and 3.0 V.

2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.

3. Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).

4. Single-ended input mode. In the differential input mode, V_{IN} max. for ANA IN+ and ANA IN- is 16 mV peak-to-peak.

5. For greater stability, an external clock can be utilized (see Pin Descriptions).

6. Minimum and maximum limits are guaranteed by ISD via 100 percent electrical testing or characterization to meet or exceed a Cpk of 1.33.

7. Filter specification applies to the antialiasing filter and to the smoothing filter.

8. The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.

9. For optimal signal quality, this maximum limit is recommended.

10. When a record command is sent, T_{RAC} = T_{RAC} + T_{RACLO} on the first row addressed.

Table 8: Absolute Maximum Ratings (Die)⁽¹⁾

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V _{SS} – 0.3 V) to (V _{CC} + 0. V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V _{SS} – 1.0 V) to (V _{CC} + 1.0 V)
Voltage applied to MOSI, SLK, INT, RAC and SS pins (Input current limited to ±20 mA)	(V _{SS} – 1.0 V) to 5.5 V
V _{CC} – V _{SS}	–0.3 V to +7.0 V

1. Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V _{CC}) ⁽¹⁾	+2.7 V to +3.3 V
Ground voltage (V _{SS}) ⁽²⁾	0 V

1. V_{CC} = V_{CCA} = V_{CCD}

2. V_{SS} = V_{SSA} = V_{SSD}.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
V _{IL}	Input Low Voltage			V _{CC} × 0.2	V	
V _{IH}	Input High Voltage	V _{CC} × 0.8		3.3 ⁽³⁾	V	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 10 μA
V _{OL1}	RAC, INT Output Low Voltage			0.4	V	I _{OL} = 1 mA
V _{OH}	Output High Voltage	V _{CC} – 0.4			V	I _{OH} = –10 μA
I _{CC}	V _{CC} Current Operating) — Playback — Record		25 30	30 40	mA mA	R _{EXT} = ∞ ⁽⁴⁾ R _{EXT} = ∞ ⁽⁴⁾
I _{SB}	V _{CC} Current (Standby)		1	10	μA	(4) (5)
I _{IL}	Input Leakage Current			±1	μA	
I _{HZ}	MISO Tristate Current		1	10	μA	
R _{EXT}	Output Load Impedance	5			KΩ	
R _{ANA IN +}	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	

Table 10: DC Parameters (Die)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
R _{ANA IN-}	ANA IN- Input Resistance	40	56	71	K Ω	
A _{ARP}	ANA IN+ or ANA IN- to AUD OUT Gain		25		dB	⁽⁶⁾

1. Typical values @ $T_A = 25^\circ\text{C}$ and 3.0 V.
2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. When driven by a 5-volt microcontroller, the maximum V_{IH} for the MOSI, SCLK, and $\overline{SS}$ pins is 5.5 volts.
4. V_{CCA} and V_{CCD} connected together.
5. $\overline{SS} = V_{CCA} = V_{CCD}$, XCLK = MOSI = $V_{SSA} = V_{SSD}$ and all other pins floating.
6. Measured with AutoMute feature disabled.

Table 11: AC Parameters (Die)

Symbol	Characteristic	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
F _S	Sampling Frequency	ISD33120	8.0		KHz	⁽⁵⁾
		ISD33150	6.4		KHz	⁽⁵⁾
		ISD33180	5.3		KHz	⁽⁵⁾
		ISD33240	4.0		KHz	⁽⁵⁾
F _{CF}	Filter Pass Band	ISD33120	3.4		KHz	3dB Roll-Off Point ^{(3) (7)}
		ISD33150	2.7		KHz	3dB Roll-Off Point ^{(3) (7)}
		ISD33180	2.3		KHz	3dB Roll-Off Point ^{(3) (7)}
		ISD33240	1.7		KHz	3dB Roll-Off Point ^{(3) (7)}
T _{REC}	Record Duration	ISD33120	115.1	124.4	sec	^{(5) (6)}
		ISD33150	143.8	155.5	sec	^{(5) (6)}
		ISD33180	172.6	186.6	sec	^{(5) (6)}
		ISD33240	229.3	249.9	sec	^{(5) (6)}
T _{PLAY}	Playback Duration	ISD33120	115.1	124.4	sec	^{(5) (6)}
		ISD33150	143.8	155.5	sec	^{(5) (6)}
		ISD33180	172.6	186.6	sec	^{(5) (6)}
		ISD33240	229.3	249.9	sec	^{(5) (6)}
T _{PUD}	Power-Up Delay	ISD33120	23.9	26.0	msec	⁽⁶⁾
		ISD33150	29.9	32.4	msec	⁽⁶⁾
		ISD33180	35.9	38.9	msec	⁽⁶⁾
		ISD33240	47.7	52.1	msec	⁽⁶⁾
T _{STOP} or T _{PAUSE}	Stop or Pause in Record or Play	ISD33120	25.0		msec	
		ISD33150	31.25		msec	
		ISD33180	37.5		msec	
		ISD33240	50.0		msec	
T _{RAC}	RAC Clock Period	ISD33120	143.8	155.5	msec	^{(6) (10)}
		ISD33150	179.7	194.4	msec	^{(6) (10)}
		ISD33180	215.6	233.2	msec	^{(6) (10)}
		ISD33240	286.6	312.3	msec	^{(6) (10)}

Table 11: AC Parameters (Die)

Symbol	Characteristic	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
T _{RACLO}	RAC Clock Low Time	ISD33120	12.50		msec	(6)
		ISD33150	15.63		msec	(6)
		ISD33180	18.75		msec	(6)
		ISD33240	25.0		msec	(6)
T _{RACM}	RAC Clock Period in	ISD33120	187.5		μsec	
	Message Cueing	ISD33150	234.4		μsec	
	Mode	ISD33180	281.3		μsec	
		ISD33240	375.0		μsec	
T _{RACML}	RAC Clock Low Time	ISD33120	15.6		μsec	
	in Message Cueing	ISD33150	19.5		μsec	
	Mode	ISD33180	23.4		μsec	
		ISD33240	31.3		μsec	
THD	Total Harmonic Distortion		1	2	%	@ 1 KHz
V _{IN}	ANA IN Input Voltage			32	mV	Peak-to-Peak ^{(4) (8) (9)}

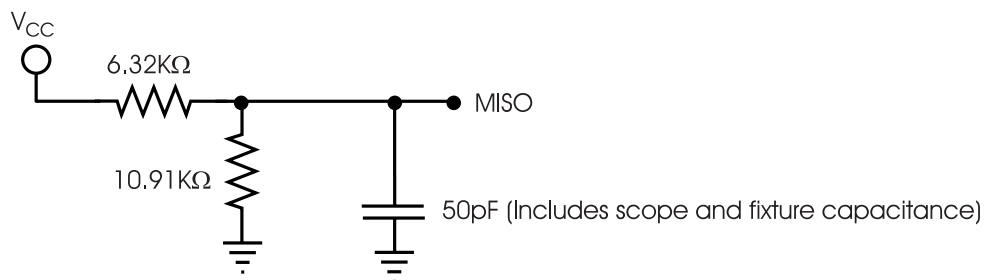
1. Typical values @ $T_A = 25^\circ\text{C}$ and 3.0 V.
2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).
4. Single-ended input mode. In the differential input mode, V_{IN} maximum for ANA IN+ and ANA IN- is 1.6 mV peak-to-peak.
5. For greater stability, an external clock can be utilized. See "PIN DESCRIPTIONS" on page 2.
6. Minimum and maximum limits are guaranteed by ISD via 100 percent electrical testing or characterization to meet or exceed a Cpk of 1.33.
7. Filter specification applies to the antialiasing filter and to the smoothing filter.
8. The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.
9. For optimal signal quality, this maximum limit is recommended.
10. When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACLO}$ on the first row addressed.

Table 12: SPI AC Parameters⁽¹⁾

Symbol	Characteristics	Min	Max	Units	Conditions
T _{SSS}	SS Setup Time	500		nsec	
T _{SSH}	SS Hold Time	500		nsec	
T _{DIS}	Data in Setup Time	200		nsec	
T _{DIH}	Data in Hold Time	200		nsec	
T _{PD}	Output Delay		500	nsec	
T _{DF} ⁽²⁾	Output Delay to hiZ		500	nsec	
T _{SSmin}	SS HIGH	1		μsec	
T _{SCKhi}	SCLK High Time	400		nsec	
T _{SCKlow}	SCLK Low Time	400		nsec	
F ₀	CLK Frequency		1,000	KHz	

1. Typical values @ T_A = 25°C and 3.0 V. Timing measured at 50 percent of the V_{CC} level.

2. Tristate test condition.



TIMING DIAGRAMS

Figure 5: Timing Diagram

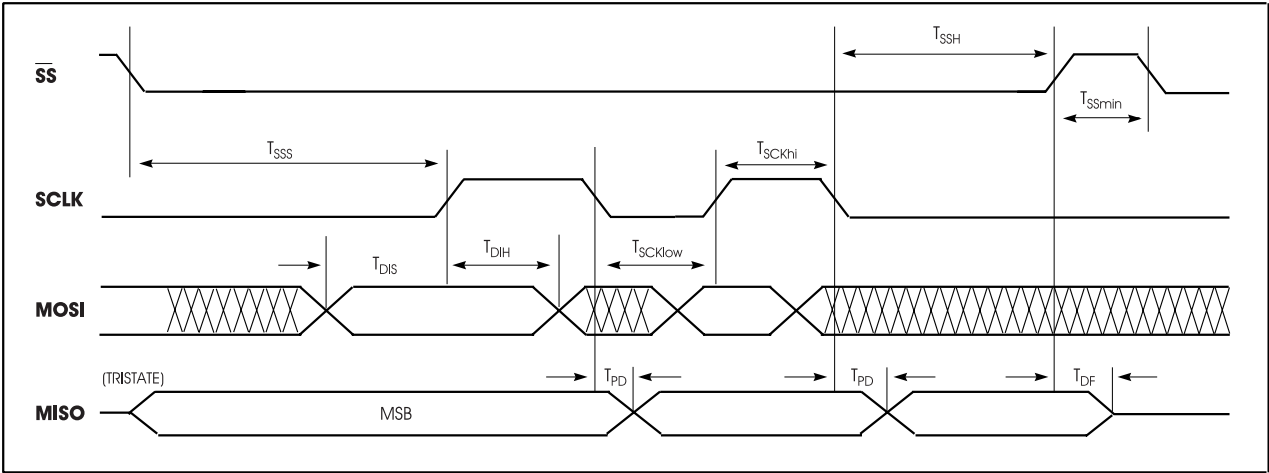


Figure 6: 8-Bit Command Format

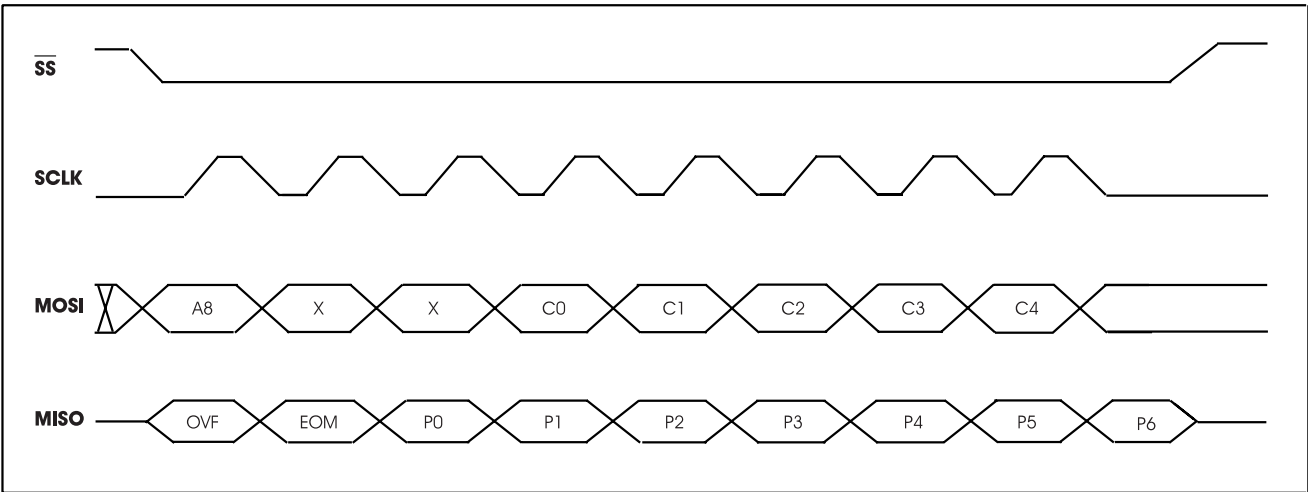


Figure 7: 16-Bit Command Format

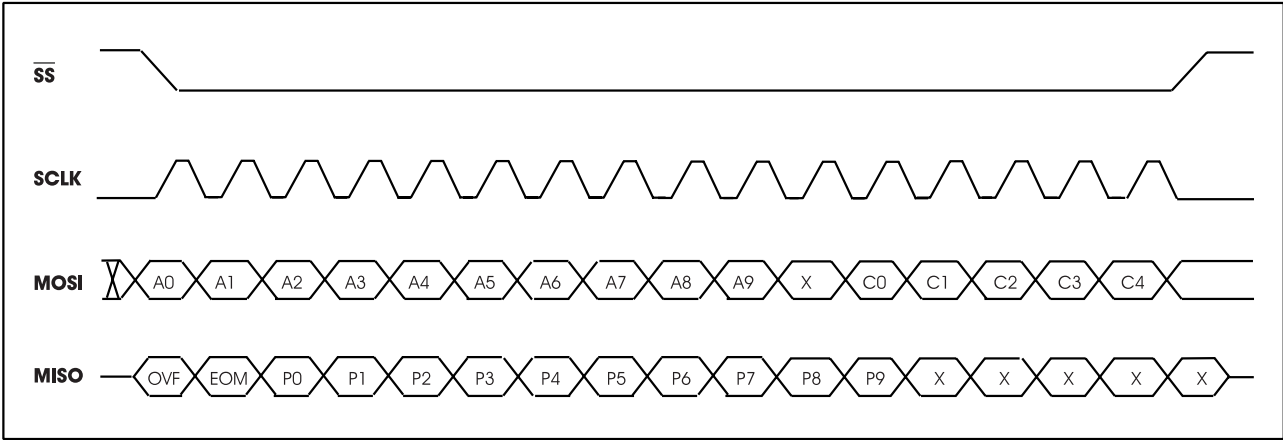


Figure 8: Playback/Record and Stop Cycle

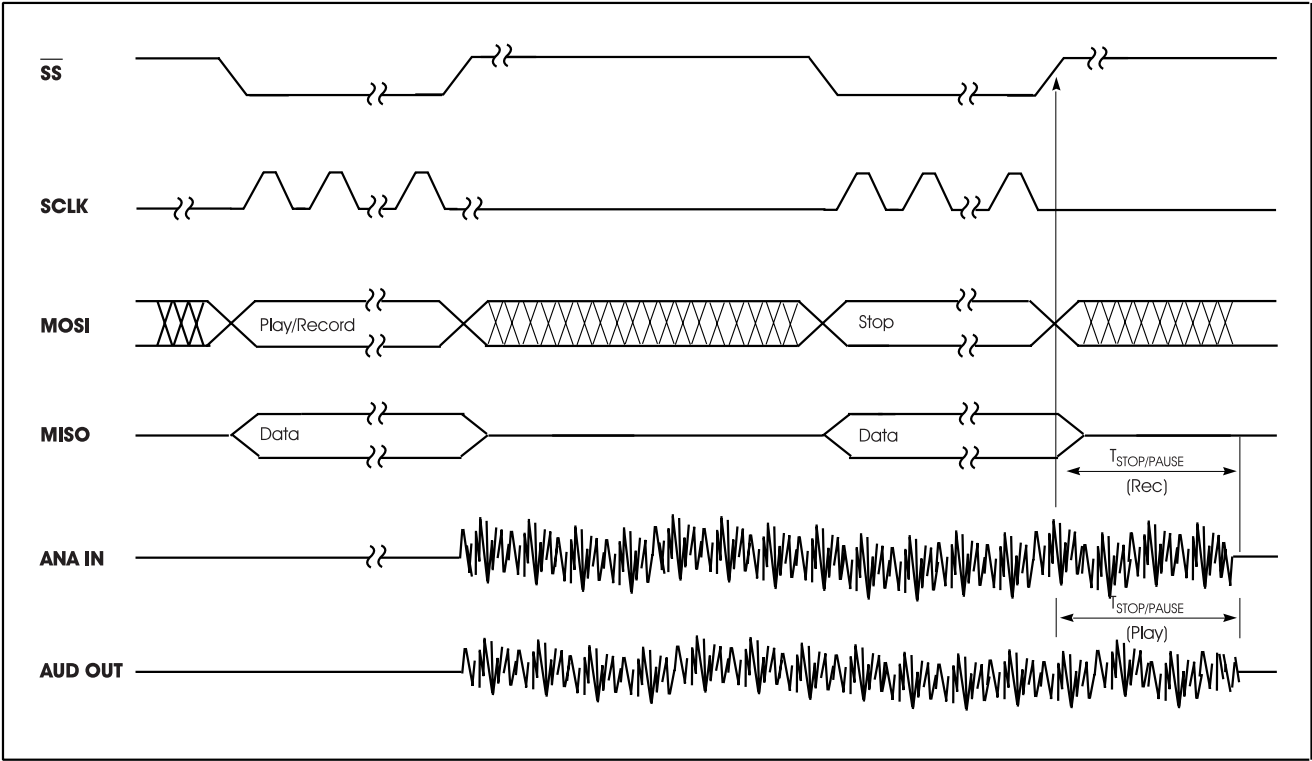
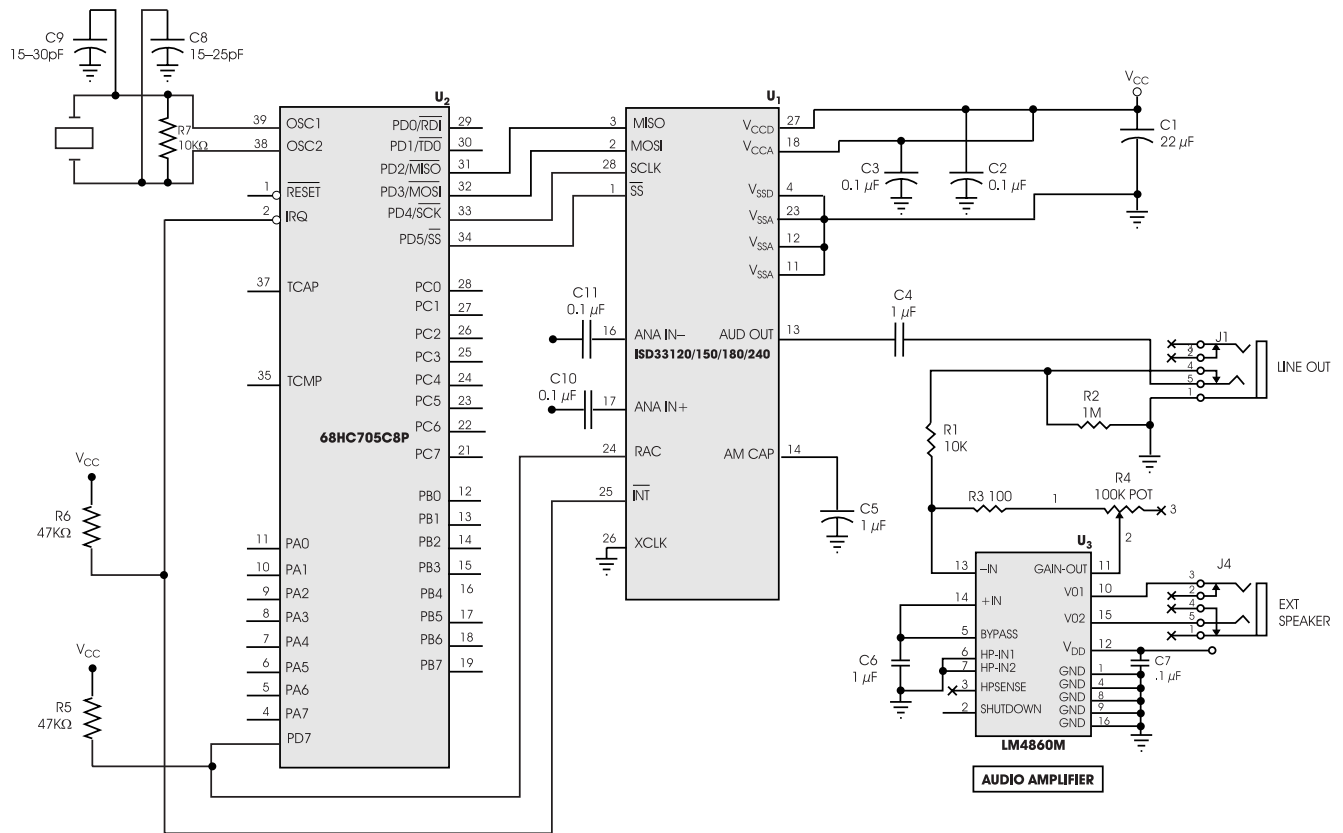
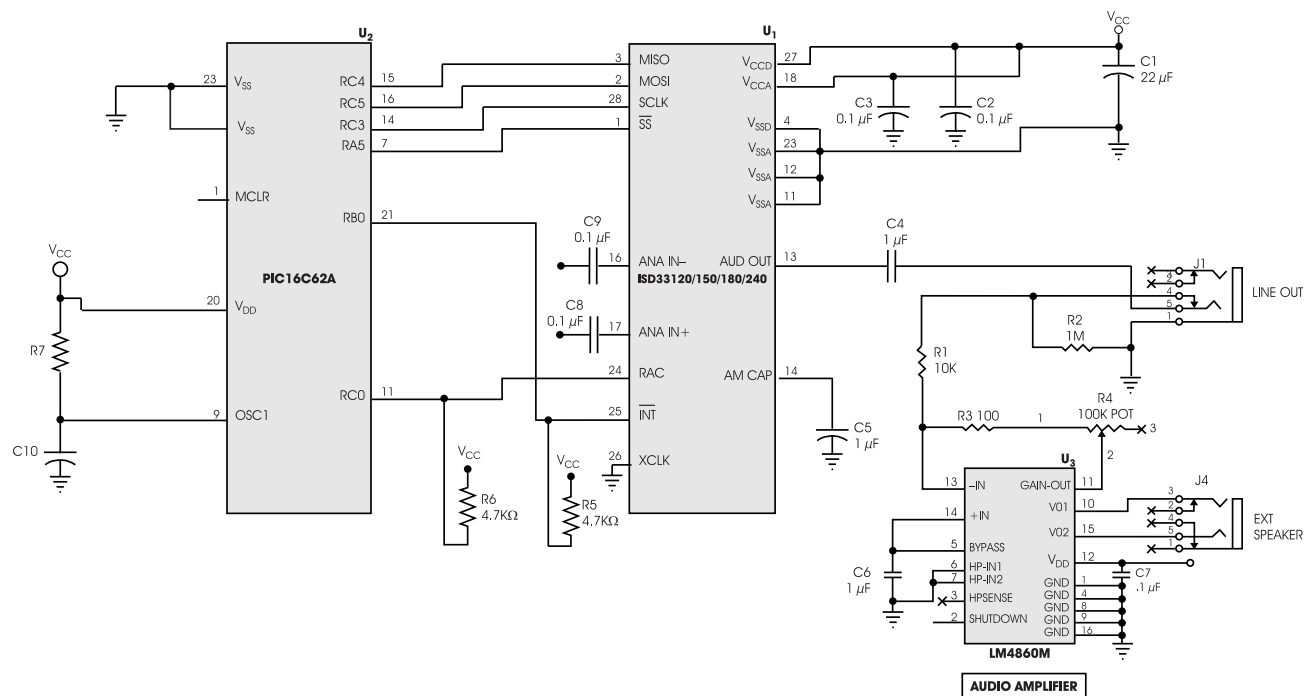


Figure 9: Application Example Using SPI



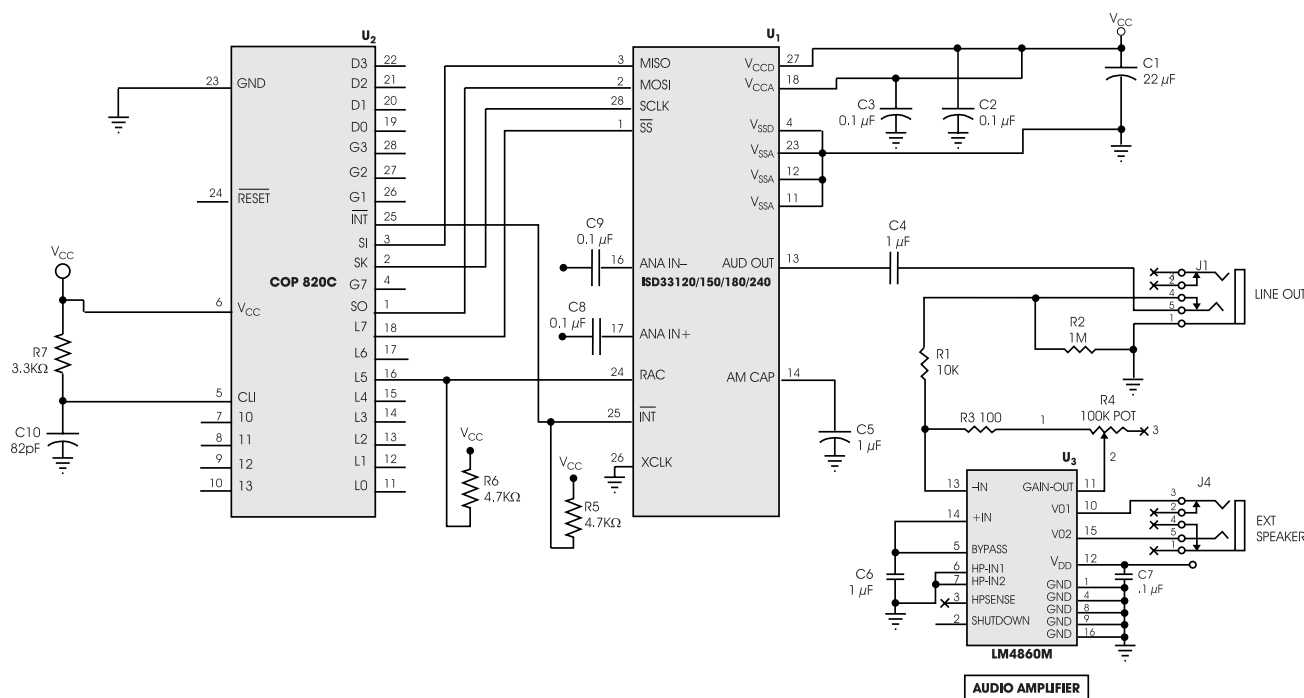
NOTE: This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.

Figure 10: Application Example Using Microwire



1. This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.

Figure 11: Application Example Using SPI Port on Microcontroller



NOTE: This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.

DEVICE PHYSICAL DIMENSIONS

Figure 12: 28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type I (E)

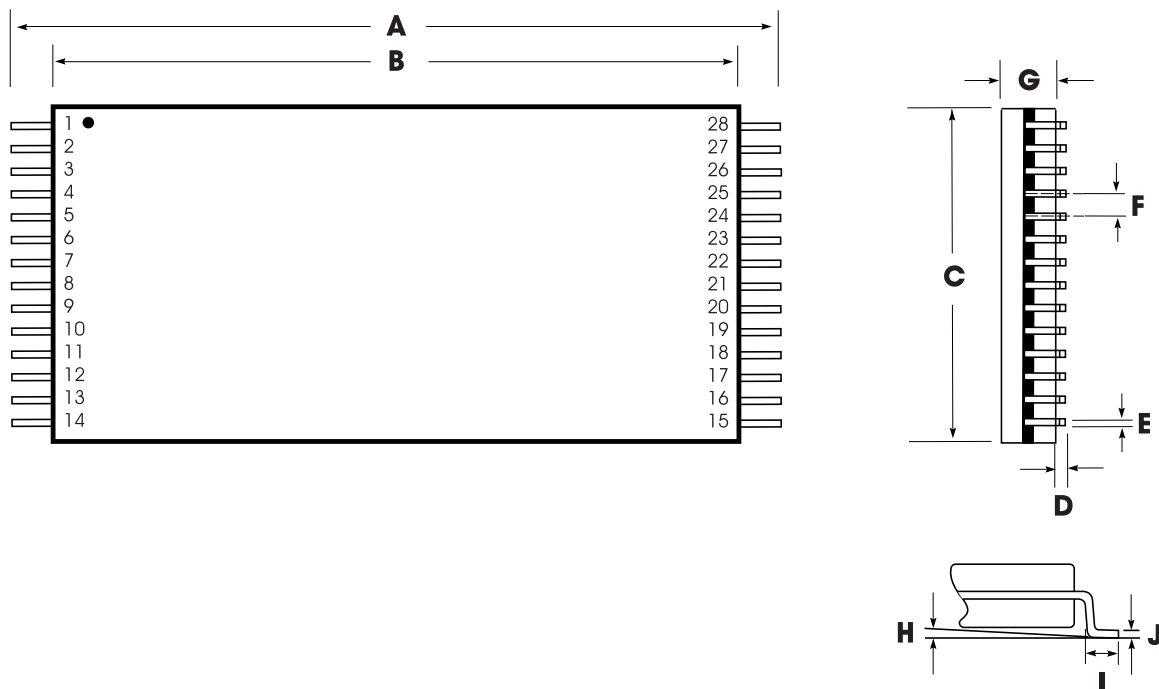


Table 13: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

NOTE: Lead coplanarity to be within 0.004 inches.

Figure 13: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

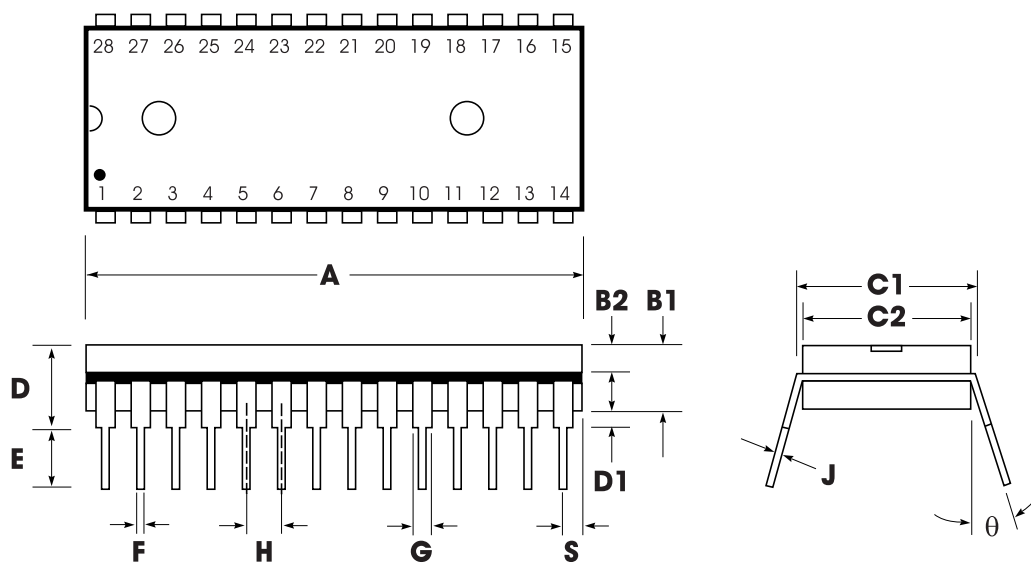
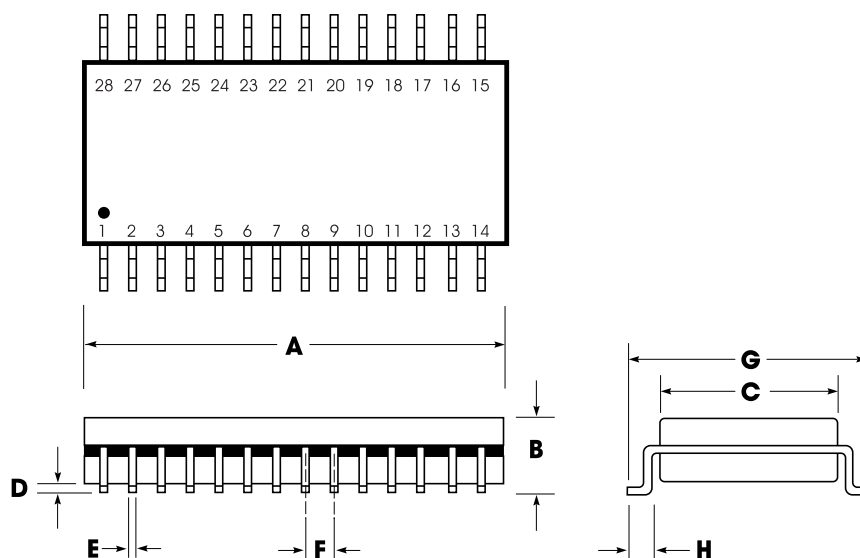


Table 14: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

Figure 14: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)**Table 15: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions**

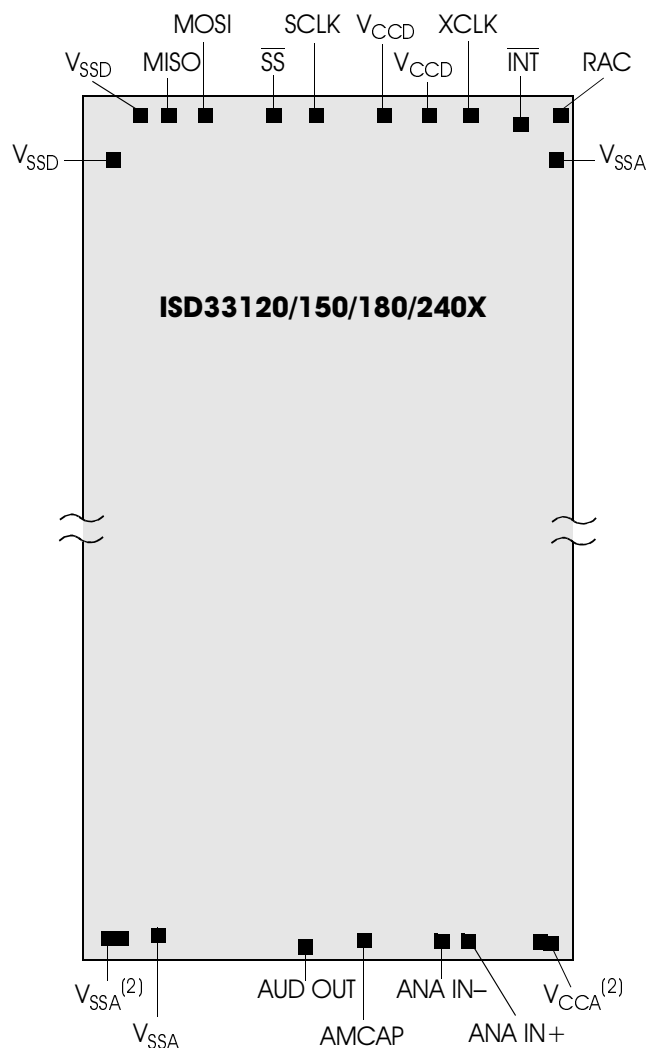
	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: Lead coplanarity to be within 0.004 inches.

Figure 15: ISD33120/150/180/240 Products Bonding Physical Layout⁽¹⁾ (Unpackaged Die)

ISD33120/150/180/240X

- I. Die Dimensions
X: 188 ± 1 mils
Y: 324 ± 1 mils
- II. Die Thickness
 $11.8 \pm .4$ mils
- III. Pad Opening (min)
109 microns (4.3 mils)



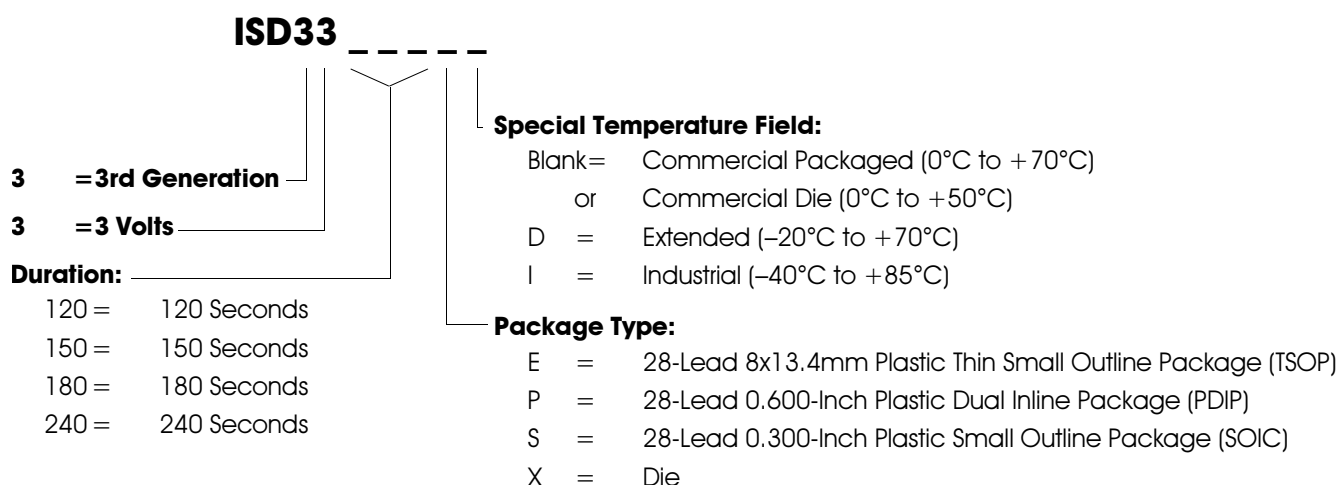
1. The backside of the die is internally connected to V_{SS} . It **MUST NOT** be connected to any other potential or damage may occur.
2. Double bond recommended.

**Table 16: ISD33120/150/180/240 Devices PIN/PAD Designations,
with Respect to Die Center (μm)**

Pin	Pin Name	X Axis	Y Axis
V _{SSA}	V _{SS} Analog Power Supply	-2120.0	-3894.8
V _{SSA}	V _{SS} Analog Power Supply	-1807.8	-3891.3
AUD OUT	Audio Output	104.7	-3905.1
AMCAP	AutoMute	619.5	-3903.3
ANA IN -	Inverting Analog Input	1686.3	-3878.0
ANA IN +	Noninverting Analog Input	1857.8	-3878.0
V _{CCA}	V _{CC} Analog Power Supply	2117.9	-3884.3
V _{SSA}	V _{SS} Analog Power Supply	2153.2	3385.9
RAC	Row Address Clock	2158.8	3890.3
$\overline{\text{INT}}$	Interrupt	1848.0	3890.3
XCLK	External Clock Input	1068.7	3901.5
V _{CCD}	V _{CC} Digital Power Supply	841.1	3908.1
V _{CCD}	V _{CC} Digital Power Supply	587.7	3862.3
SCLK	Slave Clock	-66.3	3900.8
$\overline{\text{SS}}$	Slave Select	-294.2	3900.8
MOSI	Master Out Slave In	-1022.1	3900.8
MISO	Master In Slave Out	-1510.3	3888.5
V _{SSD}	V _{SS} Digital Power Supply	-2000.3	3908.1
V _{SSD}	V _{SS} Digital Power Supply	-2196.3	3721.9

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD33000 series devices, please refer to the following part numbers, which are supported in volume for this product series. Consult the local ISD Sales Representative or Distributor for availability information.

Part Number	Part Number	Part Number	Part Number
ISD33120E	ISD33150E	ISD33180E	ISD33240E
ISD33120ED	ISD33150ED	ISD33180ED	ISD33240ED
ISD33120EI	ISD33150EI	ISD33180EI	ISD33240EI
ISD33120P	ISD33150P	ISD33180P	ISD33240P
ISD33120PD	ISD33150PD	ISD33180PD	ISD33240S
ISD33120PI	ISD33150PI	ISD33180PI	ISD33240X
ISD33120S	ISD33150S	ISD33180S	
ISD33120SD	ISD33150SD	ISD33180SD	
ISD33120SI	ISD33150SI	ISD33180SI	
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