TH8053

Low Speed CAN Transceiver

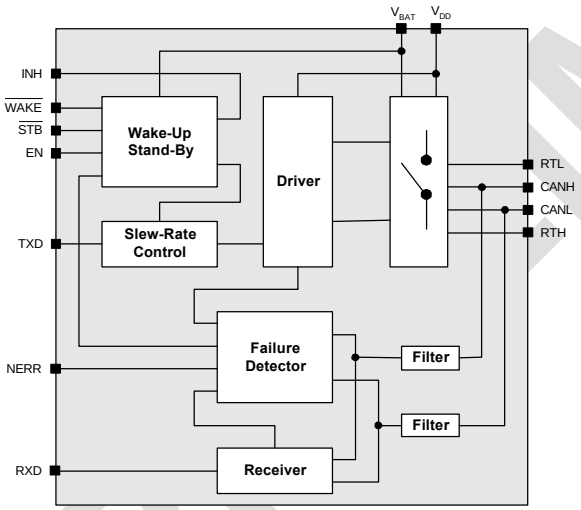
Features and Benefits

- Baud rate up to 125k Baud
- Up to 40 nodes can be connected
- Supports unshielded bus wire
- Very low RFI
- Integrated receiver filters
- Permanent dominant monitoring of transmit data input
- Good immunity to EMC

Ordering Information

Part No.	Temperature Suffix	Package	Temperature Range
TH8053	L	L	-40C to 125C Automotive

Functional Diagram



Description

The TH8053 is a fault tolerant CAN -transceiver which works as an interface between the CAN protocol controller and the physical CAN bus. It is designed to connect up to 40 control nodes in passenger cars with an overall cable length of up to 80 meters enabling data transmission/reception rates up to 125kBaud using unshielded bus wires.

In normal operation mode the device supports the high security differential transmit capability of the differential CAN bus. In the recessive state, data from the bus is converted to a single-ended signal, filtered and fed to the RXD output pin from the CAN controller (reception of data). In the dominant state, data sent from the controller to pin TXD drives the CAN bus lines.

The device automatically switches to an appropriate single ended mode in the event of a bus failure which allows further function of the control network. If the failure is corrected, the TH8053 automatically resets itself to normal operation. Furthermore, it enable single ended transmission on wires with a ground shift up to 1.5V. The TH8053 also ensures transception if the system contains a single unpowered mode (e.g. a missing termination resistor).

Another feature is the monitoring of the TXD-input to prevent the controller from obstructing the CAN bus by sending a permanent dominant state. The presence of any of these errors is indicated by a LOW-signal at the NERR-pin.

STANDBY and SLEEP modes enable low current consumption if no transmit capability is needed, or if the supply voltages drop under a specified level. A wake-up function recalls the normal operation mode whenever a slope is detected at the /WAKE-Pin or data on the bus occurs.

Other important automotive features are the low RF-interference due to a limitation of rise and fall slopes as well as the immunity to RF-radiation achieved by integrated receiver filters.

A thermal shut-down circuit prevents the TH8053 from any damage caused by increased power consumption of the output stages while all other parts of the circuit remain working.

The TH8053's bus connections (CANH, CANL) are short-circuit proof to battery and ground voltage as well as any pin is protected against ESD-Events.

Functional Description

The signal from the differential CAN bus is fed to a filter stage to inhibit high frequencies that would normally interfere with incoming bus data. The cut-off frequency of the filters has to be regarded as a trade-off between RF-suppression and propagation delay. The failure detection circuit determines whether one of the failures described in (Definition in ccordance with ISO 11519-2), exists and indicates a present error as an active LOW at the NERR output. The information of the type of failure detected is given to the failure management block which takes the appropriate measures to ensure transmission and reception of data. This includes the control of the correct termination of the CAN bus lines as well as the choice of the right derivation of the receiver signal (output to the RXD-pin) from the CANH and CANL inputs. The failure management also contains the possibility to disable one of the driver stages (e. g. in the case of failure 6 the high-side driver and the RTH termination are disabled to reduce current consumption). During any kind of single-wire transception RF-radiation and RF-sensitivity are increased.

The failure detection consists of two detection circuits, one being active in the normal operation mode and the other one working in the standby and sleep modes. Recovery of the failures is done with a certain time-out that depends on the failure. A wake-up function that detects incoming dominant signals from the bus is also included.

A wake-up command can also be generated by changing the logical voltage level at the WAKE-pin. The mode the transceiver is running within and whether the INH-pin disables an external voltage regulator can be controlled by the EN-and STB-pins as shown in Table 3 – Mode Control. Another feature offered in this CAN transceiver device is the time-out circuit at the TXD-Input that prevents occupation of the CAN bus by a long-term dominant signal sent from the CAN controller. If no failure occurs the TXD-signal coming from the CAN controller is fed to the driver stage which includes a limitation of slopes to reduce RF-interference caused by radiation on the CAN bus.

To prevent the chip from a thermal breakdown, a temperature protection circuit shuts down the driver stages which represent the biggest part oft the whole power consumption. All other parts remain active thus a reception of data is still possible. After cooling down and reaching the low temperature level the transmitter will be enabled again.

Table 1 - CAN bus failures

(Definition in ccordance with ISO 11519-2)

Nr.	Failure description	Condition
1	CANL wire interrupted	
2	CANH wire interrupted	
3	CANL short-circuited to battery supply voltage	V_{BAT}>7.2
3a		V1.8V<V_{BAT}<7.2V
4	CANH short-circuited to ground	
5	CANL short-circuited to ground	
6	CANH short-circuited to battery supply voltage	V_{BAT}>7.2 V
6a		1.8V<V_{BAT}<7.2V
7	CANH short-circuited to CANL	

Error Management

Depending on the occurring error, appropriate measures have to be taken to ensure data transmission and reception. Table 2 - Error Management lists the means to achieve this goal within the normal operation mode. The comparator signal that determines the value of RXD is given in the second column, the third and fourth ones contain the information whether either one of the terminations R_{TH} or R_{TL} is switched off to reduce the current flowing in the termination resistances. The last two columns display if one of the transmitter drivers is deactivated.

Errors 1 and 3a as well as errors 2 and 4 can't be distinguished by the receiver. In failure cases 1 and 3a the received signal from the CANL wire has got a voltage near or at V_{DD}-level, in the case of failures 2 or 4 the CANH wire is bound to ground level

Table 2 - Error Management

Error	Output to RXD	Termination[1]		Driver	
		RTH	RTL	CANH	CANL
1	D	on	on	on	on
2	D	on	on	on	on
3	H	on	off	on	off
3a	D	on	on	on	off[2]
4	L	on	on	off[3]	on
5	H	on	off	on	off
6	L	off	on	off	on
6a	L	off	on	off	on
7	H	on	off	on	off

[1] If the termination is switched off, a current of 75µA is supplied at the RTH -or RTL-pin.
[2] Low side driver is switched off after two unsuccessful attempts of reaching dominant level.
[3] High side driver is switched off after two unsuccessful attempts of reaching dominant level.

Error Management (continued)

If an interruption of the CANH or CANL wire between two MCUs is detected (failures 1 and 2) there is no need to disable the corresponding high or low side driver because differential transmission towards other MCUs may still be useful. To confirm that a bus wire is interrupted, the transmitter is switched on and the receiver observes if the according wire changes its state. After two unsuccessful attempts of reaching the dominant level, the high side driver (failure 4) or the low side driver (failure 3a) is disabled.

Operation Modes

The different operation modes can be selected by the signals provided at the EN-and /STB-pins. There are three operation modes which enable reduced power consumption: the sleep mode, the VBAT-standby mode and the VDD-standby mode.
The sleep mode (/STB=0, EN=0) has the lowest power consumption because the entire chip including the external voltage regulator is disabled. This mode can only be reached if an intermediate mode (/STB=0, EN=1) is entered which is interpreted as "go-to-sleep"-command. Otherwise, the chip switches to the VBAT-standby mode (/STB=0, EN=0) where the external voltage regulator remains active. In these modes - (go-to-sleep, sleep, VBAT-standby), the RTL-pin is switched to VBAT.
If the external voltage regulator does not provide the VDD-supply voltage, or if the device is operating in the VBAT-standby mode (external voltage regulator is active) a wake-up request from either the /WAKE-pin or the CAN bus line is visible as an active LOW at the NERR and RXD output. If VDD has been switched off in the sleep mode, the wake-up request will cause the TH8053 to enter the VBAT-standby mode as an intermediate state in which the VDD-supply is present again and so the wake-up can be observed at the NERR-and RXD-pins as well.
Another mode is the VDD-standby mode (/STB=1, EN=0).
Similar to the normal operation mode the RTL-pin is switched to VDD. The appearance of a wake-up condition in this mode is only displayed at the RXD output as an active LOW. The NERR output is used to indicate the drop of VBAT below 1V. This warn flag is necessary to show that VBAT was missing and that a reinstallation has to be done. It is reset to HIGH when the device enters the normal operation mode in which the NERR-pin is used to indicate bus failures.
During the low power modes (sleep, VBAT-and VDD-standby) the detection of errors is reduced to the monitoring of the occurence of failures 5, 6 and 7.
A complete deactivation of the detection circuit is not neccessary because the occurrence of failures 5, 6 and 7 would result in an increased power consumption.
The TH8053 switches itself to the VBAT-standby mode if VDD is missing or below the threshold. If VDD is missing the EN and /STB inputs will be held internally at LOW level to prevent the chip from entering an inappropriate mode (fail safe functionality).
In all standby modes, the TH8053 is able to receive interrupts. During the first, the normal operation time of the go-to-sleep command and the specified time after switching from mode to the standby modes the device ignores an interrupt.

Table 3 -Mode Control

/STB	EN	Mode	INH	NERR	RXD	RTL
0	0	V_{BAT}-standby[1]	high / V_{BAT}	active LOW wake-up interrupt signal if V_{DD} is present		switched to V_{BAT}
0	0	sleep[2]	floating			switched to V_{BAT}
0	1	go-to-sleep command	floating			switched to V_{BAT}
1	0	V_{DD}-standby[3]	high/ V_{BAT}	active LOW missing V_{BAT} flag	active LOW wake-up interrupt	switched to V_{DD}
1	1	normal operation	high/ V_{BAT}	active LOW error flag	HIGH = recessive bus; LOW = dominant bus	switched to V_{DD}

[1] Wake-up interrupts are released when the normal operation mode is entered
[2] Sleep mode will be entered instead of V_{BAT}-standby mode if the go-to-sleep command was applied before. (EN may turn LOW as V_{DD} drops without affecting internal functions because of fail safe functionality.)
[3] The "missing V_{BAT}" flag will be reset to HIGH when the normal operation mode is entered

Power-on procedure

The chip automatically enters the V_{BAT}-standby mode because of its fail safe functionality. In the V_{BAT}- normal operation. This way the CAN controller will be shown by the power on flag that is has to reinitialise the MCU (e.g. after exchanging the complete CAN unit or after a battery voltage breakdown).
Due to special design circuitry the CAN bus is not loaded if V_{BAT}=0V which ensures data transception on the bus even if some MCUs are unpowered.

Electrical Characteristics

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so.Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the TH8053 is only specified within the limits shown in "Operating conditions"

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit	Notes
DC supply voltage	V_{CC}	-0.3	+6.0	V	
Battery voltage	V_{Bat}	-0.3	+27	V	
			40		1
DC Input voltage at pins 2 to 6	V_{2-6}	-0.3	V_{CC} + 0.3	V	
CANH, CANL input voltage	$V_{CANH,L}$	-10	27	V	2
		-40	40		3
CANH, CANL transient input voltage	$V_{CANH, L, tran}$	-150	100	V	
Termination resistance at pins 8 and 9	$R_{TH,}$ R_{TL}	500	16000	Ω	4
DC input voltage at pin 1, 8, 9	$V_{1,8,9}$	-0.3	V_{BAT}+0.3	V	
DC input voltage at pin 7	V_{WAKE}		V_{BAT}+0.3	V	
DC input current at pin 7	I_{WAKE}	-15		mA	
Maximum latch-up free current at any pin	$I_{Latch-up}$	-500	+500	mA	
Electrostatic discharge voltage at any pin	V_{ESD}	-2000	+2000	V	5
Electrostatic discharge voltage at pin CANH and CANL	V_{ESDCAN}	-4000	+4000	V	6
Storage temperature range	T_{STG}	-55	+150	°C	
Junction temperature	T_{Junc}	-40	+150	°C	7
Thermal Resistance from junction to ambient	R_{Th}		120	K/W	

[1] t < 500ms; load dump
[2] V_{CC}=0 to 5.5V; V_{BAT}>0 V; t<0.1; no time limit
[3] V_{CC}=0 to 5.5V; V_{BAT}>0 V; t<0.1 ms; load dump
[4] R_{TH} connects pin 8 and 11, R_{TL} connects pin 9 and 12 (e.g. see Figure. 4 - Application Circuitry.
[5] For a human body model (equivalent to discharging 100pF with 1.5kΩ).
[6] For a human body model (equivalent to discharging 100pF with 1.5kΩ).

TH8053 Operating Conditions

Parameter	Symbol	Min	Max	Unit	Notes
DC supply voltage	V_{DD}	4.75	5.25	V	
Battery voltage	V_{BAT}	6	27	V	
Operating ambient temperature	T_{amb}	-40	+125	°C	
Junction temperature	T_{junc}	-40	+150	°C	[1]

TH8053 Static Characteristics

V_{DD}= 4.75 to 5.25V, V_{Bat} = 6 to 27V, T_{amb} = 40 to +125°C, V_{STB} =V_{DD}

Parameter	Sym-bol	Condition	Min	Typ	Max	Unit
Supply						
Supply current	I_{CC}	recessive, normal operation mode, TXD=V_{DD}		**4**	8	mA
		dominant, normal operation mode, no load, TXD=0V		**10**	20	mA
supply current	I_{BAT}	sleep mode, V_{DD}=0V, V_{BAT}=12V,T_{amb}<90°C		**15**	40	µA
Supply current	I_{CC}+I_{BAT}	V_{DD}-standby mode, V_{DD}=5V, V_{BAT}=12V, T_{amb}<90°C		**120**	500	µA
		V_{BAT}-standby mode, V_{DD}=5V, V_{BAT}=12V, T_{amb}<90°C		**55**	95	µA
Battery voltage for setting power-on flag	$V_{BAT, pwon}$	standby and sleep modes			1	V
Supply voltage	V_{DD}	fail safe forced V_{BAT} standby mode	2.75		4.5	V
CANH, CANL						
Differential receiver threshold voltage re-cessive to dominant	V_{diffRX}	no bus failure and bus failure 1,2, 4	-2.8	**-2.5**	-2.2	V
Differential receiver threshold voltage do-minant to recessive			-3.2	**-2.9**	-2.6	V
Single-ended receiver threshold of CANL	V_{CANLse}	bus failures 4, 6, 6a	2.8	**3.1**	3.4	V
Single-ended receiver threshold of CANH	V_{CANHse}	bus failures 3, 5, 7	1.5	**1.85**	2.2	V
CANH recessive out-put voltage	$V_{CANHrec}$	TXD=V_{DD}, R_{TH}<4k	0.1	**0.2**	0.3	V
CANH dominant out-put voltage	$V_{CANHdom}$	TXD=0V, normal operation mode, I_{CANH}=-40mA	V_{DD} -1.4		V_{DD}	V
CANL dominant out-put voltage	$V_{CANLdom}$	TXD=0V, normal operation mode, I_{CAN}=40mA		**1.1**	1.4	V
CANH output current	I_{CANH}	V_{CANH}=0V, TXD=0V	-120	**-80**	-50	mA
		sleep mode, V_{CANH}=12V		**0**		µA

[1] Junction temperature is defined in IEC 747-1

TH8053 Static Characteristics (Continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CANL output current	I_{CANL}	V_{CANL}=12V, TXD=0V	50	**80**	120	mA
		sleep mode, V_{CANH}=0V, V_{BAT}=12V		**0**		µA
Threshold for detection of short circuit between CANH or CANL and battery	$V_{HLBATdet}$	normal operation mode	6.5	**7.3**	8.0	V
Threshold for detection of short-circuit between CANH and battery	$V_{HBATdet}$	standby and sleep modes	V_{BAT}-2.5	**V_{BAT}-2**	V_{BAT} -1	V
CANH wake-up voltage	V_{Hwu}	standby and sleep modes	1.2	**1.9**	2.7	V
CANL wake-up voltage	V_{Lwu}	standby and sleep modes	2.4	**3.1**	3.8	V
difference of wake-up thresholds	V_{Lwu}-V_{Hwu}	standby and sleep modes	0.2			V
CANH leakage current	$I_{CANHleak}$	V_{DD}=0V, V_{BAT}=0V, V_{CANL}=13.5 V, R_{TL}=100, T_{junc}<85°C		**0**	5	µA
CANL leakage current	$I_{CANLleak}$	V_{DD}=0V, V_{BAT}=0V, V_{CANH}=5V, R_{TL}=100, T_{junc}<85°C		**0**	5	µA
RTH, RTL						
RTL to V_{DD} switch -on resistance	R_{RTL}	normal operation mode, I_0= -10mA		**43**	95	
		V_{DD} standby mode, $\|I_0\|$<1mA		**15**	75	
RTL to V_{BAT} switch-on resistance		V_{BAT} standby or sleep mode	8	**12.5**	23	k
RTH to ground switch -on resistance	R_{RTH}	normal operation mode, I_0=10mA		**43**	95	
RTH output voltage	V_{RTH}	standby and sleep modes, $\|I_0\|$<1mA		**0.7**	1	V
RTL output voltage	V_{RTL}	V_{DD}-standby mode, $\|I_0\|$<1mA	V_{DD}-1	**V_{DD}-0.7**		V
RTL pull-up current	I_{RTLpu}	normal operation mode, bus failures 3, 3a, 5, 7; V_{RTL}=3.4V	-45	**-75**	-110	µA
RTH leakage current	$I_{RTHleak}$	V_{DD}=0V, V_{BAT}=0V, V_{CANH}=5V, R_{TL}=100, T_{junc}<85°C		**0**	5	µA
RTL leakage current	$I_{RTLleak}$	V_{DD}=0V, V_{BAT}=0V, V_{CANL}=13.5V, R_{TL}=100, T_{junc}<85°C		**0**	5	µA

TH8053 Static Characteristics (Continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
/STB, EN, TXD						
HIGH level input voltage	V_{INhigh}	rising edge (input with Schmitt-Trigger)	0.7 V_{DD}		V_{DD}+0.3	V
LOW level input voltage	V_{INlow}	falling edge (input with Schmitt-Trigger)	-0.3		0.3 V_{DD}	V
HIGH level input current at pins /STB and EN	I_{INhigh}	V_{INhigh}=4V		**9**	20	µA
LOW-level input current at pins /STB and EN	$I_{IN, low}$	V_{INlow}=1V	4	**8**		µA
HIGH level input current at pin TXD	I_{INhigh}	V_{INhigh}=4V	-200	**-50**	-25	µA
LOW level input current at pin TXD	I_{INlow}	V_{INlow}=1V	-800	**-250**	-100	µA
RXD, NERR						
HIGH level output voltage	$V_{OUThigh}$	I_O= -100µA (NERR)	V_{DD} -0.9		V_{DD}	V
		I_O= -250µA (RXD)				
LOW level output voltage	V_{OUTlow}	I_O= -1.25mA	0		0.9	V
/WAKE						
Threshold for wake up	V_{WAKE}	V_{STB}=0V	2.4	**3.1**	4.0	V
input current	I_{WAKE}	V_{STB}=0V	-3	**-2**		µA
INH						
HIGH level voltage drop $V_{dropphigh}$ =V_{BAT}-V_{INH}	$V_{dropphigh}$	I_{INH}= -0.18mA		**0.5**	0.8	V
Leakage current	$I_{leaklow}$	sleep mode, V_{INH}=0V	-5.0		5.0	µA
Thermal Protection						
Junction temperature to shut down the CANH, CANL drivers	T_{juncsd}		150	**165**	180	°C

TH8053 Dynamic Characteristics

The Devices R1, C1 and C2 which values are given in the Column "Condition" of the table below refer to the test-schematic schown in Figure 3, "Test Circuit for Dynamic Characteristics"
For the definition of propagation delay and transitions times see Figure. 1 –TH8053 Timing Diagram

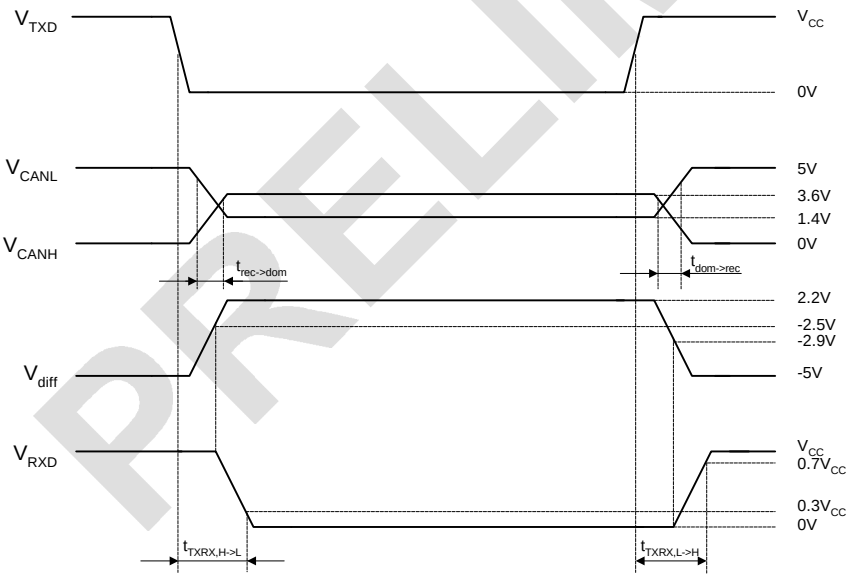
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transition time of CANH and CANL from recessive to dominant	$t_{rec-dom}$	10% to 90%, C_1=10nF, C_2=0, R_1=100	0.6	1	2	µs
Transition time of CANH and CANL from dominant to recessive	$t_{dom-rec}$	10% to 90%, C_1=1nF, C_2=0, R_1=100	0.5	0.8	1.3	µs
Propagation delay from TXD to RXD for H-L-transitions (recessive to dominant)	$t_{TXRXH-L}$	C_1=100pF, C_2=0, R_1=100, no bus failures and bus failures 1, 2, 3a, 4		0.8	1.5	µs
		C_1=C_2=3.3nF, R_1=100, no bus failures and bus failures 1, 2, 3a, 4		0.8	1.5	µs
		C_1=100pF, C_2=0, R_1=100, bus failures 3, 5, 6, 6a, 7		1.2	1.8	µs
		C_1=C_2=3.3nF, R_1=100, bus failures 3, 5, 6, 6a, 7		1.2	1.8	µs
Propagation delay from TXD to RXD for L-H-transitions (dominant to recessive)	$t_{TXRXL-H}$	C_1=100pF, C_2=0, R_1=100, no bus failures and bus failures 1, 2, 3a, 4		1.5	2.0	µs
		C_1=C_2=3.3nF, R_1=100, no bus failures and bus failures 1, 2, 3a, 4		2.2	3.0	µs
		C_1=100pF, C_2=0, R_1=100, bus failures 3, 5, 6, 6a, 7		0.9	1.5	µs
		C_1=C_2=3.3nF, R_1=100, bus failures 3, 5, 6, 7		1.4	2.1	µs
CANH or CANL minimum dominant time for wake-up	$t_{CANHLwu}$	standby or sleep modes, V_{BAT}=12V	8	20	35	µs
Minimum change time of / WAKE for wake up	$t_{WAKEmin}$	standby or sleep modes, V_{BAT}=12V	8	20	35	µs
Disable time of permanent dominant TXD timer	t_{TXDdis}	normal operation mode and all bus failures	1	2.5	4.0	ms
Low time of missing battery voltage for setting power-on flag	t_{pwon}	standby and sleep modes		0.2	1	s
Differemce of edge count between CANH and CANL for detection of failures 1, 2, 3a, 4	Δec_{fail}	normal operation mode		4		
Differemce of edge count between CANH and CANL for recovery of failures 1, 2, 3a, 4	Δec_{rec}	normal operation mode		2		

TH8053 Dynamic Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Detection time of failure 3, 6	$t_{faildet}$	normal operation mode	10		60	µs
6a			2	5	8	ms
5, 7			0.75	2	4.0	ms
5, 6, 6a, 7		standby and sleep modes, V_{BAT}=12V	0.8	4	8.0	ms
recovery time of failure 3	$t_{fail,rec}$	normal operation mode	150	400	750	µs
5, 6, 6a, 7			20	40	60	µs
5, 6, 6a, 7		standby & sleep modes, V_{BAT}=12 V		4		µs
Time for settling the normal operation mode from any other mode	$t_{nmsettle}$	V_{BAT}=12V		40		µs
Time for leaving the normal operation mode to any other mode	$t_{nm,leave}$	V_{BAT}=12V		80		µs

TH8053 Timing

Figure. 1 –TH8053 Timing Diagram



TH8053 Circuit Examples

Figure. 3 - Application Circuit

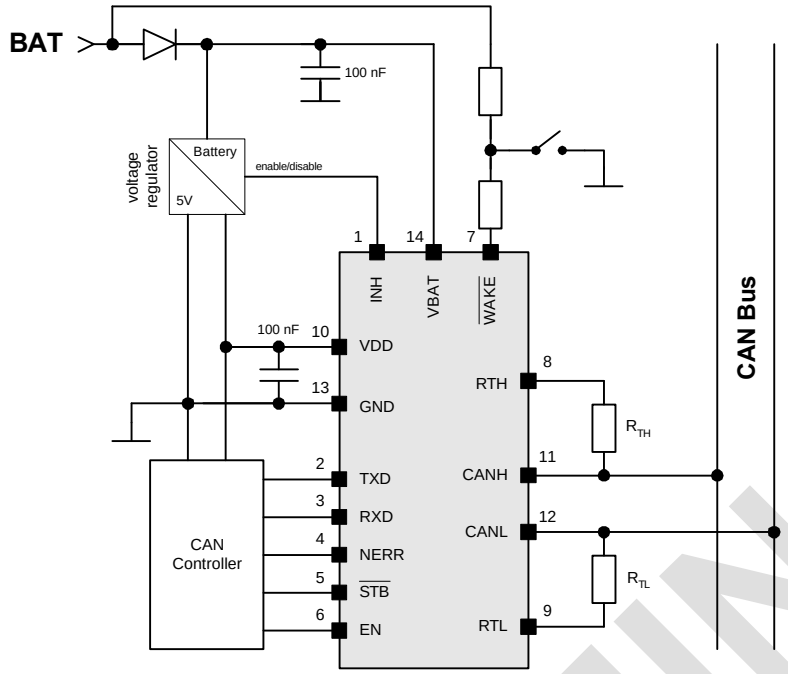
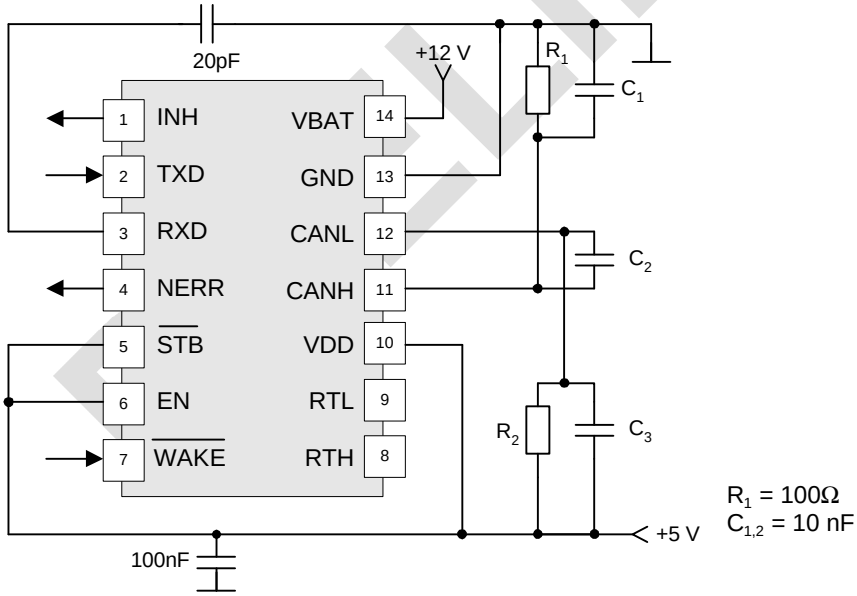
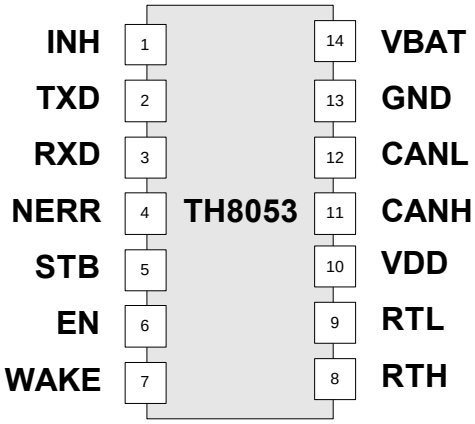


Figure. 2 - Test circuit for dynamic characteri-



TH8053 Pin Description

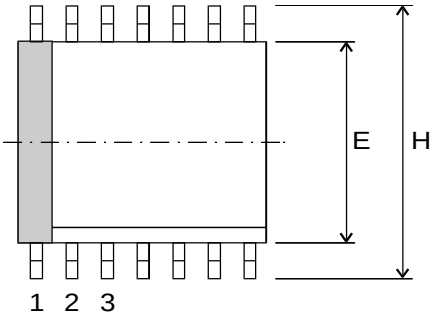


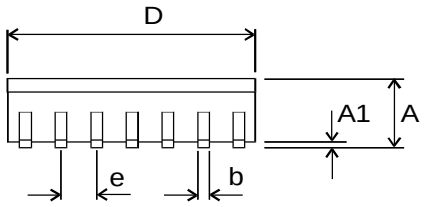
Pin	Name	I/O	Function
1	INH	O	inhibit output for switching external 5V regulator
2	TXD	I	transmit data input
3	RXD	O	receive data output
4	NERR	O	error output pin
5	STB	I	not standby digital control input
6	EN	I	enable digital control input
7	WAKE	I	not wake input signal
8	RTH		termination resistor for CANH
9	RTL		termination resistor for CANL
10	VDD		supply voltage (+5)
11	CANH	I/O	high signal bus line
12	CANL	I/O	low signal bus line
13	GND		ground
14	VBAT		battery voltage

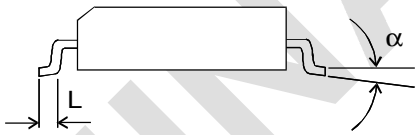
TH8053 Mechanical Specifications

”L” Package Dimensions

Note: All Dimension in millimeters







Package ”L”

Small Outline Integrated Circiut (SOIC), SO 14, 150 mil

All Dimension in mm, coplanarity < 0.1 mm									
	D	**E**	**H**	**A**	**A1**	**e**	**b**	**L**	**a**
min	8.55	3.80	5.80	1.35	0.10	1.27	0.33	0.40	0°
max	8.75	4.00	6.20	1.75	0.25		0.51	1.27	8°
All Dimension in inch, coplanarity < 0.004”									
min	0.337	0.150	0.228	0.053	0.004	0.050	0.013	0.016	0°
max	0.334	0.157	0.224	0.069	0.010		0.020	0.050	8°

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