FEATURES

- **Full Four-Quadrant Multiplication**
- **12-Bit Endpoint Linearity (±1/2 LSB)**
- **Pretrimmed Gain**
- **TTL/CMOS Compatible**
- **Low Power Consumption**
- **Low Feedthrough Error**
- **Direct Replacement for AD7521 and AD7541**
- **Superior Power Supply Rejection from +5V to +15V**
- **Low Gain and Linearity Tempcos (TYP 2ppm of FSR/°C)**
- **Latch-Up Resistant**
- **Available in Die Form**

APPLICATIONS

- **Digital/Synchro Conversion**
- **Programmable Amplifiers**
- **Ratiometric A/D Conversion**
- **Function Generator**
- **CRT Graphics Generator**
- **Digitally-Controlled Attenuator**
- **Digitally-Controlled Power Supplies**
- **Digital Filters**

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7541AX PM7541BX	AD7541TD AD7541SD	MILITARY
PM7541EX PM7541FX	AD7541BD AD7541AD	INDUSTRIAL
PM7541GP PM7541FP	AD7541KN AD7541JN	COMMERCIAL

GENERAL DESCRIPTION

The PMI PM-7541 is a 12-bit, 4-quadrant multiplying digital-to-analog converter. It is manufactured using an advanced oxide-isolated, silicon-gate, monolithic CMOS technology.

Laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity and excellent absolute accuracy. The low power dissipation, together with NMOS temperature-compensating switches, assures the performance over the full temperature range. It is a pin-compatible replacement for Analog Devices AD7521 and AD7541 with equal or better performance.

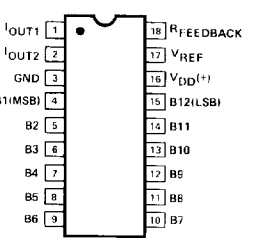
ORDERING INFORMATION †

	PACKAGE: 18-PIN		
LINEARITY	MILITARY* TEMPERATURE −55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE −40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
1 LSB	PM7541BX	PM7542FX	–
1/2 LSB	PM7541AX	PM7541EX	PM7541GP
1 LSB	–	PM7541FP	–

For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

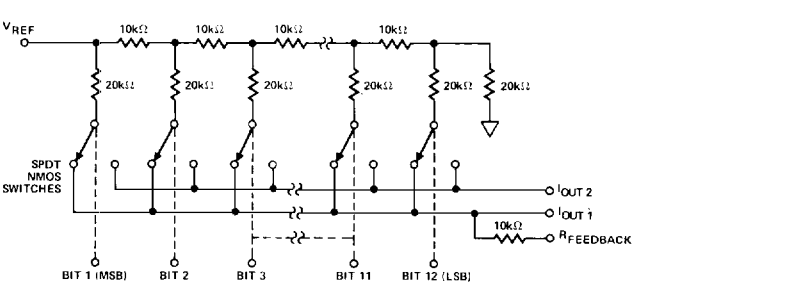
PIN CONNECTIONS



18-PIN EPOXY DIP (P-Suffix)

18-PIN HERMETIC DIP (X-Suffix)

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} (to GND) ..... ±17V
V_{REF} (to GND) ..... ±25V
V_{RFB} (to GND) ..... ±25V
Digital Input Voltage Range ..... V_{DD} to GND
Output Voltage (Pin 1, Pin 2) ..... –0.3V to V_{DD}
Operating Temperature Range
AX/BX Versions ..... –55°C to +125°C
EX/FX/FP Versions ..... –25°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
18-Pin Hermetic DIP (X)	79	11	°C/W
18-Pin Plastic DIP (P)	70	30	°C/W

NOTES:

1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified fo device in socket for CerDIP and P-DIP packages.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any ter minal except V_{REF} (Pin 17) and R_{FB} (Pin 18).
3. The digital control inputs are zener protected; however, permanent damag may occur on unprotected units from high energy electrostatic fields. Kee units in conductive foam at all times until ready to use.
4. Use proper anti-static handling procedures.
5. Absolute Maximum Ratings apply to both packaged devices and DICE Stresses above those listed under Absolute Maximum Ratings may caus permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, GND = 0V, $V_{OUT\,1}$ = $V_{OUT\,2}$ = 0V; and T_A = –55°C to +125°C apply for PM-7541AX/BX; T_A = –40°C to +85°C apply for PM-7541EX/FX/FP, and T_A = 0°C to +70°C apply for PM-7541GP, unless otherwise noted.

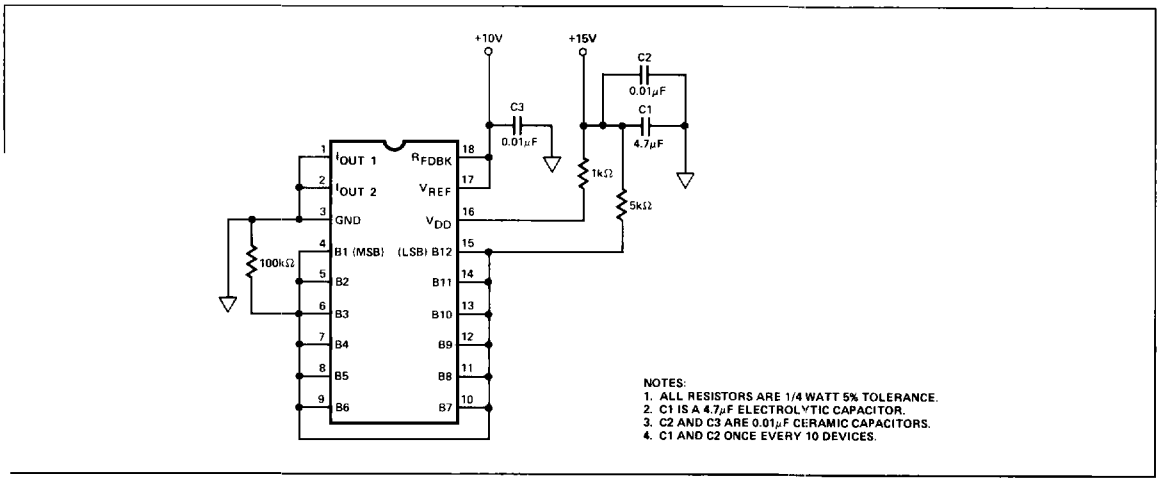
			PM-7541A/E/G			PM-7541B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Nonlinearity (Notes 1, 2)	INL		—	—	±1/2	—	—	±1	LSB
Gain Error (Notes 3, 4)	G_{FSE}	T_A = +25°C T_A = Full Temp. Range	— —	— —	±12.5 ±16.7	— —	— —	±12.5 ±16.7	LSB
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$	PSRR	V_{DD} = +14.5V to +15.5V T_A = +25°C T_A = Full Temp. Range	— —	— —	±0.01 ±0.02	— —	— —	±0.01 ±0.02	%/%
Output Leakage Current ($I_{OUT\,1}$) (Notes 5, 6)	I_{LKG}	T_A = +25°C T_A = Full Temp. Range	— —	— —	±50 ±200	— —	— —	±50 ±200	nA
DYNAMIC PERFORMANCE									
Output Current Settling Time (Note 7)	t_S	To ±1/2 LSB of FSR	—	—	1.0	—	—	1.0	µs
Feedthrough Error (Note 7)	FT	V_{REF} = 20V_{p-p} @ f = 10kHz All digital inputs low	—	—	2.0	—	—	2.0	mV_{p-p}
REFERENCE INPUT									
Input Resistance (Note 8)	R_{REF}		5	—	20	5	—	20	kΩ
DIGITAL INPUTS									
Digital Input High	V_{IH}		2.4	—	—	2.4	—	—	V
Digital Input Low	V_{IL}		—	—	0.8	—	—	0.8	V
Input Leakage Current	I_{IL}	V_{IN} = 0 to 15V	—	—	±1	—	—	±1	µA
Input Capacitance (Note 7)	C_{IN}		—	—	8	—	—	8	pF
Input Coding		(Tables 1, 2)	Binary or Offset			Binary or Offset			

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, GND = 0V, $V_{OUT\,1}$ = $V_{OUT\,2}$ = 0V; and T_A = −55°C to +125°C for apply PM-7541AX/BX; T_A = −40°C to +85°C apply for PM-7541EX/FX/FP, and T_A = 0°C to +70°C apply for PM-7541GP, unless otherwise noted. *Continued*

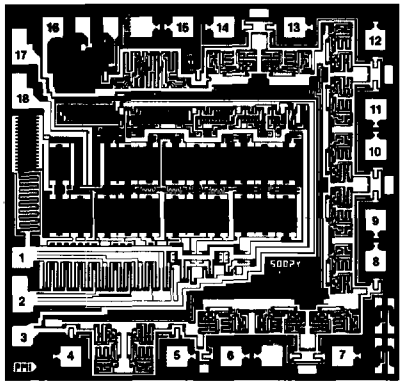
			PM-7541A/E/G			PM-7541B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG OUTPUTS									
Output Capacitance (Note 7)	$C_{OUT\,1}$ $C_{OUT\,2}$	Digital Inputs = V_{IH}	— —	85 30	200 60	— —	85 30	200 60	pF
Output Capacitance (Note 7)	$C_{OUT\,1}$ $C_{OUT\,2}$	Digital Inputs = V_{IL}	— —	30 85	60 200	— —	30 85	60 200	pF
POWER SUPPLY									
V_{DD} Range	V_{DD}	Accuracy is not guaranteed over this range.	+5	—	+16	+5	—	+16	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	—	—	2	—	—	2	mA

NOTES:
1. A/E/G versions are monotonic to 12-bits.
2. B/F/H versions are monotonic to 11-bits.
3. Using internal feedback resistor.
4. Maximum gain change from +25°C to T_{MAX} or T_{MIN} is ±4.2 LSB maximum.
5. Digital Inputs = V_{IL}.
6. Specification also applies for $I_{OUT\,2}$ with all digital inputs = V_{IH}.
7. Guaranteed and not tested.
8. Absolute temperature coefficient is approximately +300 ppm/°C.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils
(2.590 × 2.540 mm, 6.58 sq. mm)

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT (BIT 2)
6. DIGITAL INPUT (BIT 3)
7. DIGITAL INPUT (BIT 4)
8. DIGITAL INPUT (BIT 5)
9. DIGITAL INPUT (BIT 6)
10. DIGITAL INPUT (BIT 7)
11. DIGITAL INPUT (BIT 8)
12. DIGITAL INPUT (BIT 9)
13. DIGITAL INPUT (BIT 10)
14. DIGITAL INPUT (BIT 11)
15. DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16. POSITIVE POWER SUPPLY
17. REFERENCE INPUT VOLTAGE
18. INTERNAL FEEDBACK RESISTOR

WAFER TEST LIMITS at V_{DD} = +15V, V_{REF} = +10V, GND = 0V, $V_{OUT\,1}$ = $V_{OUT\,2}$ = 0V, T_A = +25°C.

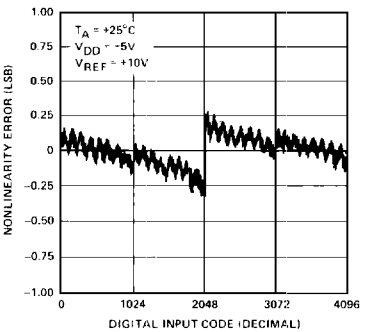
PARAMETER	SYMBOL	CONDITIONS	PM-7541G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Nonlinearity	INL		±1	LSB MAX
Gain Error (Note 1)	G_{FSE}		±12.5	LSB MAX
Power Supply Rejection	PSRR	V_{DD} = +14.5V to +15.5V	±0.01	%/% MAX
Output Leakage Current ($I_{OUT\,1}$) (Note 2)	I_{LKG}	Digital Inputs = V_{IL}	±50	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		5/20	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0 to 15V	±1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{iH} or V_{IL}	2	mA MAX

NOTES:
1. Using internal feedback resistor.
2. Specification also appl es for $I_{OUT\,2}$ but all Digital Inputs = V_{iH}.

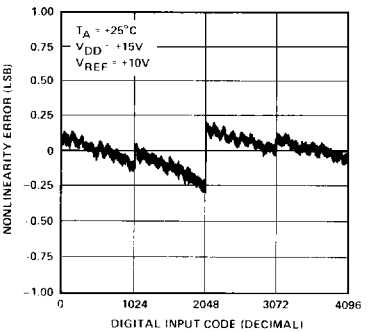
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guarantee for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

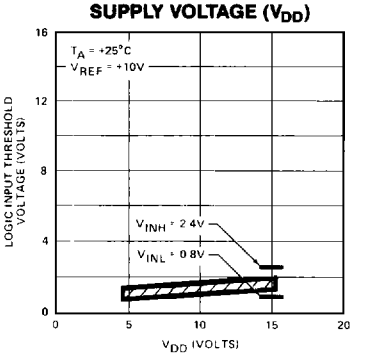
NONLINEARITY ERROR vs DIGITAL CODE



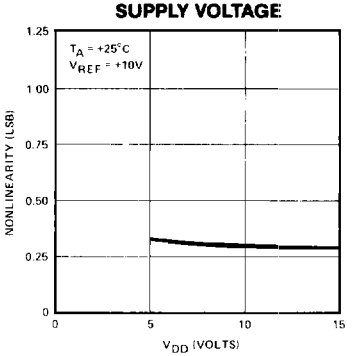
NONLINEARITY ERROR vs DIGITAL CODE



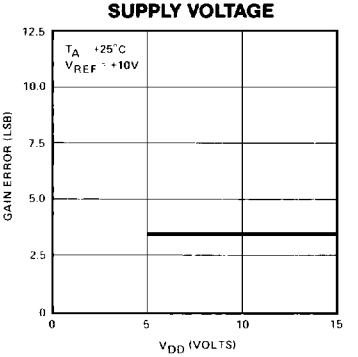
LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE (V_{DD})



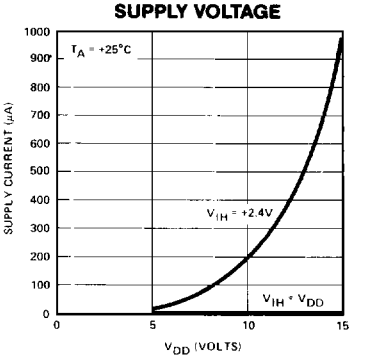
NONLINEARITY vs SUPPLY VOLTAGE



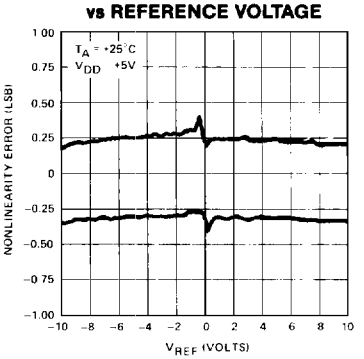
GAIN ERROR vs SUPPLY VOLTAGE



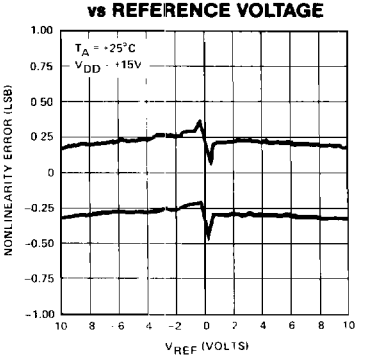
SUPPLY CURRENT vs SUPPLY VOLTAGE



NONLINEARITY ERROR vs REFERENCE VOLTAGE

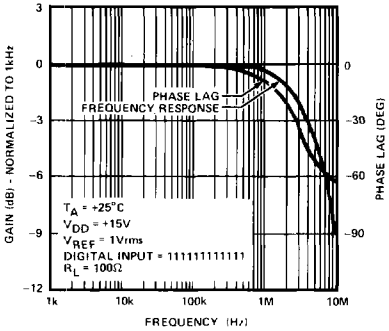


NONLINEARITY ERROR vs REFERENCE VOLTAGE

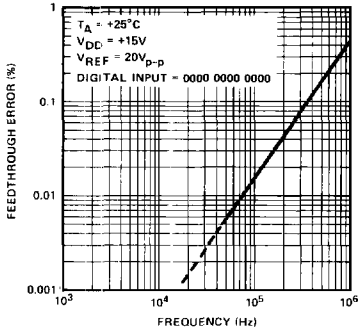


TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} PHASE LAG AND FREQUENCY RESPONSE



FEEDTHROUGH ERROR vs FREQUENCY



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus; i.e., zero to full scale.

GAIN

Ratio of the DAC's external-operational-amplifier output voltage to the V_{REF} input voltage.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from $I_{OUT\,1}$ or $I_{OUT\,2}$ terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on $I_{OUT\,1}$ terminal with all digital inputs LOW, or on $I_{OUT\,2}$ terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The PM-7541 is a 12-bit multiplying D/A converter consisting of a highly-stable, silicon-chrome thin film R-2R ladder network and twelve pairs of NMOS current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the PM-7541 is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\,1}$ and $I_{OUT\,2}$ BUS lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The design includes a matching switch in series with the feedback (R_{FB}) and terminating resistors. These switches (Figure 1) provide improved gain and linearity performance over the operating temperature range.

FIGURE 1: Simplified DAC Circuit

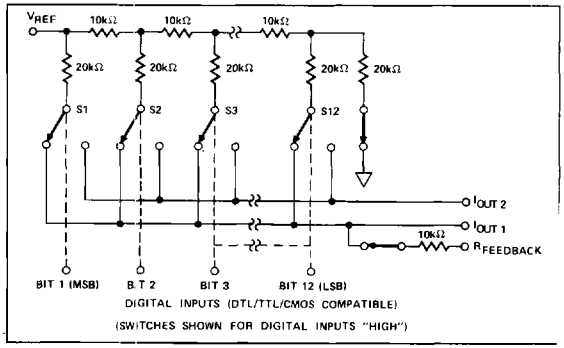
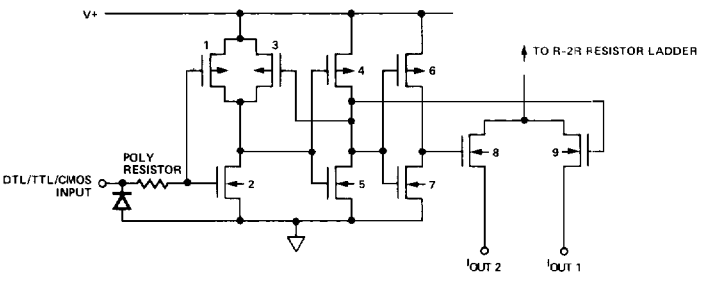


FIGURE 2: CMOS Switch



)ne of the twelve CMOS switches is shown in Figure 2. The igital input stage, devices 1, 2, and 3, drives the two inverters, evices 4, 5, 6, and 7; these inverters in turn drive the two output urrent steering switches, devices 8 and 9. Devices 1, 2, and 3 re designed such that the digital control inputs are DTL, TTL, nd CMOS compatible over the full military temperature range.

he twelve output current-steering switches are in series with ıe R-2R resistor ladder, and therefore, can introduce bit errors. is essential then, that the switch "ON" resistance be binarily :aled so that the voltage drop across each switch remains)nstant. If, for example, switch 1 of Figure 1 was designed with ı "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., then ith a 10 volt reference input, the current through switch 1 is 5mA, switch 2 is 0.25mA, etc., a constant 5mV drop will then ; maintained across each switch.

)UIVALENT CIRCUIT ANALYSIS

gures 3 and 4 show the equivalent circuits for all digital inputs)W and HIGH respectively. The reference current is switched $I_{OUT\,2}$ when all inputs are LOW and $I_{OUT\,1}$ when inputs are GH. The $I_{LEAKAGE}$ current source is the combination of rface and junction leakages to the substrate; the 1/4096 rrent source represents the constant 1-bit current drain ·ough the ladder terminating resistor. The output capacitance dependent upon the digital input code, and is therefore)dulated between the low and high values.

3URE 3: PM-7541 Equivalent Circuit (All Inputs LOW)

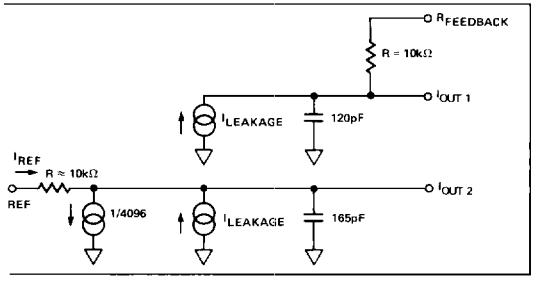
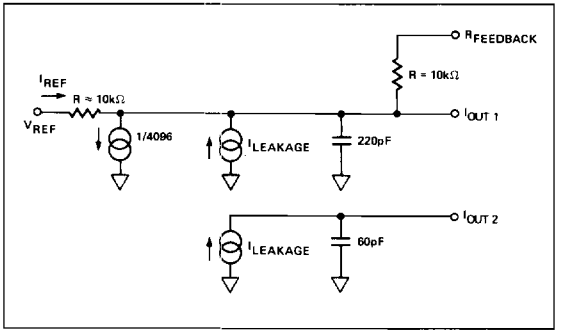


FIGURE 4: PM-7541 Equivalent Circuit (All Digital Inputs HIGH)



DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, is also modulated by the digital input code. The resistance looking back into the $I_{OUT\,1}$ terminal, may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). The static accuracy and dynamic performance will be affected by this modulation. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7541. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase Compensation (See Figures 5 and 6).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

Linearity depends upon the potential of $I_{OUT\,1}$ and $I_{OUT\,2}$ (pins 1 and 2) being exactly equal to GND (pin 3). In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, see Figures 5 and 6. The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifiers usual bias current compensation resistor in the noninverting input should not be used; the input should be connected directly to ground with a low-resistance wire. This resistor can cause a variable offset voltage contributing an error. All pins going to ground should be taken to a common point to avoid ground loops. The V_{DD} power supply should have a low noise level and not have transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD}; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge whenever the PC card is disconnected from the system.

OUTPUT AMPLIFIER CONSIDERATIONS

For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been pointed out that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

FIGURE 5: Unipolar Binary Operation (2-Quadrant)

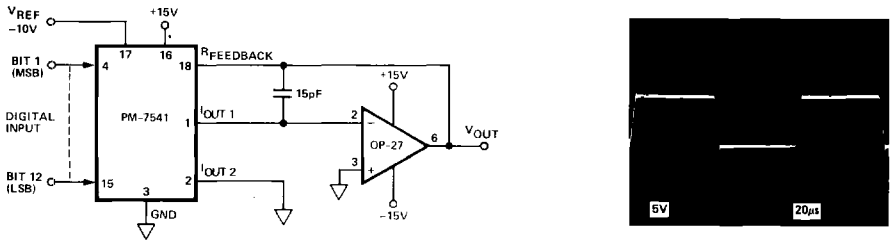
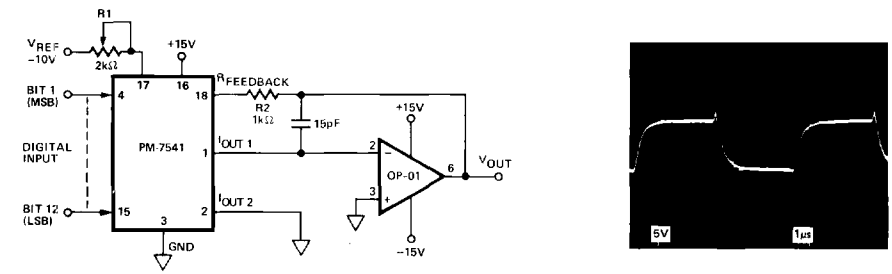


FIGURE 6: Unipolar Binary Operation (2-Quadrant)



The static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 8 and the equation:

$$\text{Error Voltage} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O = function of digital code.
$R_O \cong 10k\Omega$ for more than 4-bits of logic 1.
$R_O \cong 30k\Omega$ for any single bit logic 1.

Therefore, the offset gain varies as follows:

At code 001111111111: $V_{ERROR\,1} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2\,V_{OS}$

At code 010000000000: $V_{ERROR\,2} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = \frac{4}{3}V_{OS}$

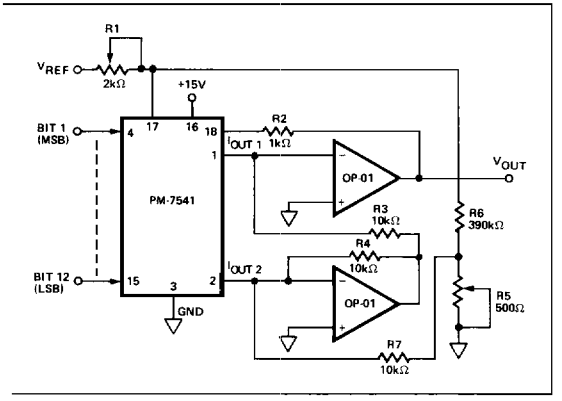
The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for V_{REF} = +10V) of 2.5mV for the PM-7541 DAC, it is clearly important that V_{OS} be nulled, either using the amplifier's nulling pins or an external network.

APPLICATIONS

Figures 5, 6, and 7 show simple unipolar and bipolar circuits with their associated waveforms using the PM-7541 and two PMI types of output amplifiers. A small feedback capacitor should be used across the amplifier to help prevent overshoot and ringing when using high-speed op amps. Resistor R1 is used to trim for full scale, low tempco (approximately 50ppm/°C) resistors or trimpots should be selected when gain adjustments are required.

FIGURE 7: Bipolar Operation (4-Quadrant)



UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuits of Figures 5 and 6 can either be used as a fixed reference D/A converter, or as an attenuator with an AC input voltage. In the fixed reference mode, the DAC provides an analog output voltage in the range of zero to plus or minus V_{REF}, depending on V_{REF} polarity. The reference input voltage can range between -20V to +20V; this is due to the ability of V_{REF} being able to exceed V_{DD}, the limiting factor being the op amp voltage range. Table 1 shows the code relationship for the circuit of Figure 6. R1 can be omitted with a resulting maximum gain error of 0.3% of full scale.

TABLE 1: Code Table for Circuit of Figure 6

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99975 V_{REF}
100000000000	-0.50000 V_{REF}
011111111111	-0.49975 V_{REF}
000000000000	0

BIPOLAR BINARY OPERATION (FOUR-QUADRANT)

The recommended circuit and code relationship is shown in Figure 7 and Table 2. The digital input is offset binary coded and multiplies V_{REF} per Table 2. Resistors R3 and R4 should be equal within 0.1% at all temperatures, but need not track the resistors within the PM-7541. The network comprised of R5, R6, and R7 sums 1/2 LSB of current into $I_{OUT\,2}$ to ensure correct coding at zero. R1 can be adjusted to produce the outputs shown in Table 2. However, when the application permits it, R1 and R2 should be omitted. The maximum gain error in this condition is 0.3% of full scale. R5 may be replaced by a 100Ω fixed resistor; the maximum zero error is then 0.015% of full scale. The input offset voltage of both amplifiers should be adjusted to less than 0.1mV and be better than 0.5mV over the temperature range of interest. With V_{REF} set to 10V, R5 is adjusted so that with code 100000000000, V_{OUT} = 0V ±0.2mV. R1 is adjusted so that code 000000000000 causes V_{OUT} to equal V_{REF}.

TABLE 2: Code Table for Circuit of Figure 7

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99951 V_{REF}
100000000001	-0.00049 V_{REF}
100000000000	0
010000000000	+0.50000 V_{REF}
000000000000	+1.00000 V_{REF}

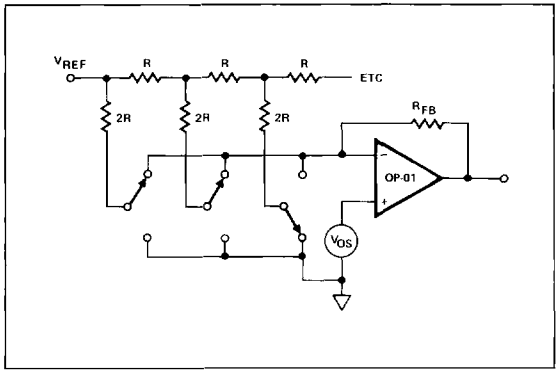
OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Set R5 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT2} amplifier offset trimpot for 0V ±0.1mV at I_{OUT2} amplifier output.
5. Connect a short circuit across R4.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset trimpot for 0V ±0.1mV at I_{OUT1} amplifier output.
8. Remove short circuit across R4.
9. Connect MSB (Bit-1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R5 for 0V ±0.2mV at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V_{DD}.
2. Monitor V_{OUT} for $-V_{REF}\left(1 - \frac{1}{2^{11}}\right)$ volts reading while adjusting R1.

FIGURE 8: Simplified Circuit



ANALOG/DIGITAL DIVISION

The transfer function for the PM-7541 connected in the multiplying mode as shown in Figure 6 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots\cdots\cdots \frac{A_{12}}{2^{12}}\right)$$

where A_x assume a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 9, it now is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots\cdots\cdots \frac{A_{12}}{2^{12}}}\right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

FIGURE 9: Analog/Digital Divider