



FEATURES

DATA

- Data Modes: ITU-T (formerly CCITT) V.34, V.32bis, V.32, V.22bis, V.22, V.21, Bell 212A, 103 and Bell 202 Rec. (CID)
- Data Rates: 115,200 to 300 bit/s
- "AT" Command Set
- Error Control: V.42 and MNP™ 2-4
- Data Compression: V.42bis and MNP 5
- T.I.E.S (Time Independent Escape Sequence)
- Caller ID

FAX

- Fax Modes: ITU-T V.17, V.29, V.27ter., V.21 (Channel 2)

GENERAL DESCRIPTION

The Sierra SQ3460 V.32bis, Plug and Play plus WaveFax® Modem Chip Set enables the modem designer to build a high performance, fully featured Fax, Data and Voice Mail modem with differentiation, minimum design effort and with ease of installation (Plug and Play (PnP)) for their customers.

The SQ3460 is a highly integrated modem chip set that will operate over General Switched Telephone Network (G.S.T.N.) two-wire full duplex lines. It supports all commonly used ITU-T (International Telecommunications Unit-Telecommunica-

- Class 1 and 2 Fax Interface
- 14,400 to 2400 bit/s

Voice/Business Audio

- Voice Mail Mode—16 bit linear— 4.8, 7.2, 8.0, 9.6 and 11k samples/s, 8 bit μ law— 4.8, 7.2, 8.0, 9.6, and 11K samples/s data rate
- Sierra 2.3x Voice Commands
- Integrated DMA Interface for high quality Voice Mail
- Windows.WAV file compatible— installs as sound board
- Software—Windows MCI Wave Driver, Windows MCI Voice Driver

PnP

- Plug and Play (PnP) ISA Revision 1.0a Compatible
- PnP Legacy systems ready
- PnP BIOS systems ready
- Windows 95™ ready

Power

- 5 Volt CMOS Technology
- Low power demand—less than 1.0W

Bus Interface

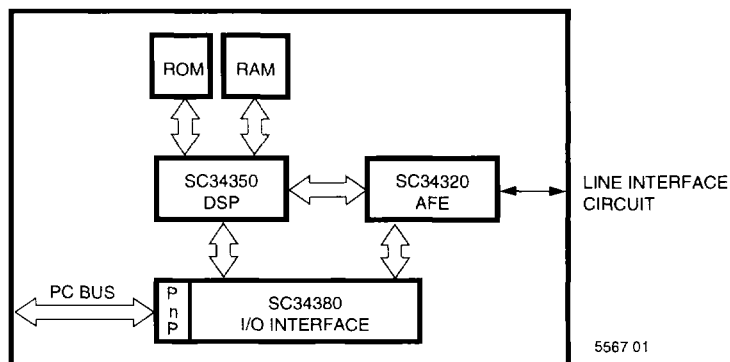
- Built in 16C550 Compatible UART Direct PC Bus Interface

tions (formerly CCITT)) and Bell data modes from 28,800 bits/s to 300 bit/s. It also supports the ITU-T V.42bis compression protocol that can deliver data at speeds up to 115,200 bit/s. V.17 Group III facsimile supports data at 14,400, 12,000, 9,600, 7,200, 4,800 and 2,400 bit/s.

The SQ3460 Chip Sets also support multiple voice-mail modes. Voice can be compressed down to 14.4 Kbps using Sierra's CVSD voice compression. Linear and Mu-Law voice modes are also supported. The linear voice mode allows .WAV files to be played through the mo-

dem without any compression/decompression required. Mu-Law mode will compress 16 bit samples into 8 bits, retaining 16 bit voice quality. Extensive support for multiple sampling rates is provided (4.8, 7.2, 8, 9.6, 11k samples/s). The lower sampling rates provide an alternative to compression for reducing disk space/channel bandwidth requirements. 8k s/s gives access to industry standard voice compression, text to speech, and speech recognition technology. 11k s/s is available for the commonly used Business Audio format .WAV files.

BLOCK DIAGRAM



SIERRA SEMICONDUCTOR
SIERS001

GENERAL DESCRIPTION (continued)

Sierra's WaveFax technology combines an integrated DMA interface, an 11k s/s sampling rate and a Wave driver to provide a Microsoft Windows 3.1 MCI Wave interface. WaveFax will install as a sound card under Microsoft Windows 3.1, providing compatibility with Microsoft system sounds, Microsoft

Sound Recorder, and other software utilizing the MCI wave interface. The DMA interface can also be used for voice mail allowing super-high quality greetings, and providing a technique by which .WAV music can be mixed into the background of outgoing messages.

The SQ3460 Chip Sets are supported with Sierra's extensive "AT" command set that now includes the Sierra 2.3x Voice commands.

The SQ3460CA consists of the SC34320CT (44 pin TQFP) Analog Front End, the SC34350CQ (132 pin PQFP) Digital Signal Processor, and the SC34380CQ (144 pin PQFP) I/O Interface.

GENERAL DESCRIPTION - SC34320CT

The SC34320 is a single chip Analog Front-End (AFE) designed for high speed voice-grade Modems up to 28,800 bit/s with echo canceling capability.

Associated with our SC34350CQ (DSP), it provides a powerful solu-

tion for our multi-mode Modem meeting ITU-T V.34, V.32bis, V.32, V.22bis, V.22, V.21 and BELL 103, 202, 212A data mode and V.21 (Chan. 2), V.27, V.29, V.17, fax modes.

The transmit section includes a 16-bit over-sampling D/A converter with a programmable interpolating filter. The receive section includes a 16-bit oversampling A/D converter with two programmable filters (one for decimation and the other for reconstruction).

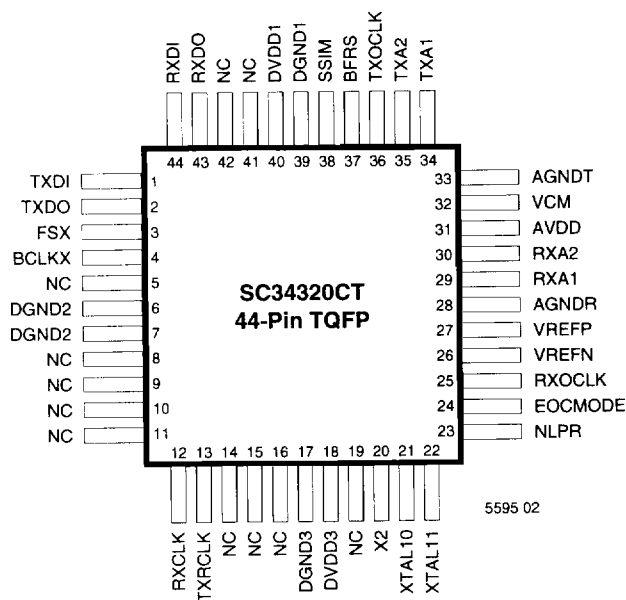
PIN DESCRIPTIONS - SC34320CT

PIN NAME	PIN NUMBER	DESCRIPTION
AGNDR	28	Analog Ground (0V).
AGNDT	33	Analog Ground (0V).
AV _{DD}	31	Positive Analog Power Supply (+5V±5%).
BCLKX	4	Transmit Bit Clock Output.
BFRS	37	Must be tied to +5V.
DGND1	39	Digital Ground (0V)
DGND2	6	Digital Ground (0V).
DGND3	17	Digital Ground (0V).
DV _{DD1}	40	Positive Digital Power Supply. (+5V±5%)
DV _{DD2}	7	Positive Digital Power Supply. (+5V±5%).
DV _{DD3}	18	Positive Digital Power Supply. (+5V±5%).
EOCMODE	24	Must be tied to +5V.
FSX	3	Transmit Frame Synchronization Output.
NC	5, 8, 9, 10, 11, 14, 15, 16, 19, 20, 41, 42	No Connection. These pins should be left unconnected.
NLPR	23	Low Power Reset Input.
R _X A1	29	Receive Positive Analog Input.
R _X A2	30	Receive Negative Analog Input.

PIN DESCRIPTIONS - SC34320CT (continued)

PIN NAME	PIN NUMBER	DESCRIPTION
R _X DI	44	Receive Serial Data Input.
R _X DO	43	Receive Serial Data Output.
R _X OCLK	25	Receive Oversampling Clock Input. Output high-impedance in normal mode.
R _X RCLK	12	Receive Baud Rate Clock Output.
SSIM	38	Serial Synchronous Interface Mode Input.
T _X A1	34	Smoothing filter positive Output.
T _X A2	35	Smoothing filter negative Output.
T _X DI	1	Transmit Serial Data Input.
T _X DO	2	Transmit Serial Data Output.
T _X OCLK	36	Transmit Oversampling Clock Input. Output high-impedance in normal mode.
T _X RCLK	13	Transmit Baud Rate Clock Output.
V _{CM}	32	Common Mode Voltage Input (2.5V±10%).
V _{REFN}	26	16 bit D/AC and A/DC Negative Reference Voltage.
V _{REFP}	27	16 bit D/AC and A/DC Positive Reference Voltage.
XTAL10	21	External Clock/Crystal Input 1.
XTAL11	22	External Clock/Crystal Input 2.

CONNECTION DIAGRAM - SC34320CT



SIGNAL DESCRIPTIONS - SC34350CQ DSP

The SC34350 high speed Digital Signal Processor (DSP) is designed for use with the SC34320 Analog Front End (AFE) and the SC34380 I/O interface. These 3 chips create Sierra's high speed V.34 (28,800 bit/s) data, fax, voice mail modem chip set.

The SC34350 performs all of the ITU-T/Bell modem modulation/demodulation and also performs the error control, data compression and "AT" command operation.

The signals for the SC34350CQ DSP are described below by each signal, its pin location, function, and operating modes, i.e., input (I), output (O), or high-impedance (Z). The signals are grouped according to their functional purpose.

Signal Descriptions - SC34350CQ

PIN NAME	PIN NUMBER	STATE	DESCRIPTION
ADDRESS AND DATA BUSES			
A15 (MSB)	77	I/O/Z	Parallel address bus A15 (MSB) through A0 (LSB). Multiplexed to address external data/program memory or I/O. Placed in high-impedance state in hold mode.
A14	76		
A13	75		
A12	74		
A11	73		
A10	72		
A9	64		
A8	63		
A7	62		
A6	61		
A5	60		
A4	59		
A3	58		
A2	57		
A1	56		
A0 (LSB)	55		
D15 (MSB)	6	I/O/Z	Parallel address bus D15 (MSB) through D0 (LSB). Multiplexed to transfer data between the core CPU and external data/program memory or I/O devices.
D14	7		
D13	8		
D12	9		
D11	10		
D10	11		
D9	12		
D8	13		
D7	23		
D6	24		
D5	25		
D4	26		
D3	27		
D2	28		
D1	29		
D0 (LSB)	30		

NOTE: All input pins that are unused should be connected to VDD or an external pull-up resistor.

Signal Descriptions - SC34350CQ (continued)

PIN NAME	PIN NUMBER	STATE	DESCRIPTION															
MEMORY CONTROL SIGNALS																		
\overline{DS} \overline{PS} \overline{IS}	89 91 90	O/Z	Data, Program, and I/O space select signals.															
READY	128	I	Data ready input. Indicates that an external device is prepared for the bus transaction to be completed.															
R/ \overline{W}	92	I/O/Z	Read/Write signal. Indicates transfer direction during communication to an external device. Normally in read mode (high), unless low level asserted for performing a write operation. Placed in high-impedance state in hold mode.															
\overline{STRB}	93	I/O/Z	Strobe signal. Always high unless asserted low to indicate an external bus cycle.															
\overline{RD}	82	O/Z	Read select indicates an active, external read cycle and may connect directly to the output enable (\overline{OE}) of external devices.															
\overline{WE}	83	O/Z	Write enable. The falling edge of this signal indicates that the device is driving the external data bus (D15-D0).															
MULTIPROCESSING SIGNALS																		
\overline{HOLD}	129	I	Hold Input. This signal is asserted to request control of the address, data, and control lines.															
\overline{HOLDA}	108	O/Z	Hold acknowledge signal. Indicates to the external circuitry that the processor is in a hold state.															
\overline{BR}	94	I/O/Z	Bus request signal. Asserted during access of external global data memory space.															
\overline{IAQ}	1	O/Z	Instruction acquisition signal. This signal is asserted (active low) when there is an instruction address on the address bus.															
\overline{BIO}	130	I	Branch control input. Samples as the BIO condition.															
XF	109	O/Z	External flag output (latched software-programmable signal).															
\overline{IACK}	112	O/Z	Interrupt acknowledge signal.															
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS																		
$\overline{INT4}$ $\overline{INT3}$ $\overline{INT2}$ $\overline{INT1}$	41 40 39 38	I	External user interrupt inputs.															
\overline{NMI}	42	I	Nonmaskable interrupt.															
\overline{RS}	127	I	Reset input.															
MP/ \overline{MC}	5	I	Mode select pin.															
OSCILLATOR/TIMER SIGNALS CLKIN 1/2																		
CLKOUT1	110	O/Z	Master clock output signal (or CLKIN2 frequency).															
CLKMD1 CLKMD2	71 103	I	<table border="0"> <tr> <td>CLKMD1</td> <td>CLKMD2</td> <td>Clock Mode</td> </tr> <tr> <td>0</td> <td>0</td> <td>External clock with divide-by-two option.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>External divide-by-one option.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Internal or external divide-by-two option.</td> </tr> </table>	CLKMD1	CLKMD2	Clock Mode	0	0	External clock with divide-by-two option.	0	1	Reserved	1	0	External divide-by-one option.	1	1	Internal or external divide-by-two option.
CLKMD1	CLKMD2	Clock Mode																
0	0	External clock with divide-by-two option.																
0	1	Reserved																
1	0	External divide-by-one option.																
1	1	Internal or external divide-by-two option.																
X2/CLKIN1	96	I	Input pin to internal oscillator from the crystal.															
X1	97	O	Output pin from the internal oscillator for the crystal.															
CLKIN2	95	I	Divide-by-1 input clock for driving the internal machine rate.															
TOUT	122	O	Timer output. This pin signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT1 cycle wide.															

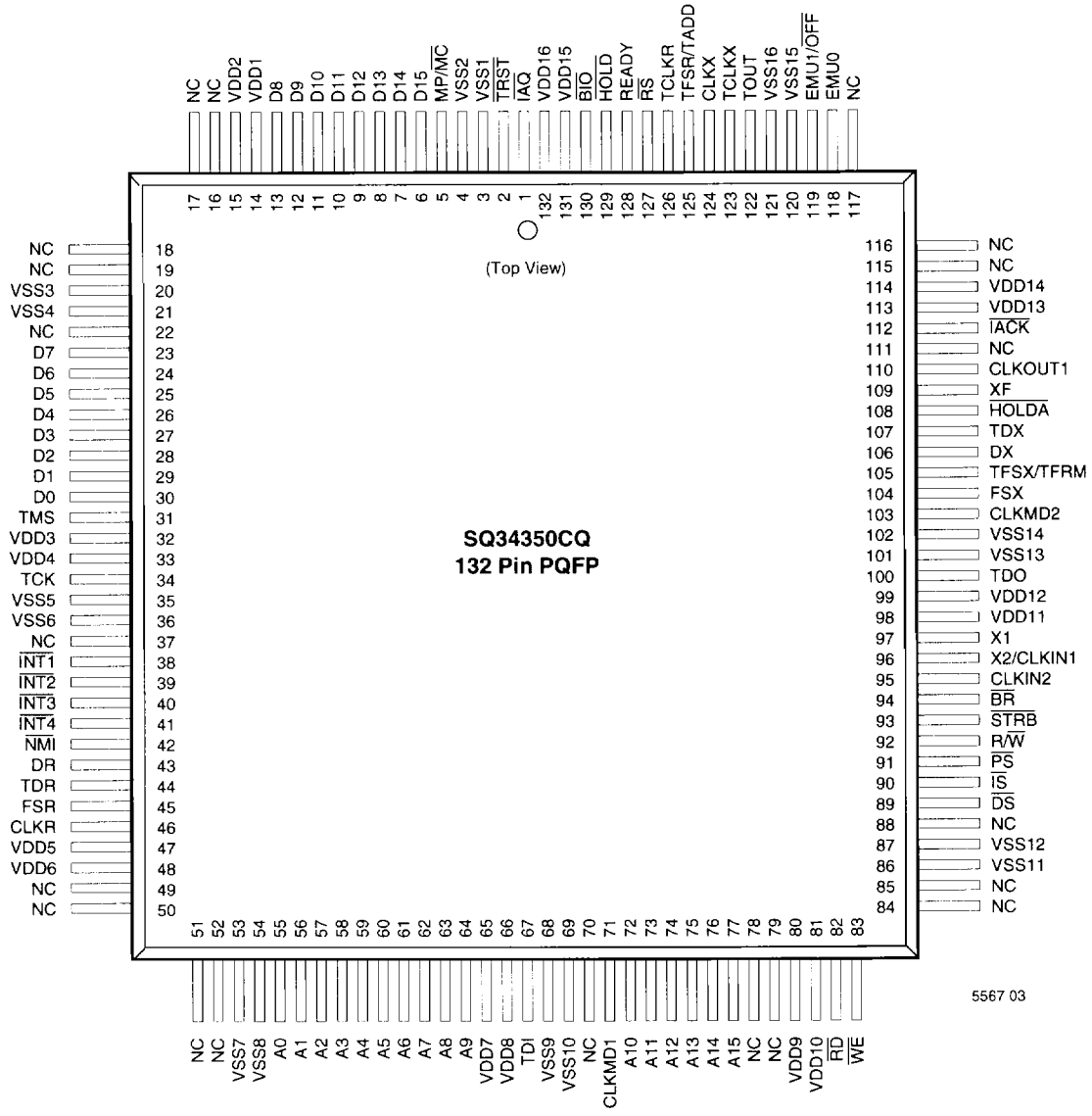
Signal Descriptions - SC34350CQ (continued)

PIN NAME	PIN NUMBER	STATE	DESCRIPTION
SERIAL PORT SIGNALS			
CLKR TCLKR	46 126	I I	Receive clock inputs.
CLKX TCLKX	124 123	I/O/Z I/O/Z	Transmit clock.
DR TDR	43 44	I I	Serial data receive inputs. Serial data is received in the RSR (serial port receive shift register) via the DR/TDR pin.
DX TDX	106 107	O/Z	Serial data transmit outputs. Serial data transmitted from the XSR (serial port transmit shift register) via the DX/TDX pin.
FSR TFSR/TADD	45 125	I I/O/Z	Frame synchronization pulse for receive input.
FSX TFSX/TFRM	104 105	I/O/Z I/O/Z	Frame synchronization pulse for transmit input/output.
TEST SIGNALS			
TCK	34	I	JTAG test clock.
TDI	67	I	JTAG test data input.
TDO	100	O/Z	JTAG test data output.
TMS	31	I	JTAG test mode select.
$\overline{\text{TRST}}$	2	I	JTAG test reset.
EMU0	118	I/O/Z	Emulator pin 0.
EMU1/ $\overline{\text{OFF}}$	119	I/O/Z	Emulator pin 1/disable all outputs. EMU1/ $\overline{\text{OFF}}$ =low
RESERVED	16 17 18 19 22 37 49 50 51 52 70 78 79 84 85 88 111 115 116 117	N/C	Reserved pin. These pins should be left unconnected.
SUPPLY PINS			
V _{DD1,2,3,4}	14, 15, 32, 33		Power supply for data bus.
V _{DD5,6,9,10}	47, 48, 80, 81		Power supply for address bus.
V _{DD8,13,14}	65, 66, 113, 114		Power supply for inputs and internal logic.
V _{DD11,12,15,16}	98, 99, 131, 132		Power supply for memory control signals.
V _{SS1,2,11,12}	3, 4, 86, 87		Ground for memory control signals.

Signal Descriptions – SC34350CQ (continued)

PIN NAME	PIN NUMBER	STATE	DESCRIPTION
V _{SS3,4,5,6}	20, 21, 35, 36		Ground for data bus.
V _{SS13,14,15,16}	101, 102, 120, 121		Ground for inputs and internal logic.

**PINOUTS FOR SQ34350
132 PIN PQFP**



NOTE: NC = No connect. (These pins are reserved.)

SC34380CQ I/O INTERFACE

The SC34380 is not only the interface between the DSP (SC34350) and the AFE (SC34320). It also provides the system timing required

for Sierra's V.34 solution. Some of the other functions include: Plug and Play (PnP) operation, 16C550 compatible UART interface to the

ISA bus, or a USART interface for a serial (EIA-232) interface.

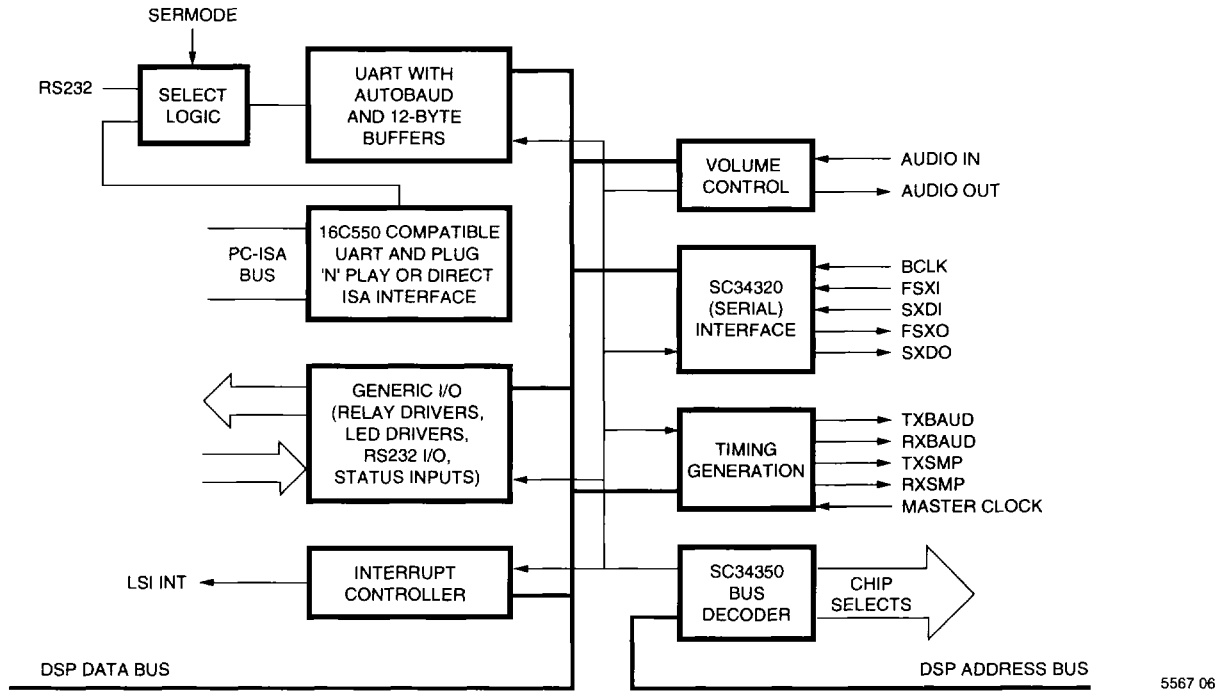


Figure 1. SC34380CQ Block Diagram

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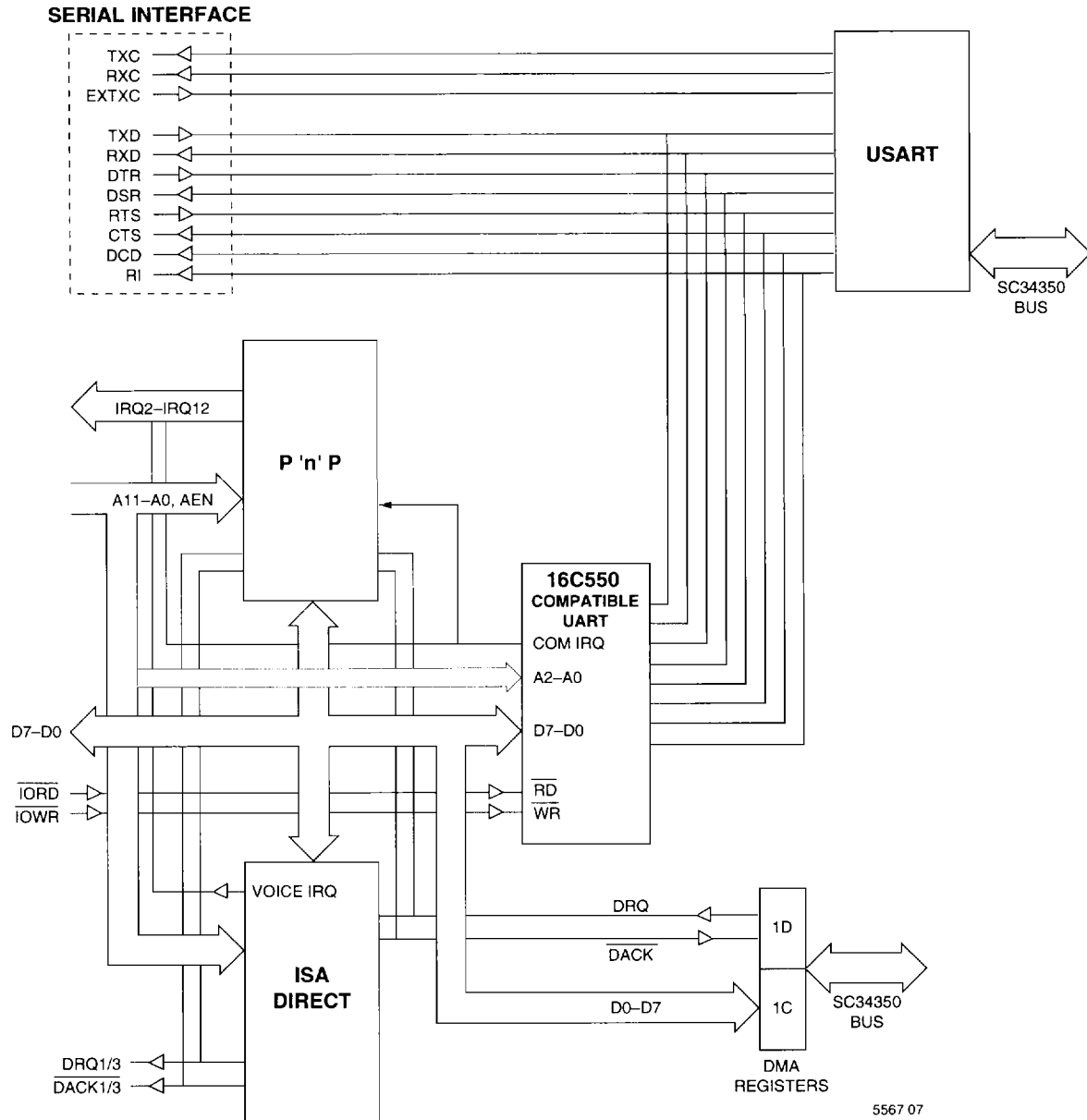


Figure 2. Serial/Parallel Interface Overview

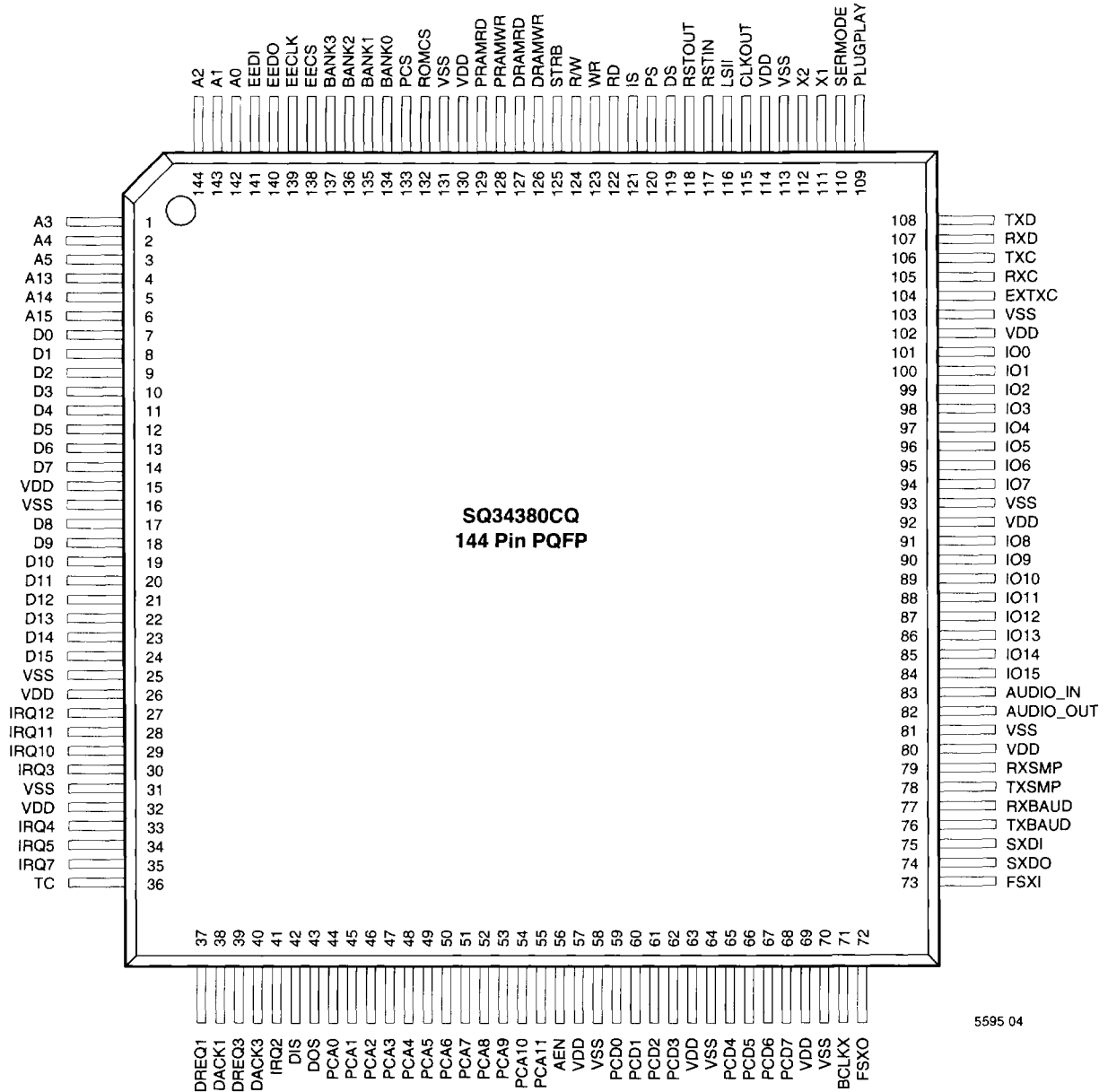
Signal Descriptions - SC34380CQ

PIN NAME	PIN NUMBER	STATE	ATTRIBUTES	DESCRIPTION
A0-A5	142-144, 1-3	IN		SC34350 Addresses 0-5
A13-A15	4-6	IN		SC34350 Addresses 13-15
AEN	56	IN	TTL/Pull-up	PC Address Enable
AUDIOIN	83	IN	ANALOG	Input from DAA for audio
AUDIOOUT	82	OUT	ANALOG	Output from volume control to audio amp.
BANK0-BANK3	134-137	OUT	4mA	Bank 0-3 Outputs for option B ROM
BCLKX	71	IN		Shift Clock from AFE.
CLKOUT	115	OUT	4mA	Buffered XTAL OUT
D0-D15	7-24	I/O	4mA	SC34350 Data Bus 0-15
DACK1	38	IN	TTL/Schmitt/Pull-up	PC DMA Acknowledge 1
DACK3	40	IN	TTL/Schmitt/Pull-up	PC DMA Acknowledge 3
DIS	42	IN	TTL/Schmitt/Pull-up	PC Data In (read) Strobe
DOS	43	IN	TTL/Schmitt/Pull-up	PC Data Out (write) Strobe
DRAMRD	127	OUT	8mA	Data RAM Read
DRAMWR	126	OUT	8mA	Data RAM Write
DRQ1	37	OUT	12mA/Tristate	PC DMA Request 1
DRQ3	39	OUT	12mA/Tristate	PC DMA Request 3
DS	119	IN		SC34350 Data Strobe
EECLK	139	OUT	4mA	PnP EERAM Shift Clock
EESCS	138	OUT	4mA	PnP EERAM Chip Select
EEDI	141	IN	Pull-Up	Serial Data from PnP EERAM
EEDO	140	OUT	4mA	Serial Data to PnP EERAM
EXTXC	104	IN	TTUPull-Up	RS232 External Transmit Clock
FSXI	73	IN		Serial Frame Sync from the SC34320
FSXO	72	OUT	2mA	Serial Frame Sync to the SC34320
IO0-IO15	101-84	I/O	12mA/Pull-Up	General Purpose I/O 0-15
IRQ2/COM IRQ	41	OUT	12mA Tristate	PC IRQ2 or Com Port IRQ
IRQ3/NOICE IRQ	30	OUT	12mA Tristate	PC IRQ3 or Voice DMA IRQ
IRQ4/HS*	33	OUT	12mA Tristate	PC IRQ4 or High Speed LED
IRQ5/AA*	34	OUT	12mA Tristate	PC IRQ5 or Auto Answer LED
IRQ7/RINGOUT*	35	OUT	12mA Tristate	PC IRQ7 or RS232-RI
IRQ10/DCD*	29	OUT	12mA Tristate	PC IRQ10 or RS232-DCD
IRQ11/CTS*	28	OUT	12mA Tristate	PC IRQ11 or RS232-CTS
IRQ12/DSR*	27	OUT	12mA Tristate	PC IRQ12 or RS232-DSR
IS	121	IN		SC34350 I/O Strobe
LSII	116	OUT	4mA	Interrupt From SC34380CQ
PCA0/DTR*	44	IN	TTL/Pull-Up	PC Address 0 or RS232-DTR
PCA1/RTS*	45	IN	TTL/Pull-Up	PC Address 1 or RS232-DTR
PCA2	46	IN	TTL/Pull-Up	PC Address 2

Signal Descriptions - SC34380CQ (continued)

PIN NAME	PIN NUMBER	STATE	ATTRIBUTES	DESCRIPTION
PCA3-PCA9	47-53	IN	TTL/Pull-Up	PC Address 3-9
PCA10/COMS0	54	IN	TTL/Pull-Up	PC Address 10 or Com Port Select 0
PCA11/COMS1	55	IN	TTL/Pull-Up	PC Address 11 or Com Port Select 1
PCD0-PCD7	59-62, 65-68	I/O	24mA lo/3mA hi **	PC Data Bus 0-7
\overline{PCS}	133	OUT	4mA	Decoded Address Output -Future
PLUGPLAY	109	IN	Pull-Up	PnP or ISA Direct Interface Select
\overline{PRAMRD}	129	OUT	8mA	Program RAM Read
\overline{PRAMWR}	128	OUT	8mA	Program RAM Write
\overline{PS}	120	IN		SC34350 Program Strobe
R/W	124	IN		SC34350 Read/Not Write Signal
\overline{RD}	122	IN		SC34350 Read
\overline{ROMCS}	132	OUT	4mA	ROM or FLASH Select
RSTIN	117		TTL/Schmitt	Reset InDut
\overline{RSTOUT}	118	OUT	4mA	Low Going Reset Out
RXBAUD	77	OUT	2mA	Rx Svnthesizer Clock To DSP
RXC	105	OUT	4mA	R232 Receive Clock
RXD	107	OUT	4mA	RS232 Receive Data
RXSMP	79	OUT	2mA	SC34320 Rx Sample Clock
SERMODE	110	IN	Pull-Up	Serial/Parallel mode select
\overline{STRB}	125	IN		SC34350 External Access Strobe
SXDI	75	IN		Serial Data to SC34320
SXDO	74	OUT	4mA	Serial Data from SC34320
TC	36	IN	TTL/Schmitt/Pull-up	PC Terminal Count
TTUPull-UD	51	IN		PCA7
TXBAUD	76	OUT	2mA	Tx Svnthesizer Clock To DSP
TXC	106	OUT	4mA	RS232 Transmit Clock
TXD	108	IN	TTL/Pull-Up	RS232 Transmit Data
TXSMP	78	OUT	2mA	SC34320 Tx Sample Clock
\overline{WR}	123	IN		SC34350 Write
X1	111	XTAL IN		Master Crystal in
X2	112	XTAL OUT		Master Crystal out
VDD	15, 26, 32, 57, 63, 69, 80, 92, 102, 114, 130	POWER		+5V has 11 Pins
VSS	16, 25, 31, 58, 64, 64, 70, 81, 93, 103, 113, 131	POWER		GND has 12 Pins

**PINOUTS FOR SQ34380
144 PIN PQFP**



**SQ34380CQ
144 Pin PQFP**

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Modem Voice DMA Logic

The SC34380 logic implements voice DMA and interrupt capabilities. The UART scratch register can be used for data and register 198h is used for status as defined by Table 3.

Register 198 Definition

Bit 0: The DMA request bit, initiates the DMA. Writing a "1" to this bit initiates the DMA. Reading this bit allows the user to see if a DMA is in progress. This bit is cleared by a valid acknowledge.

Bit 1: PnP

- "1": Plug and Play.

Bit 2: The DMA channel select bit, selects which channel is active:

- "0": Use DMA channel 1
- "1": Use DMA Channel 3.

Bit 3: The DMA request enable bit, enables the DMA request (bit 0) onto the DMA channel, which has been selected by bit 2.:

- "0": Tristate all DMA request pins
- "1": Enable DMA request pin select by bit2.

Bit 4: The Voice IRQ enable bit, enables the voice IRQ pin. This bit is analogous to the OUT2 enable bit (MCR.3) for the COMPORT IRQ pin:

- "0": Disable Voice IRQ
- "1": Enable Voice IRQ

Bit 5: The status of the LOOP pin is read into this bit.

Bit 6: The status of the LRD pin is read into this bit.

Bit 7: This bit selects the register that controls the register which controls the voice DMA logic:

- "0": Use the registers residing at 280h-2FFh.
- "1": Use register 198h.

On power up this bit is reset, therefore the default is that the DMA logic will use registers 280h-2FFh.

DMA Request (internal signal)

DMA requests are generated by the controller writing a 1 to bit0 of register 198h. Requests are cleared by resets of the chip or by a valid DMA acknowledge. The current state of the DMA request is returned on bit 0 during reads of 198h. When bit 1 (PNP) is 1, Plug and Play controls which ISA DMA channel is in use. When this bit is 0, the controller controls the DMA channel using bit 2.

DMA Acknowledge (internal signal)

A valid acknowledge is generated by a valid ISA $\overline{\text{DACK}}$ signal from the DMA channel. This valid acknowledge clears bit0 of register 198h, forces CS low and A2-A0 high (scratch register address) of the 16C550 UART.

Voice Interrupt (internal signal)

If at any time during a valid DMA acknowledge the ISA terminal count (TC) goes high (valid), the voice interrupt will be strobed low for the duration of TC being valid (that is the voice interrupt is $\overline{\text{DACK.AND. TC}}$). Note that since this interrupt is normally high and strobed low, a single low to high interrupt transition will be generated on the ISA bus when the interrupt is first enabled.

FIRMWARE COMPATIBILITY

In order to maintain compatibility with the existing firmware, another option different from above, had to be provided for the modem voice DMA interface. With this option, the peripheral address space, 200h-2FFh, is split into two address spaces:

- The DSP address space, 200h-27Fh, is external and DSPCS is the chip select for this address space. DSPCS pin replaces the MCS pin.
- The Voice DMA address space, 27Fh-2FFh, becomes internal locations for the Voice DMA registers, These registers existed before in the PLDs.

LOCATION	NAME	7	6	5	4	3	2	1	0
198h	DMA	R198_SEL	LRD	LOOP	VOICE _ENA	DREQ _ENA	CH_SEL	PNP Status	REQ
		W/R, 0	R	R	W/R, 0	W/R, 0	W/R, 0	R, Pin	W/R, 0

- W: Writeable register
- R: Readable register
- 0: Initialized to 0, on power up.

Table 3. SC34380 Register 198 Definition

Following are the registers associated with the Voice DMA and their bits definition:

LOCATION	NAME	7	6	5	4	3	2	1	0
28Xh	DMA_SEL	0	0	0	0	0	0	0	DMA_SEL
		NU	NU	NU	NU	NU	NU	NU	W/R, 0

NOTE: DMA_SEL: "0": No Voice DMA.
"1": Voice DMA.

LOCATION	NAME	7	6	5	4	3	2	1	0
29Xh	DMA_Channel	0	0	0	0	0	0	0	DMA1_3
		NU	NU	NU	NU	NU	NU	NU	W/R, 0

NOTE: DMA1_3: "1": Channel 1.
"0": Channel 3.

LOCATION	NAME	7	6	5	4	3	2	1	0
2AXh	DMA_REQ	0	0	0	0	0	0	0	DMA_REQ
		NU	NU	NU	NU	NU	NU	NU	W/R, 0

NOTE: DMA_REQ: This bit initiates the DMA. Writing a "1" to this bit initiates the DMA. Reading this bit allows the user to see if a DMA is in progress. This bit is cleared by a valid acknowledge.

LOCATION	NAME	7	6	5	4	3	2	1	0
2CXh	LRD	0	0	0	0	0	0	LRD	0
		NU	NU	NU	NU	NU	NU	R	NU

NOTE: LRD: the status of the LRD pin is read into this bit.

LOCATION	NAME	7	6	5	4	3	2	1	0
2DXh	LOOP	0	0	0	0	0	0	LOOP	0
		NU	NU	NU	NU	NU	NU	R	NU

NOTE: LOOP: the status of the loop pin is read into this bit.

PLUG AND PLAY AUTO-CONFIGURATION

The Plug and Play auto-configuration logic is provided in order to eliminate the need of hardware jumpers and ease installation of a Sierra AccuSound data fax modem card in an ISA bus-based host system. This logic configures all necessary I/O base address ports, port decoding ranges, interrupt request (IRQ) lines and direct memory access (DMA) channels. All data required for Plug and Play is stored in an external E²PROM; data values shown in this section as FFH are when no E²PROM is present. When the last byte in the E²PROM reads 55H, these values are read from E²PROM.

The major steps of the auto-configuration process are as follows:

- Put Plug and Play ISA card in configuration mode
- Isolate Plug and Play ISA card
- Assign a handle and read the card's resource data structure
- After the resource requirements and capabilities are determined for the card, use the handle to assign conflict free resources to each card in the host system
- Activate Plug and Play ISA card and remove it from configuration mode

The Plug and Play software identifies and configures devices using a set of commands defined in this specification. The commands are executed using three, 8-bit I/O ports. 16-bit accesses (assertion of IOCS16#) to the configuration ports are not supported. A sequence of data writes to one of the ports is used as the key to enable the Plug and Play logic on all cards in the system. This sequence, referred to as the initiation key, is described in the functional description section.

All Plug and Play cards respond to the same I/O port addresses, so the Plug and Play software needs

an isolation mechanism to address one particular card at a time. The isolation protocol uses a unique number on each card to isolate one Plug and Play card at a time. After isolation, the Plug and Play software assigns each card a handle, which is used to select that unique Plug and Play card.

The card must support a readable resource data structure that describes the resources supported and those requested by the functions on the card. Each function is defined as a logical device. Plug and Play resource information is provided for each logical device and each logical device is independently configured through the Plug and Play standard registers.

Following isolation, the Plug and Play software reads the resource data structure on the card. When all resource capabilities and demands are known, a process of resource arbitration is invoked to determine resource allocation to each ISA card in the host system. The configuration of ISA cards is done using the command registers specified for each resource type. The command set also supports the ability to activate or deactivate the function(s) on the card.

After configuration is complete, the Plug and Play card is removed from configuration mode. To re-enable configuration mode, the initiation key needs to be re-issued. This prevents accidental erasure of the configuration information.

For a detailed specification regarding Plug and Play devices, please refer to the "Plug and Play ISA

Specification" (version 1.0a), published by Intel Corporation and Microsoft Corporation.

Auto-configuration Ports

The configuration space is implemented as a set of 8-bit registers. These registers are used by the Plug and Play software to issue commands, check status, access the resource data information, and configure the Plug and Play hardware for the host computer. Three 8-bit ports are used by the software to access the configuration space on each Plug and Play ISA card. The ports are listed in Table 3.

The ADDRESS and WRITE_DATA ports are located at fixed addresses. The WRITE_DATA port is located at an address alias of the ADDRESS port. All three auto-configuration ports use a 12-bit ISA address decode. The READ_DATA port is relocatable within the I/O range from 0203H to 03FFH. This is the only readable auto-configuration port.

ADDRESS Port

The Plug and Play registers are accessed by the host by first writing the address of the desired register to the ADDRESS port, followed by a read of data from the READ_DATA port or a write of data to the WRITE_DATA port. A write to the ADDRESS port may be followed by any number of WRITE_DATA or READ_DATA accesses to the same register location without the need to write to the ADDRESS port before each access. The ADDRESS port is also the write destination of the initiation key, which is described later.

PORT NAME	LOCATION	TYPE
ADDRESS	0279H (Printer status port)	Write-only
WRITE_DATA	0A79H (Printer status port + 0800H)	Write-only
READ_DATA	Relocatable in range 0203H to 03FFH	Read-only

Table 4.

WRITE_DATA Port

The WRITE_DATA port is used by the host to write information to the Plug and Play registers. The destination of the data is determined by the last setting of the ADDRESS port.

READ_DATA Port

The READ_DATA port is used by the host to read information from the Plug and Play registers. The source of the data is determined by the last setting of the ADDRESS port. The address of the READ_DATA port is set by writing the proper value to a Plug and Play control register. The isolation protocol verifies that the location selected for the READ_DATA port is free of conflict.

Initiation Key

The initiation key places the Plug and Play logic into configuration mode. This is done by a predefined series of writes to the ADDRESS port. If the proper series of I/O writes is detected, then the Plug and Play auto-configuration ports are enabled.

The hardware check of the initiation key is implemented as a *linear feedback shift register* (LFSR). Software generates the LFSR sequence and writes it to the ADDRESS port as a sequence of 8-bit write cycles. The hardware compares the byte of write data with the value in the shift register at each write. Any time the data does not match, the hardware will reset to the initial value of the LFSR.

Isolation Protocol

A simple algorithm is used to isolate the Plug and Play card. This algorithm uses the signals on the ISA bus and requires lock-step operation between the Plug and Play hardware and the isolation software.

The key element of this mechanism is that the card contains a unique

number, referred to as the *serial identifier* for the rest of the discussion. The serial identifier is a 72-bit unique, non-zero, number composed of two, 32-bit fields and an 8-bit checksum. The first 32-bit field is a vendor identifier. The other 32 bits can be any value, for example, a serial number, part of a LAN address, or a static number, as long as there will never be two cards in a single system with the same 64 bit number. The serial identifier is accessed bit-serially by the isolation logic and is used to differentiate the cards.

Hardware Protocol

The isolation protocol can be invoked by the Plug and Play software at any time. The initiation key, described earlier, puts the card into configuration mode. The hardware on the card expects 72 pairs of I/O read accesses to the READ_DATA port. The card's response to these reads depends on the value of each bit of the serial identifier which is being examined one bit at a time.

If the current bit of the serial identifier is a "1", then the card will drive the data bus to 55H to complete the first I/O read cycle. If the bit is "0", then the card puts its data bus driver into high impedance. The card in high impedance will check the data bus during the I/O read cycle to sense if another card is driving D[1:0] to "01." During the second I/O read, the card(s) that drove the 55H, will now drive a AAH. All high impedance cards in the host system will check the data bus to sense if another card is driving D[1:0] to "10."

If a high impedance card sensed another card driving the data bus with the appropriate data during both cycles, then that card ceases to participate in the current iteration of card isolation. Such cards, which lose out, will participate in future iterations of the isolation protocol.

NOTE: During each read cycle, the Plug and Play hardware drives the entire 8-bit data bus, but only checks the lower 2 bits.

If a card was driving the bus or if the card was in high impedance and did not sense another card driving the bus, then it should prepare for the next pair of I/O reads. The card shifts the serial identifier by one bit and uses the shifted bit to decide its response.

The above sequence is repeated for the entire 72-bit serial identifier. At the end of this process, one card remains. This card is assigned a handle referred to as the *Card Select Number* (CSN) that will be used later to select the card. Cards which have been assigned a CSN will not participate in subsequent iterations of the isolation protocol. The card must be assigned a CSN before it will respond to the other commands defined in the specification.

It should be noted that the protocol permits the 8-bit checksum to be stored in non-volatile memory on the card or generated by the on-card logic in real-time. The same LFSR algorithm described in the initiation key section is used in the checksum generation.

The Plug and Play card must not drive the IOCHRDY signal during serial isolation. However, the card may drive IOCHRDY at any other time.

Plug and Play Resources

This specification will only detail the Plug and Play resources specific to the Sierra voice, data, fax product. For other information regarding Plug and Play resources and programming Plug and Play devices, please consult the "Plug and Play ISA Specification" (version 1.0a), published by Intel Corporation and Microsoft Corporation.

Plug and Play cards return read-only configuration information in two formats. The serial identifier is returned bit-wise by the Plug and Play devices in response to reads

FIELD NAME	LENGTH	DEFINITION
Vendor ID Byte 0	8 bits	Bit[7] 0 Bits[6:2] First character in compressed ASCII Bits[1:0] Second character in compressed ASCII bits[4:3]
Vendor ID Byte 1	8 bits	Bits[7:5] Second character in compressed ASCII bits[2:0] Bits[4:0] Third character in compressed ASCII
Vendor ID Byte 2	8 bits	Product Number (Vendor Assigned)
Vendor ID Byte 3	8 bits	Product Number (Vendor Assigned)
Serial Number Byte 0	8 bits	Serial Number Bits[7:0]
Serial Number Byte 1	8 bits	Serial Number Bits[15:8]
Serial Number Byte 2	8 bits	Serial Number Bits[23:16]
Serial Number Byte 3	8 bits	Serial Number Bits [31:24]
Checksum	8 bits	Checksum of ID and serial number verifies that the information has been correctly read from a Plug and Play ISA card.

Table 5. Serial Identifier

from the Serial Isolation register. Plug and Play cards also provide resource data sequentially a byte at a time in response to reads from the Resource Data register. The resource configuration data completely describes all resource needs and options of the device.

Vendor ID

The 32-bit vendor identifier is an EISA ID. This ID consists of:

- bits[15:0]—three character compressed ASCII EISA ID. Compressed ASCII is defined as 5 bits per character, "00001" = "A" ... "11010" = "Z".
- bits[31:16] – manufacturer specific device code. The SC34380 device code is vendor definable.

Serial/Unique Number

The 32-bit serial number is used in the isolation process for selection of individual Plug and Play ISA cards. If FFFFFFFFH is returned, no serial number has been pre-programmed.

Checksum

The checksum field is used to ensure that no conflicts have occurred while reading the device

identifier information. The checksum generation is described in Appendix B of the "Plug and Play ISA Specification."

Plug and Play Resource Data Types

Plug and Play resource data fully describes all resource requirements of a Plug and Play ISA card as well as resource programmability and interdependencies. Plug and Play resource data can be described as a series of "tagged" data structures.

The SC34380 reserves the last byte of the stored resource information in the E²PROM. Byte 511 is set to 55H.

Plug and Play Standard Registers

This specification will only detail the Plug and Play registers specific to the SC34380 product. For other information regarding Plug and Play registers and programming Plug and Play devices, please consult the "Plug and Play ISA Specification" (version 1.0a), published by Intel Corporation and Microsoft Corporation.

Figure 3 illustrates the order of the card registers and the logical de-

vice registers. As this figures shows, the card registers are unique for each card. However, the logical devices registers are repeated for each logical device on the card. The SC34380 supports 2 logical devices: FAX/Modem and Modem Voice Channel.

NOTE: Any unimplemented registers in the range 00H to 2FH must return 0 on reads.

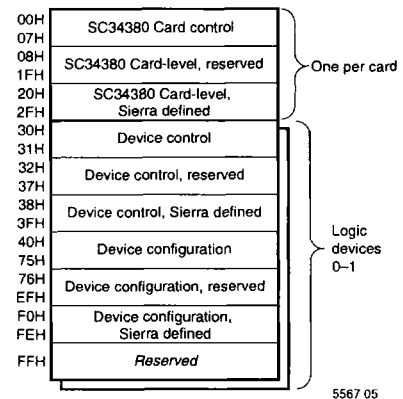


Figure 3. Plug and Play Register Map

Plug and Play Card Control Registers (00H to 2FH)

NAME	REGISTER INDEX	DEFINITION
Set RD_DATA Port	00H	Writing to this location modifies the address of the port used for reading from the Plug and Play ISA cards. Bits[7:0] become I/O read port address bits[9:2]. Reads from this register are ignored.
Serial Isolation	01H	If the card is in the <i>Isolation</i> state, a read to this register causes the card to compare one bit of the boards ID. This register is read only.
Config Control	02H	Bit[2] - Reset CSN to 0. A write to bit[2] of this register causes all cards to reset their CSN to zero. Bit[1] - Return to the <i>Wait for Key</i> state. A write to bit[1] of this register causes the card to enter the <i>Wait for Key</i> state, but all CSNs are preserved and logical devices are not affected. Bit[0] - Reset all logical devices and restore configuration registers to their power-up values. A write to bit[0] of this register performs a reset function on all logical devices. This resets the contents of configuration registers to their default state. The card's logical devices enter their default state and the CSN is preserved. This register is write-only. The values are not sticky, that is, hardware will automatically clear them and there is no need for software to clear the bits.
Wake[CSN]	03H	If the card has a CSN that matches the write data[7:0], a write to this port will cause the card to go from the <i>Sleep</i> state to either the <i>Isolation</i> state if the write data for this command is zero or the <i>Config</i> state if the write data is not zero. Additionally, the pointer to the byte-serial device is reset. This register is write-only.
Resource Data	04H	A read from this address reads the next byte of resource information. The Status register must be polled until bit[0] is set before this register may be read. This register is read only.
Status	05H	Bit[0] when set indicates it is okay to read the next data byte from the Resource Data register. This register is read-only.
Card Select Number	06H	A write to this port sets the card's CSN. The CSN is a value uniquely assigned to each ISA card after the serial identification process so that each card may be individually selected during a Wake[CSN] command. This register is read/write.
Logical Device Number	07H	Selects the current logical device (0 or 1). All reads and writes of I/O, interrupt and DMA configuration information access the registers of the logical device written here. In addition, the I/O Range Check and Activate commands operate only on the selected logical device. This register is read/write.
Card Level Reserved	08H - 1FH	<i>Reserved for future use (return 0)</i>
Card Level Vendor Defined	20H - 2FH	<i>Vendor defined (not used, return 0)</i>

SYSTEM INTERFACES

Clock

The Sierra V.34 solution needs only a single 28.571 MHz crystal. The SC34380 provides all of the system clocks required, including a buffered clock for the DSP.

The specification for the 28.571 MHz crystal is shown in Table 5.

Approved parts:

CCL-6-28.571C153

DSP Memory

The DSP requirements are:

4 X 32K X 8 SRAM with 15 nS access time are required.

2 X 128K X 8 Flash are used in the FastTrack demo board and accomodates all the features that are available at this time. The access time of this memory must be 45 nS max.

DAA

The Data Access Arrangement (DAA) connects the SC34320 AFE to the RJ11 phone jacks and thus to the telephone line. The primary function of the DAA is to isolate the modem from the telephone line so the modem will not harm the GSTN. This isolation is mandated by the FCC, Telephone Operating Companies (PTT) and UL.

The recommended transformer for high speed modem DAA's, used in the *FastTrack™* Kits, is one that has no DC current/loop current (dry transformer) flowing in the primary winding. A dry transformer, with the same equivalent size as a wet transformer, can be designed with better amplitude, frequency and phase characteristics.

Relays are used for on/off hook, voice mode and Caller ID functions. A MOV provides protection from telephone line transients. Inductor-capacitor networks prevent frequencies generated by the modem from being transmitted into the telephone line (limits are specified in Code of Federal Regulations TITLE 47 PART 15B).

Host Bus Interface

The interface to the host PC consists of a COM PORT (COM1 to COM4) interface and a Direct Memory Access (DMA) interface. The 16C550 compatible UART in the SC34380 is connected to the PC COM PORT using a generate a DMA request signal, for data transfer, and force the selection of the scratchpad register (STR) in the 16C550. The PC then issues a DMA acknowledgment that allows STR to be used for DMA.

Serial EEPROM

The SC34380 will address a 4K X 1 serial EEPROM that is required for non-volatile storage of telephone numbers and modem settings.

T.I.E.S.

Time Independent Escape Sequence (T.I.E.S.) is an in-band escape sequence that allows the modem to escape from the data mode to the command mode. The escape command is identical to that used by Hayes. The escape character is normally a + (default setting), however, it can be changed using S-Register S2. T.I.E.S. provides the same results and reliability as the Hayes patented time dependent escape sequence, but without requiring a license or royalty. T.I.E.S. is the default setting in Sierra controller firmware. It can be changed, however, to the time dependent escape sequence for those who prefer and have a license to the Hayes patented technology.

SCHEMATICS

Schematics are available upon request for a Voice, Data, Fax V.34 implementation using the SQ3460CA chip set.

Hayes is a trademark of Hayes Microcomputer Systems

Operating Temperature Range	0°C to +70°C
Frequency Temperature Stability	± 0.005% from 0°C to +70°C
Specifications at 25°C ± 2°C	
Frequency	28.571 MHz
Frequency Calibration Tolerance	0.005% (50 ppm)
Parallel load Capacitance	18 pF
Effective Series Resistance	40Ω max.
Drive Level—correlation/operating	0.5 mW
Shunt Capacitance	7 pF max.
Oscillation Mode	3rd overtone
Test Circuit	Saunders 150C
Mechanical Holder Type	HC18/U or HC-49/U
Mechanical Dimensions	
Height	13.46 mm max.
Width	11.80 mm max.
Depth	4.64 mm max.
Lead Length	12.70 mm min.
Lead Spacing	4.88 mm
Lead Diameter	0.43 mm

Table 5. Specifications for 28.571 MHz Crystal

TYPICAL POWER CONSUMPTION

	OPERATING
SQ3460CA	750 mW

ELECTRICAL SPECIFICATIONS - SC34320 Analog Front End (AFE)**Absolute Maximum Ratings (Notes 1 and 2)**

V_{DD} Supply Voltage	6V
Input Signals with Respect to Ground	$V_{SS} - 0.6V$ to $V_{DD} + 0.6V$
Operating Temperature Range	0 to +70°C
Storage Temperature Range	-65 to 150°C
Lead Temperature (Soldering 10 sec)	300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Power dissipation temperature derating — Plastic Package: -12 mW/C from 65°C to 85°C.

DC Electrical Characteristics ($T_A = 0$ to 70°C, $V_{DD} = +5V \pm 5\%$, $V_{SS} = RXGND = GND$)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Quiescent Current			40	52	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.2			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V
V_{OH}	High Level Output ($I_{OH} = 0.5$ mA)		2.4			V
V_{OL}	Low Level Output ($I_{OL} = 1.6$ mA)				0.4	V

Analog Characteristics

NAME	TYPE	CHARACTERISTIC	VALUE
RXA1/A2	I	Input Impedance Voltage Range Total Distortion	>100K Ω 2.5 \pm 1.5V ≤ 89 dB ($\pm 1V$ in)
VXA1/A2		Minimum Load Maximum Capacitive Load Output Impedance Output Voltage D.C. Offset Total Distortion	10K Ω 50 pF 20 Ω 2.5 \pm 1.5V <100 mV ≤ 89 dB ($\pm 1V$ out)

ELECTRICAL SPECIFICATIONS (SC34350CQ DSP)**Absolute Maximum Ratings (Notes 1, 2)**

V_{CC} Supply Voltage	+6V
Input Signals with Respect to Ground	-0.3V to $V_{CC} + 0.6V$
Operating Temperature Range	0 to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering for 10 sec)	+300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Power dissipation temperature derating — Plastic Package: -12 mW/C from 65°C to 85°C.

DC Electrical Characteristics ($T_A = 0$ to 70°C, $V_{CC} = +5V \pm 5%$, GND = 0V)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.75	5.0	5.25	V
I_{CC}	Nominal Operating Current @ $V_{CC} = 5.0$ V, $F_{CLK} = 28.571$ MHz		75		mA
I_{CCPD}	Power Down Current @ $V_{CC} = 5.0$ V, $F_{CLK} = 28.571$ MHz		5		μ A
V_{IH}	High Level Input Voltage				
	CLKIN, CLKIN2	3.0		$V_{CC} + 0.3$	V
	CLKX, CLKR, TCLKX, TCLKR	2.5		$V_{CC} + 0.3$	V
	All others	2.0		$V_{CC} + 0.3$	V
V_{IL}	Low Level Input Voltage	-0.3		0.8	V
V_{OH}	High Level Output Voltage	2.4	3.0		V
V_{OL}	Low Level Output Voltage		0.3	0.6	V
F_{CLK}	Crystal Clock Frequency	$\pm 0.005\%$	28.571	$\pm 0.005\%$	MHz

ELECTRICAL SPECIFICATIONS (SC34380CQ)**Absolute Maximum Ratings (Notes 1, 2)**

V _{CC} Supply Voltage	+6V
Input Signals with Respect to Ground	-0.6V to V _{CC} + 0.6V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering for 10 sec)	+300°C

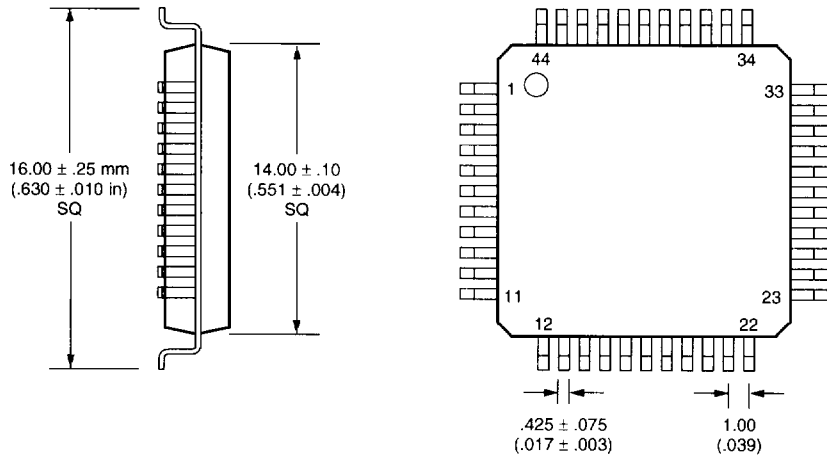
NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.

NOTE 2: Power dissipation temperature derating — Plastic Package: -12 mW/C from 65°C to 85°C.

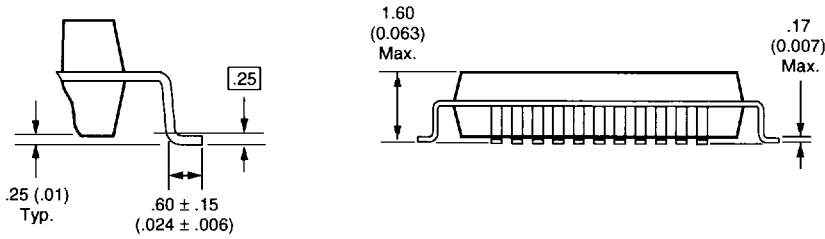
DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = +5V ± 5%, GND = 0V)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V _{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I _{CC}	Nominal Operating Current @ V _{CC} = 5.0 V, F _{CLK} = 28.571 MHz				mA
I _{CCPD}	Power Down Current @ V _{CC} = 5.0 V, F _{CLK} = 28.571 MHz				mA
V _{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	2 0.7 V _{CC}			V V
V _{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			0.8 0.3 V _{CC}	V V
VT+	Positive Hysteresis Threshold for RESET & RI input pins	2.6	2.8	3.4	V
VT-	Negative Hysteresis Threshold for RESET & RI input pins	1.8	2.2	2.5	V
V _{OH}	High Level Output Voltage for D7-D0, INT0 @ I _{OH} = 8 mA for RDY—open collector for other output pins @ I _{OH} = 2 mA	2.4			V
V _{OL}	Low Level Output Voltage for D7-D0, INT0 pins @ I _{OL} = 8 mA for RDY @ I _{OL} = 8 mA for other output pins @ I _{OL} = 2 mA			0.4	V
I _I	Leakage Current		±1	±20	µA
F _{CLK}	Crystal Clock Frequency	±0.005%		±0.005%	MHz

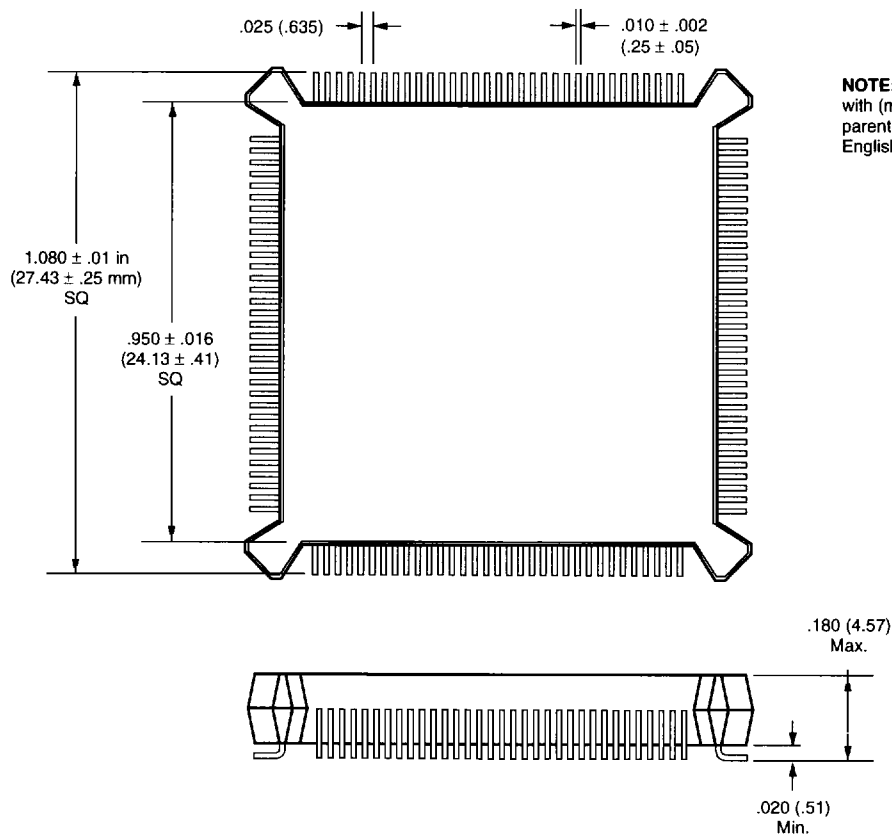
SC34320CT - 44-Pin Thin Quad Flat Pack (TQFP)



NOTE: All dimensions are in millimeters with (English-inch) conversion in parentheses. In case of conflict, metric dimensions govern.

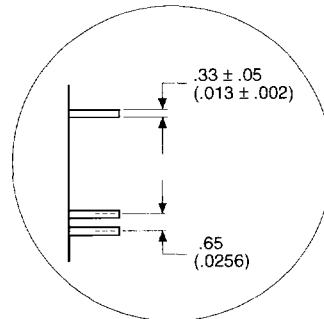
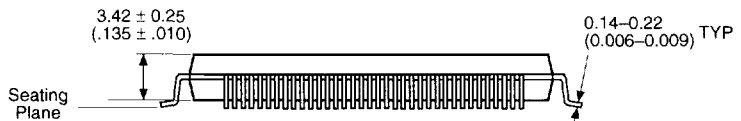
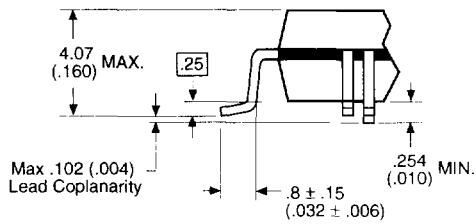
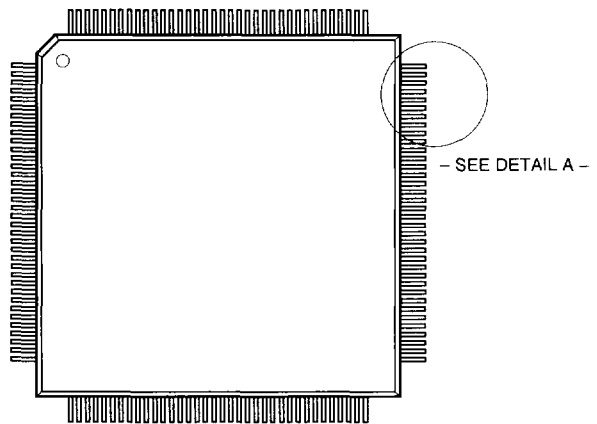
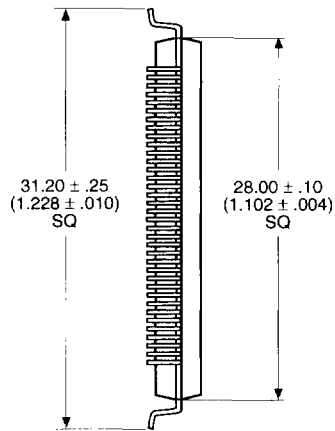


SC34350 - 132-Pin Bumpered Plastic Quad Flat Pack (PQFP)



NOTE: All dimensions are in inches with (metric-mm) conversion in parentheses. In case of conflict, English dimensions govern.

SC34380 - 144-Pin Plastic Quad Flat Pack (PQFP)



- DETAIL A -

NOTE: All dimensions are in millimeters with (English-inch) conversion in parentheses. In case of conflict, metric dimensions govern.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.