# HM51W16405B Series
# HM51W17405B Series

4,194,304-word × 4-bit Dynamic Random Access Memory

HITACHI

ADE-203-543 (Z)
Preliminary
Rev. 0.0
Apr. 20, 1996

## Description

The Hitachi HM51W16405B Series, HM51W17405B Series are CMOS dynamic RAMs organized 4,194,304-word × 4-bit. They employ the most advanced CMOS technology for high performance and low power. The HM51W16405B Series, HM51W17405B Series offer Extended Data Out (EDO) Page Mode as a high speed access mode.

## Features

- Single 3.3 V (±0.3 V)
- High speed
  - — Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - — Active mode : 360mW/324 mW/288 mW (max) (HM51W16405B Series)
    : 396mW/360 mW/324 mW (max) (HM51W17405B Series)
  - — Standby mode : 7.2 mW (max)
    : 0.36 mW (max) (L-version)
- EDO page mode capability
- Long refresh period
  - — 4096 refresh cycles : 64 ms (HM51W16405B Series)
    : 128 ms (L-version)
  - — 2048 refresh cycles : 32 ms (HM51W17405B Series)
    : 128 ms (L-version)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

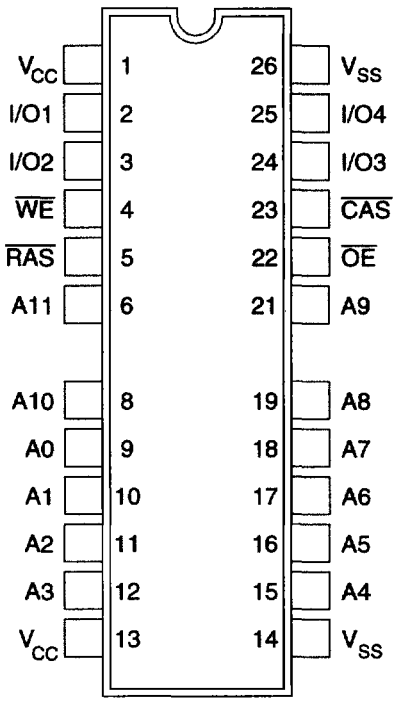
- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh (L-version)
- Battery backup operation (L-version)
- Test function
  - — 16-bit parallel test mode

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM51W16405BS-6 | 60 ns | 300-mil 26-pin plastic SOJ (CP-26/24DB) |
| HM51W16405BS-7 | 70 ns | |
| HM51W16405BS-8 | 80 ns | |
| HM51W16405BLS-6 | 60 ns | |
| HM51W16405BLS-7 | 70 ns | |
| HM51W16405BLS-8 | 80 ns | |
| HM51W17405BS-6 | 60 ns | |
| HM51W17405BS-7 | 70 ns | |
| HM51W17405BS-8 | 80 ns | |
| HM51W17405BLS-6 | 60 ns | |
| HM51W17405BLS-7 | 70 ns | |
| HM51W17405BLS-8 | 80 ns | |
| HM51W16405BTS-6 | 60 ns | 300-mil 26-pin plastic TSOP II (TTP-26/24DA) |
| HM51W16405BTS-7 | 70 ns | |
| HM51W16405BTS-8 | 80 ns | |
| HM51W16405BLTS-6 | 60 ns | |
| HM51W16405BLTS-7 | 70 ns | |
| HM51W16405BLTS-8 | 80 ns | |
| HM51W17405BTS-6 | 60 ns | |
| HM51W17405BTS-7 | 70 ns | |
| HM51W17405BTS-8 | 80 ns | |
| HM51W17405BLTS-6 | 60 ns | |
| HM51W17405BLTS-7 | 70 ns | |
| HM51W17405BLTS-8 | 80 ns | |

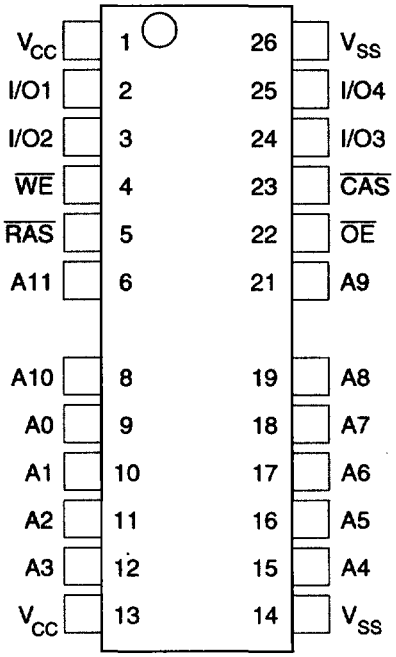
## Pin Arrangement

HM51W16405BS/BLS Series




(Top view)

HM51W16405BTS/BLTS Series



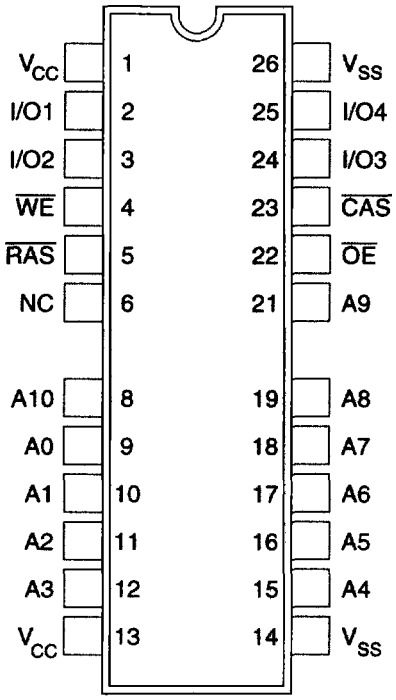

(Top view)

## Pin Description

| Pin name | Function | |
|---|---|---|
| A0 to A11 | Address input | |
| | — Row/Refresh address | A0 to A11 |
| | — Column address | A0 to A9 |
| I/O1 to I/O4 | Data input/Data output | |
| $\overline{RAS}$ | Row address strobe | |
| $\overline{CAS}$ | Column address strobe | |
| $\overline{WE}$ | Read/Write enable | |
| $\overline{OE}$ | Output enable | |
| $V_{CC}$ | Power supply | |
| $V_{SS}$ | Ground | |

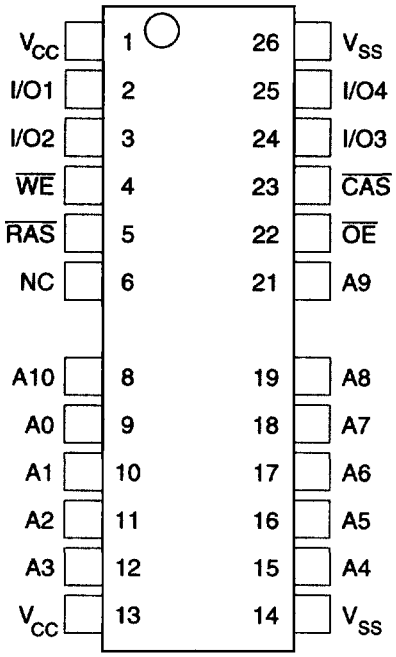
## Pin Arrangement

HM51W17405BS/BLS Series




(Top view)

HM51W17405BTS/BLTS Series

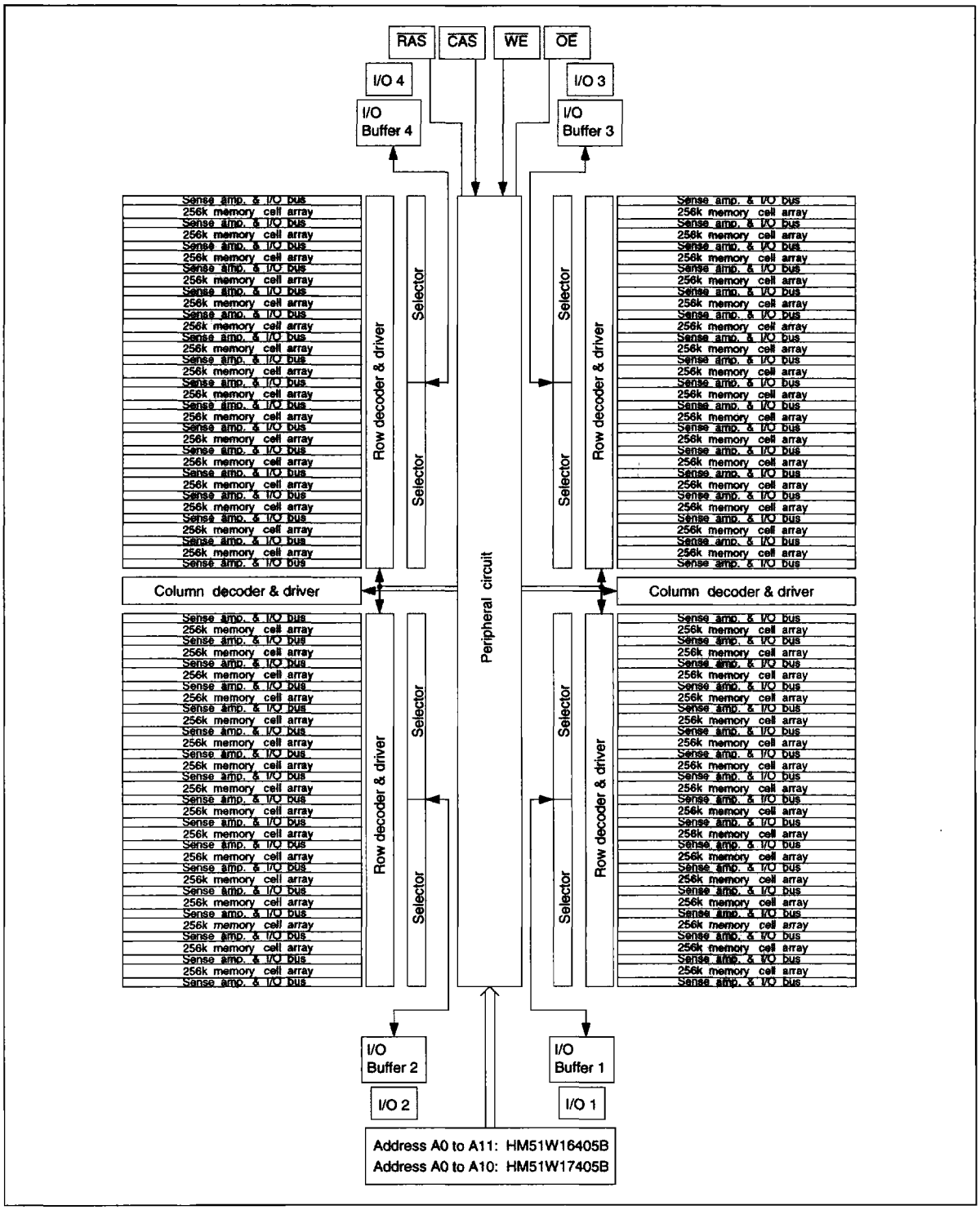



(Top view)

## Pin Description

| Pin name | Function |
|---|---|
| A0 to A10 | Address input<br>— Row/Refresh address A0 to A10<br>— Column address A0 to A10 |
| I/O1 to I/O4 | Data input/Data output |
| $\overline{RAS}$ | Row address strobe |
| $\overline{CAS}$ | Column address strobe |
| $\overline{WE}$ | Read/Write enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

## Block Diagram



## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | −0.5 to $V_{CC}$ + 0.5 (≤ 4.6 V (max)) | V |
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | −0.5 to 4.6 | V |
| Short circuit output current | Iout | 50 | mA |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | −55 to +125 | °C |

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | 1, 2 |
| Input high voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | −0.3 | — | 0.8 | V | 1 |

Note: 1. All voltage referred to $V_{SS}$.

## DC Characteristics

(Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V) (HM51W16405B Series)

| | | HM51W16405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test conditions |
| Operating current*1, *2 | $I_{CC1}$ | — | 80 | — | 70 | — | 65 | mA | $t_{RC}$ = min |
| Standby current | $I_{CC2}$ | — | 2 | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$<br>Dout = High-Z |
| | | — | 1 | — | 1 | — | 1 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| Standby current (L-version) | $I_{CC2}$ | — | 100 | — | 100 | — | 100 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| $\overline{RAS}$-only refresh current*2 | $I_{CC3}$ | — | 80 | — | 70 | — | 65 | mA | $t_{RC}$ = min |
| Standby current*1 | $I_{CC5}$ | — | 5 | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{CAS}$ = $V_{IL}$<br>Dout = enable |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | 80 | — | 70 | — | 65 | mA | $t_{RC}$ = min |
| EDO page mode current*1, *3 | $I_{CC7}$ | — | 100 | — | 90 | — | 80 | mA | $t_{HPC}$ = min |
| Battery backup current | $I_{CC10}$ | — | 300 | — | 300 | — | 300 | µA | CMOS interface<br>Dout = High-Z, CBR refresh: $t_{RC}$ = 31.3 µs<br>$t_{RAS}$ ≤ 0.3 µs |
| Self refresh mode current (L-version) | $I_{CC11}$ | — | 200 | — | 200 | — | 200 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V<br>Dout = High-Z |
| Input leakage current | $I_{LI}$ | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ 4.6 V |
| Output leakage current | $I_{LO}$ | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ 4.6 V<br>Dout = disable |
| Output high voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –2 mA |
| Output low voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

Notes : 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.

## DC Characteristics

(Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V) (HM51W17405B Series)

| | | HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test conditions |
| Operating current*1, *2 | $I_{CC1}$ | — | 110 | — | 100 | — | 90 | mA | $t_{RC}$ = min |
| Standby current | $I_{CC2}$ | — | 2 | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$<br>Dout = High-Z |
| | | — | 1 | — | 1 | — | 1 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| Standby current (L-version) | $I_{CC2}$ | — | 100 | — | 100 | — | 100 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| $\overline{RAS}$-only refresh current*2 | $I_{CC3}$ | — | 110 | — | 100 | — | 90 | mA | $t_{RC}$ = min |
| Standby current*1 | $I_{CC5}$ | — | 5 | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{CAS}$ = $V_{IL}$<br>Dout = enable |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | 110 | — | 100 | — | 90 | mA | $t_{RC}$ = min |
| EDO page mode current*1, *3 | $I_{CC7}$ | — | 110 | — | 100 | — | 90 | mA | $t_{HPC}$ = min |
| Battery backup current | $I_{CC10}$ | — | 300 | — | 300 | — | 300 | µA | CMOS interface<br>Dout = High-Z, CBR refresh: $t_{RC}$ = 62.5 µs<br>$t_{RAS}$ ≤ 0.3 µs |
| Self refresh mode current (L-version) | $I_{CC11}$ | — | 200 | — | 200 | — | 200 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≤ 0.2 V<br>Dout = High-Z |
| Input leakage current | $I_{LI}$ | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ 4.6 V |
| Output leakage current | $I_{LO}$ | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ 4.6 V<br>Dout = disable |
| Output high voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –2 mA |
| Output low voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

Notes : 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.

3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.

## Capacitance ($Ta = 25°C$, $V_{CC} = 3.3\ V \pm 0.3\ V$)

| Parameter | Symbol | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input capacitance (Address) | $C_{I1}$ | — | 5 | pF | 1 |
| Input capacitance (Clocks) | $C_{I2}$ | — | 7 | pF | 1 |
| Output capacitance (Data-in, Data-out) | $C_{I/O}$ | — | 7 | pF | 1, 2 |

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V) *1, *2, *18

### Test Conditions

- Input rise and fall time: 2 ns
- Input levels: $V_{IL}$ = 0 V, $V_{IH}$ = 3 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + $C_L$ (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

| | | HM51W16405B/HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Random read or write cycle time | $t_{RC}$ | 104 | — | 124 | — | 144 | — | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 40 | — | 50 | — | 60 | — | ns | |
| $\overline{CAS}$ precharge time | $t_{CP}$ | 10 | — | 13 | — | 15 | — | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 60 | 10000 | 70 | 10000 | 80 | 10000 | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 10 | 10000 | 13 | 10000 | 15 | 10000 | ns | |
| Row address setup time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row address hold time | $t_{RAH}$ | 10 | — | 10 | — | 10 | — | ns | |
| Column address setup time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column address hold time | $t_{CAH}$ | 10 | — | 13 | — | 15 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 45 | 20 | 52 | 20 | 60 | ns | 3 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 15 | 30 | 15 | 35 | 15 | 40 | ns | 4 |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 15 | — | 18 | — | 20 | — | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 48 | — | 58 | — | 68 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{OE}$ to Din delay time | $t_{OED}$ | 15 | — | 18 | — | 20 | — | ns | 5 |
| $\overline{OE}$ delay time from Din | $t_{DZO}$ | 0 | — | 0 | — | 0 | — | ns | 6 |
| $\overline{CAS}$ delay time from Din | $t_{DZC}$ | 0 | — | 0 | — | 0 | — | ns | 6 |
| Transition time (rise and fall) | $t_T$ | 2 | 50 | 2 | 50 | 2 | 50 | ns | 7 |

## Read Cycle

| | | HM51W16405B/HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | — | 60 | — | 70 | — | 80 | ns | 8, 9, 19 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | — | 15 | — | 18 | — | 20 | ns | 9, 10, 17, 19 |
| Access time from address | $t_{AA}$ | — | 30 | — | 35 | — | 40 | ns | 9, 11, 17, 19 |
| Access time from $\overline{OE}$ | $t_{OEA}$ | — | 15 | — | 18 | — | 20 | ns | 9, 19 |
| Read command setup time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read command hold time to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 12 |
| Read command hold time from $\overline{RAS}$ | $t_{RCHR}$ | 60 | — | 70 | — | 80 | — | ns | |
| Read command hold time to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 12 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 30 | — | 35 | — | 40 | — | ns | |
| Column address to $\overline{CAS}$ lead time | $t_{CAL}$ | 18 | — | 23 | — | 28 | — | ns | |
| $\overline{CAS}$ to output in low-Z | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | |
| Output data hold time | $t_{OH}$ | 3 | — | 3 | — | 3 | — | ns | |
| Output data hold time from $\overline{OE}$ | $t_{OHO}$ | 3 | — | 3 | — | 3 | — | ns | |
| Output buffer turn-off time | $t_{OFF}$ | — | 15 | — | 15 | — | 15 | ns | 13 |
| Output buffer turn-off to $\overline{OE}$ | $t_{OEZ}$ | — | 15 | — | 15 | — | 15 | ns | 13 |
| $\overline{CAS}$ to Din delay time | $t_{CDD}$ | 15 | — | 18 | — | 20 | — | ns | 5 |
| Output data hold time from $\overline{RAS}$ | $t_{OHR}$ | 3 | — | 3 | — | 3 | — | ns | |
| Output buffer turn-off to $\overline{RAS}$ | $t_{OFR}$ | — | 15 | — | 15 | — | 15 | ns | |
| Output buffer turn-off to $\overline{WE}$ | $t_{WEZ}$ | — | 15 | — | 15 | — | 15 | ns | |
| $\overline{WE}$ to Din delay time | $t_{WED}$ | 15 | — | 18 | — | 20 | — | ns | |
| $\overline{RAS}$ to Din delay time | $t_{RDD}$ | 15 | — | 18 | — | 20 | — | ns | |

### Write Cycle

| | | HM51W16405B/HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Write command setup time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 14 |
| Write command hold time | $t_{WCH}$ | 10 | — | 13 | — | 15 | — | ns | |
| Write command pulse width | $t_{WP}$ | 10 | — | 10 | — | 10 | — | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 10 | — | 13 | — | 15 | — | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 10 | — | 13 | — | 15 | — | ns | |
| Data-in setup time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 15 |
| Data-in hold time | $t_{DH}$ | 10 | — | 13 | — | 15 | — | ns | 15 |

### Read-Modify-Write Cycle

| | | HM51W16405B/HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Read-modify-write cycle time | $t_{RWC}$ | 149 | — | 175 | — | 199 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | 82 | — | 95 | — | 107 | — | ns | 14 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | 37 | — | 43 | — | 47 | — | ns | 14 |
| Column address to $\overline{WE}$ delay time | $t_{AWD}$ | 52 | — | 60 | — | 67 | — | ns | 14 |
| $\overline{OE}$ hold time from $\overline{WE}$ | $t_{OEH}$ | 15 | — | 18 | — | 20 | — | ns | |

### Refresh Cycle

| | | HM51W16405B/HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $\overline{CAS}$ setup time (CBR refresh cycle) | $t_{CSR}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{CAS}$ hold time (CBR refresh cycle) | $t_{CHR}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{WE}$ setup time (CBR refresh cycle) | $t_{WRP}$ | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{WE}$ hold time (CBR refresh cycle) | $t_{WRH}$ | 10 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | $t_{RPC}$ | 0 | — | 0 | — | 0 | — | ns | |

### EDO Page Mode Cycle

| | | HM51W16405B/HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| EDO page mode cycle time | $t_{HPC}$ | 25 | — | 30 | — | 35 | — | ns | 20 |
| EDO page mode $\overline{RAS}$ pulse width | $t_{RASP}$ | — | 100000 | — | 100000 | — | 100000 | ns | 16 |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | — | 35 | — | 40 | — | 45 | ns | 9, 17, 19 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{CPRH}$ | 35 | — | 40 | — | 45 | — | ns | |
| Output data hold time from $\overline{CAS}$ low | $t_{DOH}$ | 3 | — | 3 | — | 3 | — | ns | 9, 17 |
| $\overline{CAS}$ hold time referred $\overline{OE}$ | $t_{COL}$ | 10 | — | 13 | — | 15 | — | ns | |
| $\overline{CAS}$ to $\overline{OE}$ setup time | $t_{COP}$ | 5 | — | 5 | — | 5 | — | ns | |
| Read command hold time from $\overline{CAS}$ precharge | $t_{RCHC}$ | 35 | — | 40 | — | 45 | — | ns | |

### EDO Page Mode Read-Modify-Write Cycle

| | | HM51W16405B/HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| EDO page mode read- modify-write cycle time | $t_{HPRWC}$ | 79 | — | 90 | — | 99 | — | ns | |
| $\overline{WE}$ delay time from $\overline{CAS}$ precharge | $t_{CPW}$ | 54 | — | 62 | — | 69 | — | ns | 14 |

### Test Mode Cycle *[18]

| | | HM51W16405B/HM51W17405B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Test mode $\overline{WE}$ setup time | $t_{WTS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Test mode $\overline{WE}$ hold time | $t_{WTH}$ | 10 | — | 10 | — | 10 | — | ns | |

### Refresh (HM51W16405B Series)

| Parameter | Symbol | Max | Unit | Notes |
|---|---|---|---|---|
| Refresh period | $t_{REF}$ | 64 | ms | 4096 cycles |
| Refresh period (L-version) | $t_{REF}$ | 128 | ms | 4096 cycles |

**Refresh** (HM51W17405B Series)

| Parameter | Symbol | Max | Unit | Notes |
|---|---|---|---|---|
| Refresh period | $t_{REF}$ | 32 | ms | 2048 cycles |
| Refresh period (L-version) | $t_{REF}$ | 128 | ms | 2048 cycles |

**Self Refresh Mode** (L-version)

| | | HM51W16405BL/HM51W17405BL | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -6 | | -7 | | -8 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $\overline{RAS}$ pulse width (self refresh) | $t_{RASS}$ | 100 | — | 100 | — | 100 | — | µs | |
| $\overline{RAS}$ precharge time (self refresh) | $t_{RPS}$ | 110 | — | 130 | — | 150 | — | ns | |
| $\overline{CAS}$ hold time (self refresh) | $t_{CHS}$ | –50 | — | –50 | — | –50 | — | ns | |

Notes:
1. AC measurements assume $t_T = 2$ ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
4. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
5. Either $t_{OED}$ or $t_{CDD}$ must be satisfied.
6. Either $t_{DZO}$ or $t_{DZC}$ must be satisfied.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycles.
13. $t_{OFF}$ (max) and $t_{OEZ}$ (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPW}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. $t_{RASP}$ defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among $t_{AA}$, $t_{CAC}$ and $t_{CPA}$.
18. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M ×4 are don't care during test mode. Test mode is set by performing a $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.

    If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.

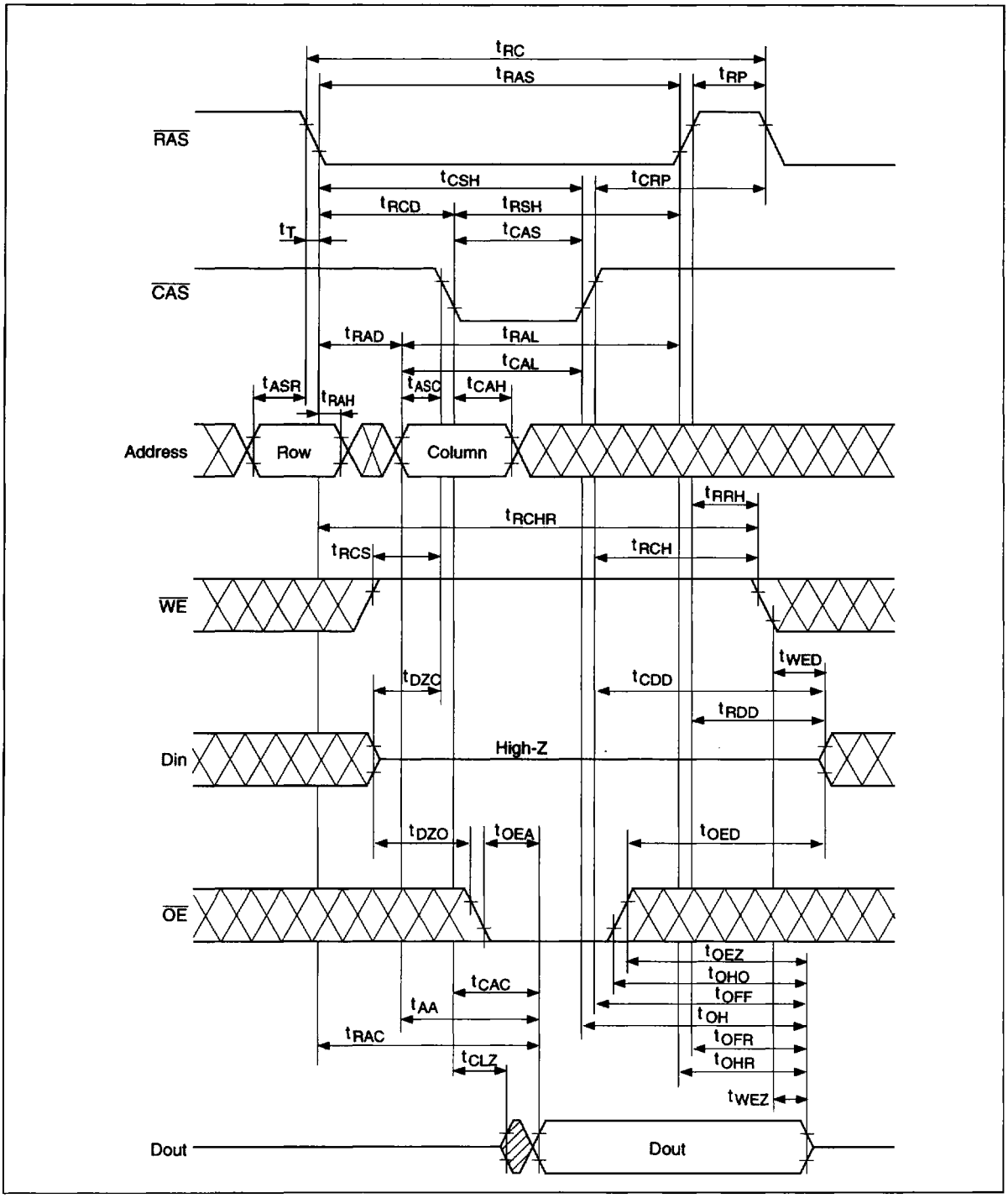
    Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

    To get out of test mode and enter a normal operation mode, perform either a regular $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or $\overline{RAS}$-only refresh cycle.
19. In a test mode read cycle, the value of $t_{RAC}$, $t_{AA}$, $t_{CAC}$ and $t_{CPA}$ is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
20. $t_{HPC}$ (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2\ t_T$) becomes greater than the specified $t_{HPC}$ (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Please do not use $t_{RASS}$ timing, 10 µs ≤ $t_{RASS}$ ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS}$ > 100 µs, then $\overline{RAS}$ precharge time should use $t_{RPS}$ instead of $t_{RP}$.
22. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
23. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 2048 cycles (4096 cycles: HM51W16405B Series, 2048 cycles: HM51W17405B Series) of distributed CBR refresh with 15.6 µs interval should be executed within 64 or 32 ms (64 ms: HM51W16405B Series, 32 ms: HM51W17405B Series) immediately after exiting from and before entering into the self refresh mode.
24. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
25. XXX: H or L (H: $V_{IH}$ (min) ≤ $V_{IN}$ ≤ $V_{IH}$ (max), L: $V_{IL}$ (min) ≤ $V_{IN}$ ≤ $V_{IL}$ (max))

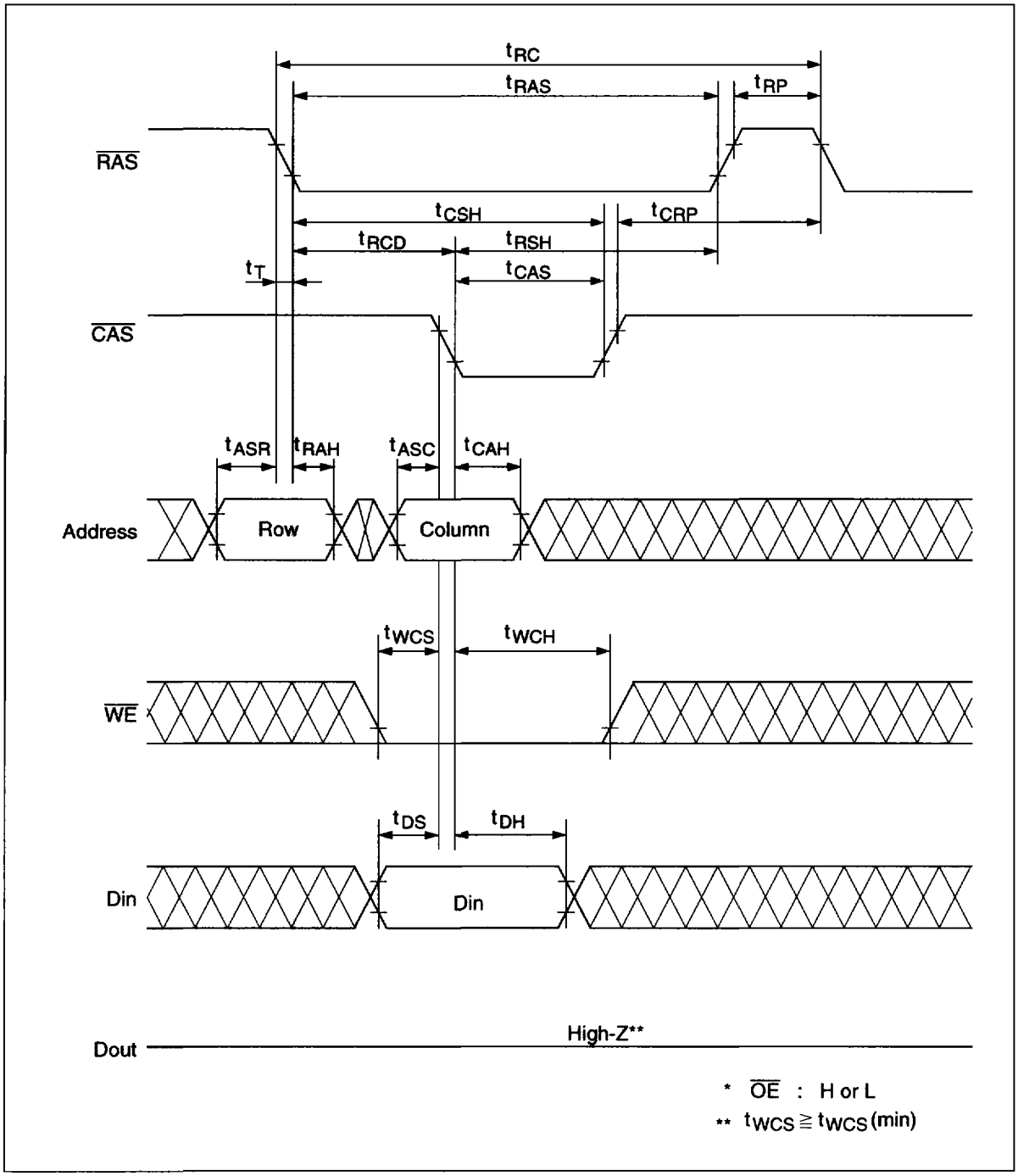
    ///////: Invalid Dout

## Timing Waveforms*[25]

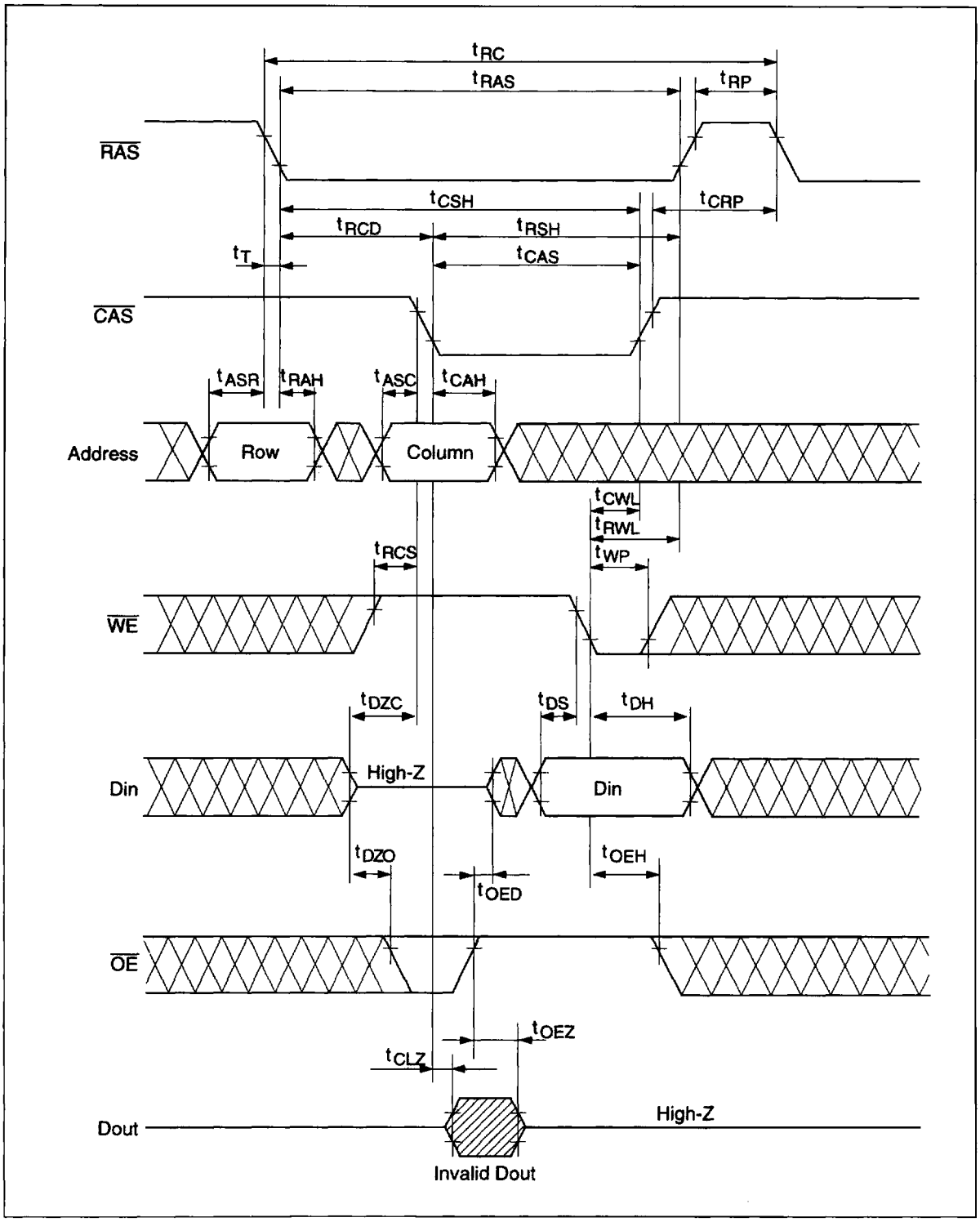
### Read Cycle



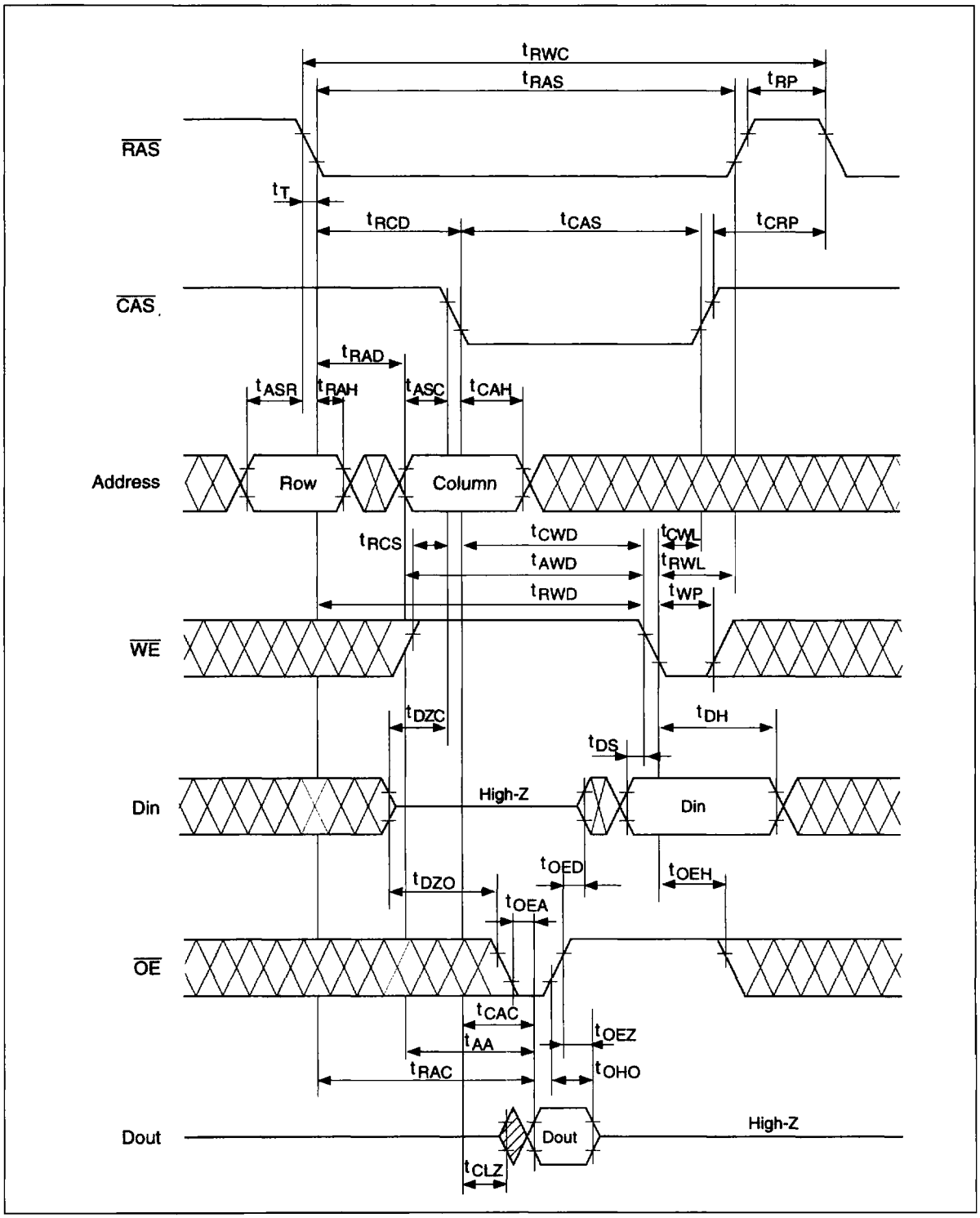
**Early Write Cycle**



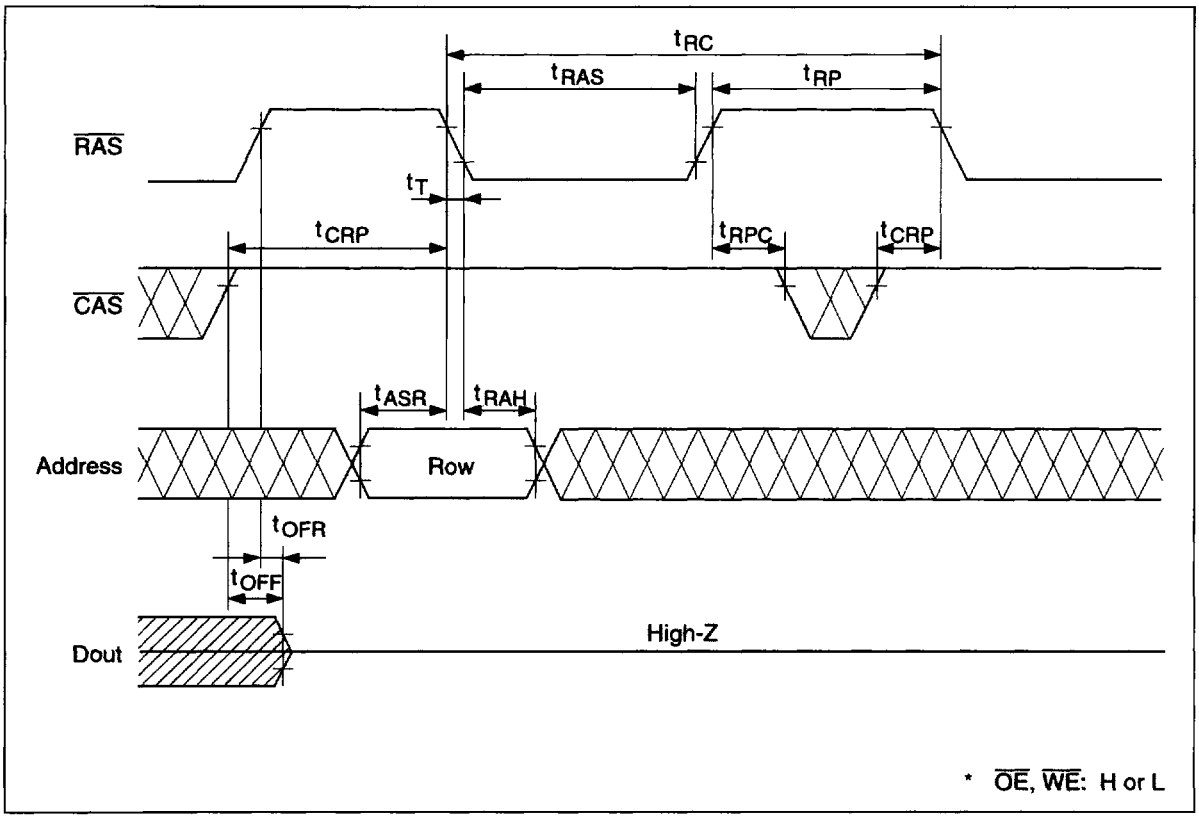
**Delayed Write Cycle**



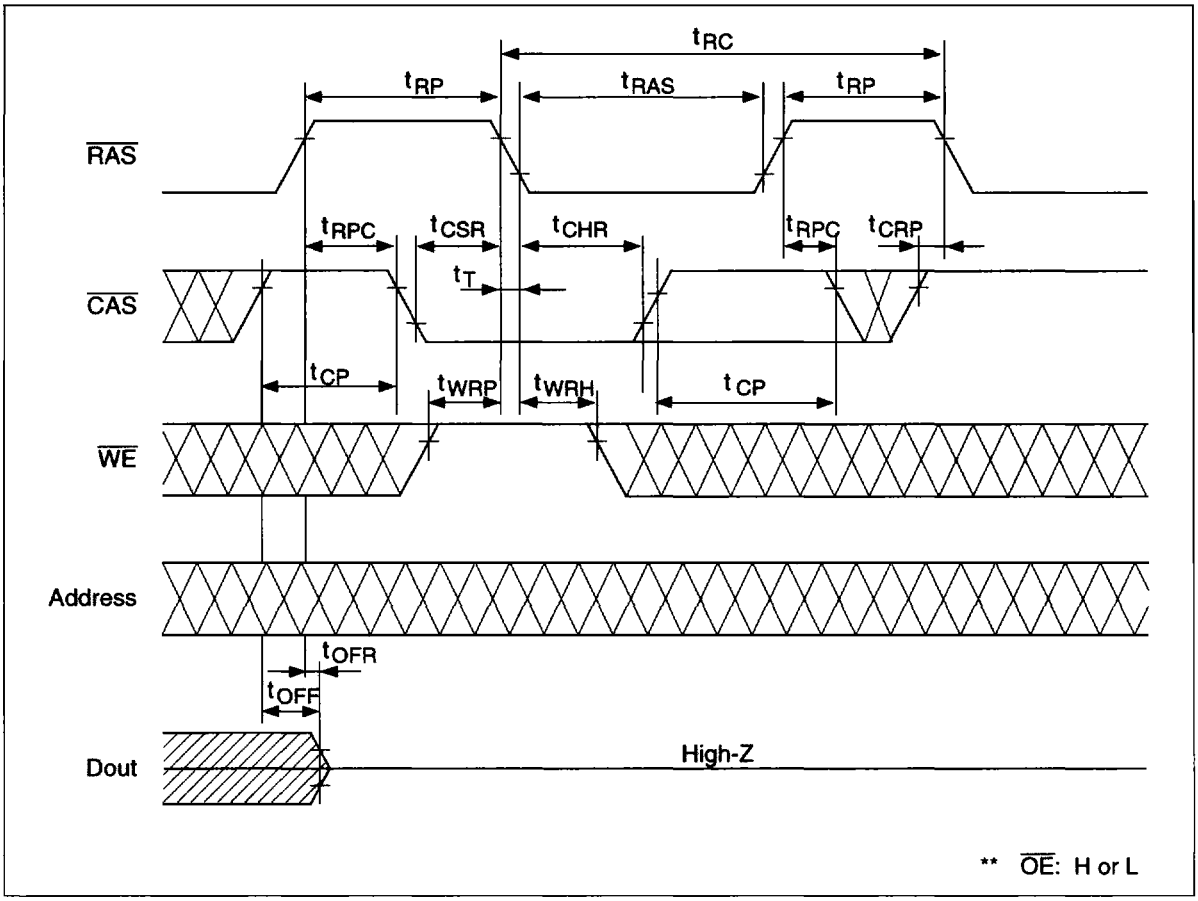
**Read-Modify-Write Cycle**



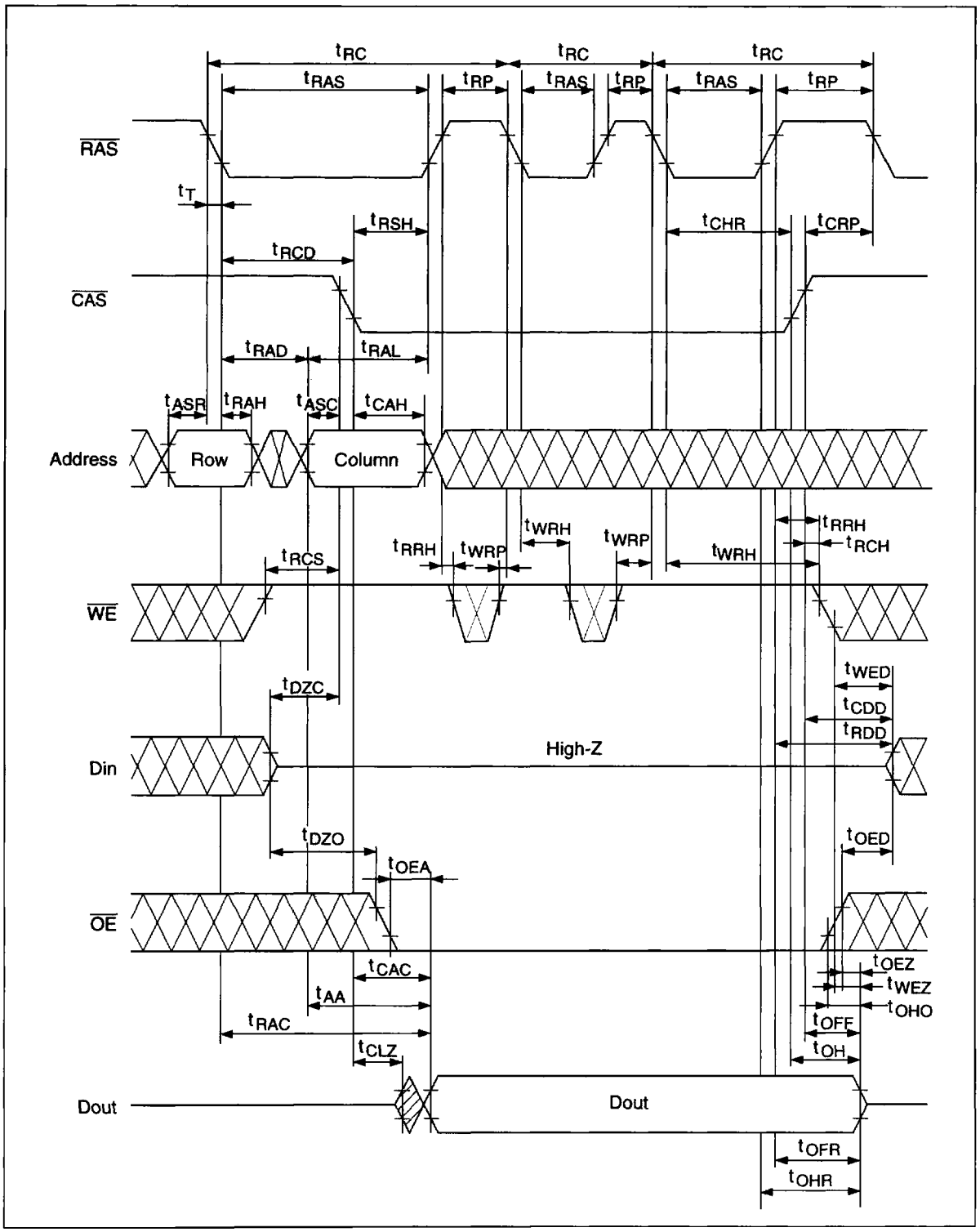
**$\overline{\text{RAS}}$-Only Refresh Cycle**



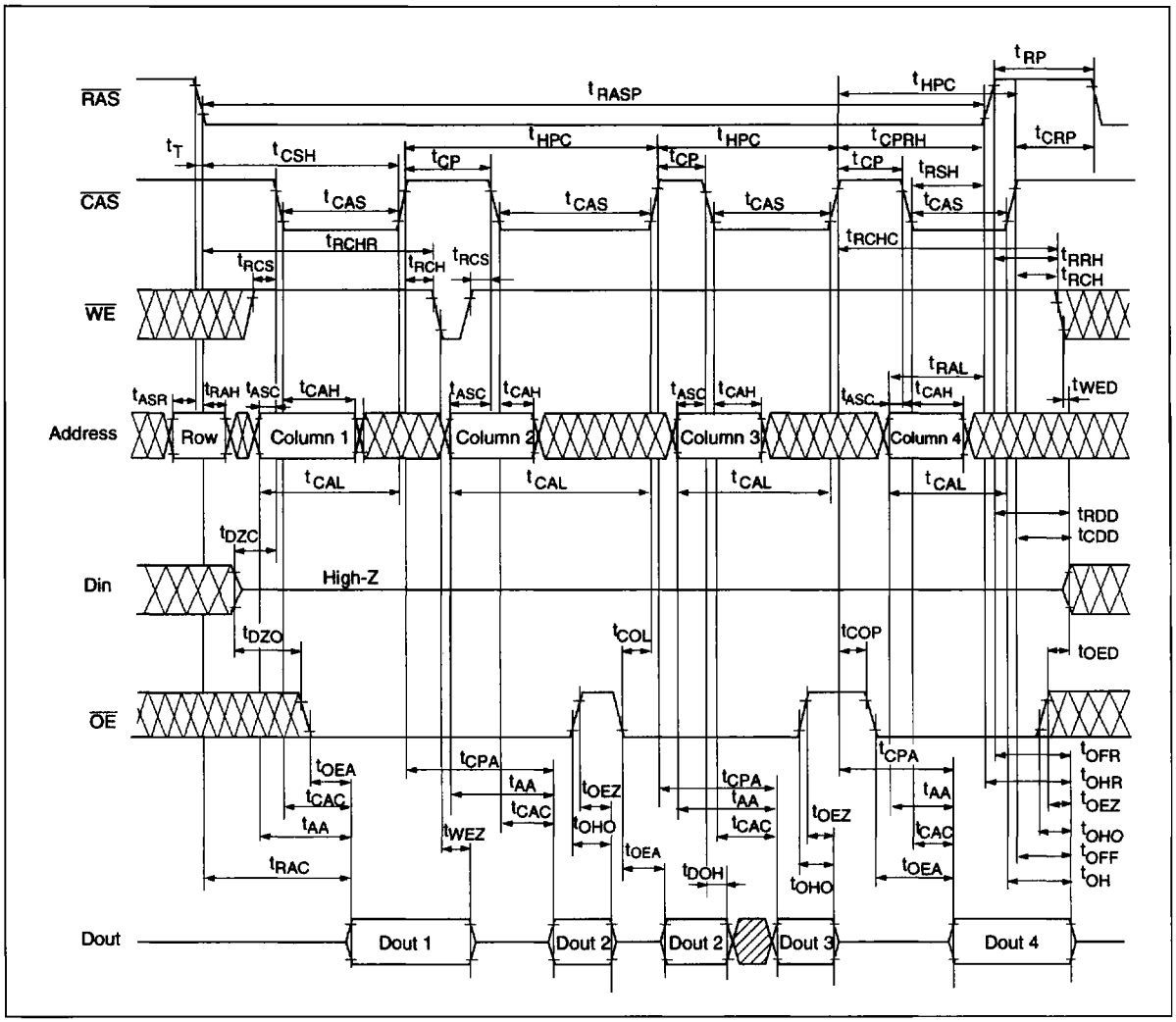
### $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



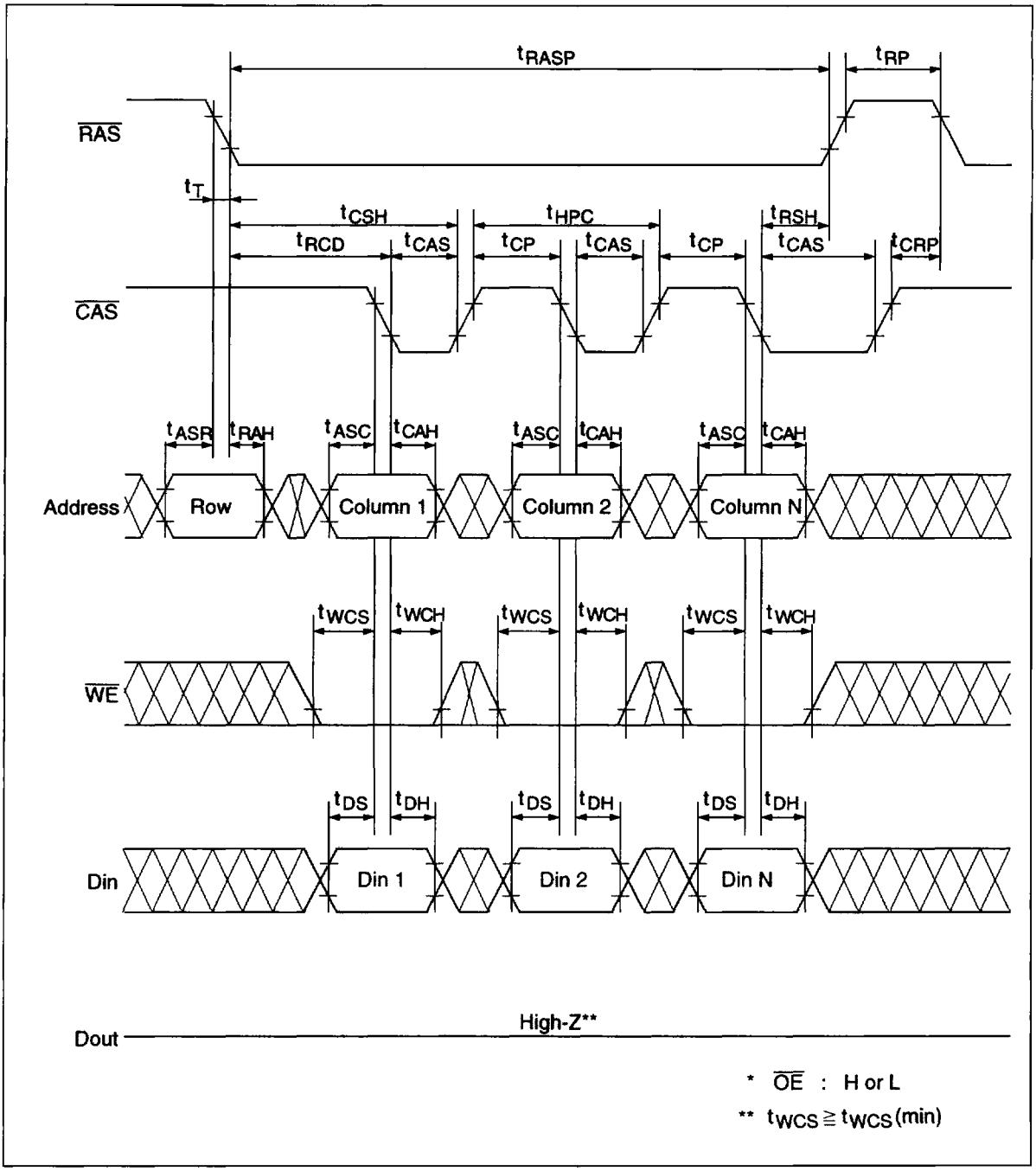
**Hidden Refresh Cycle**



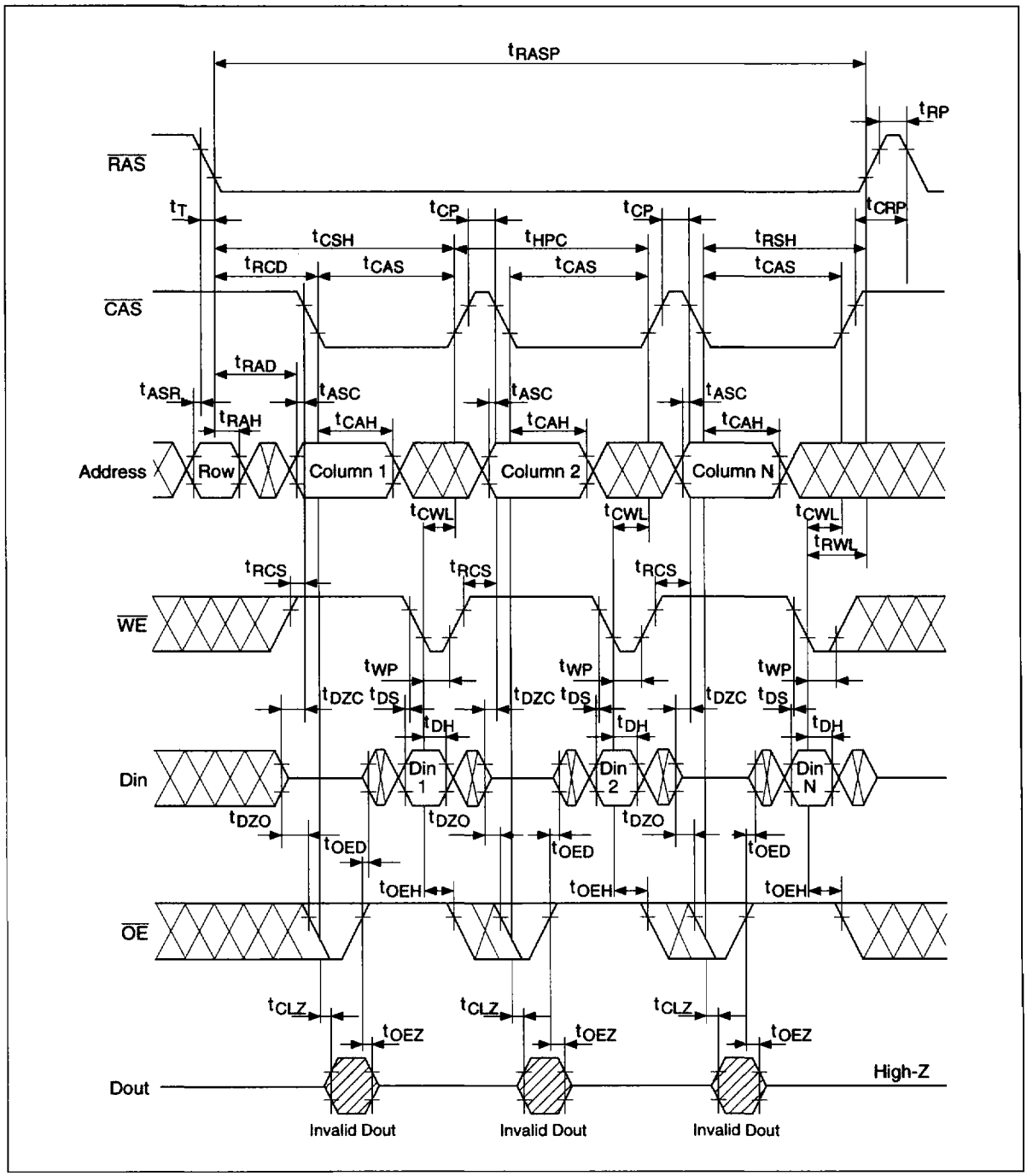
## EDO Page Mode Read Cycle



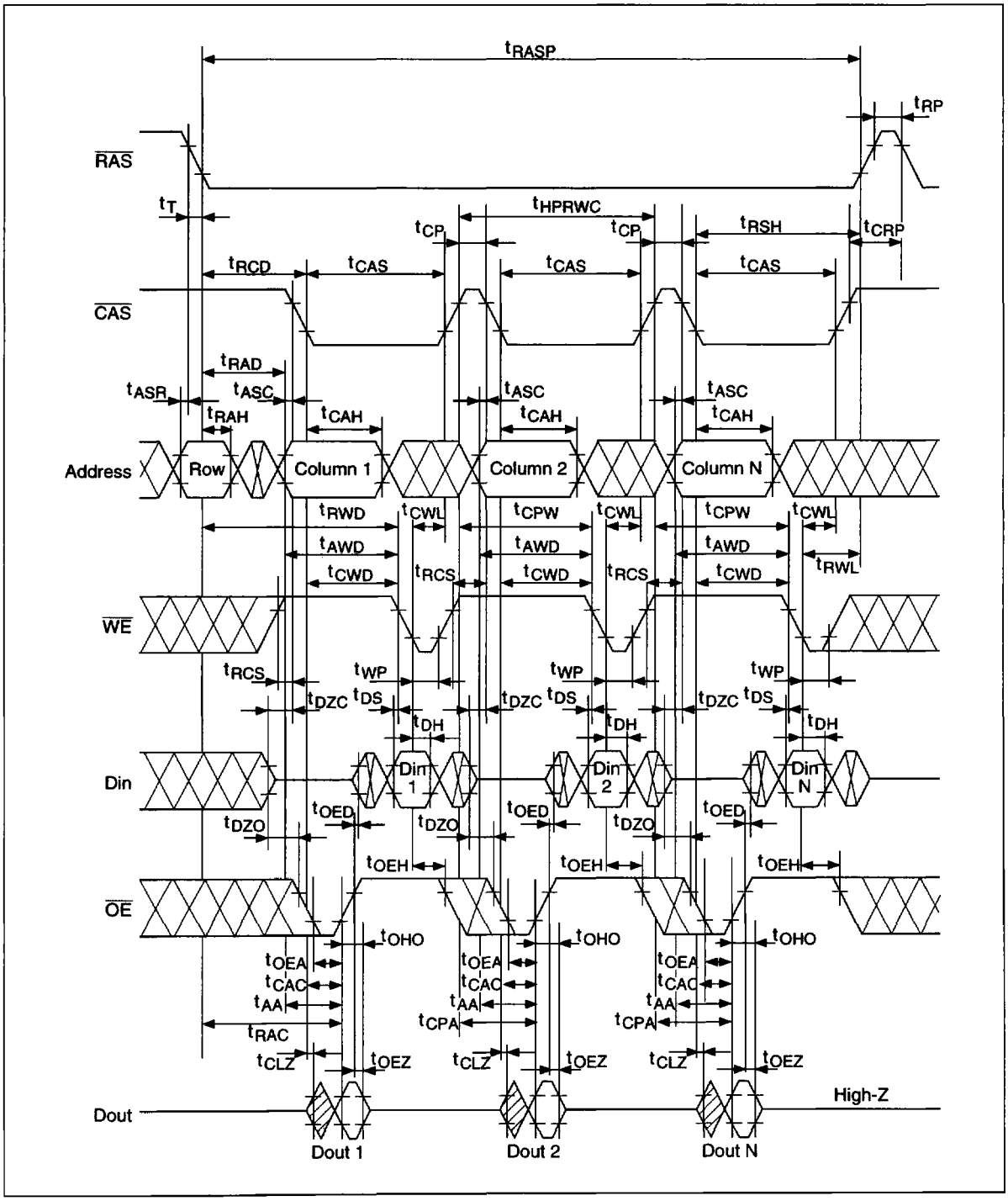
**EDO Page Mode Early Write Cycle**



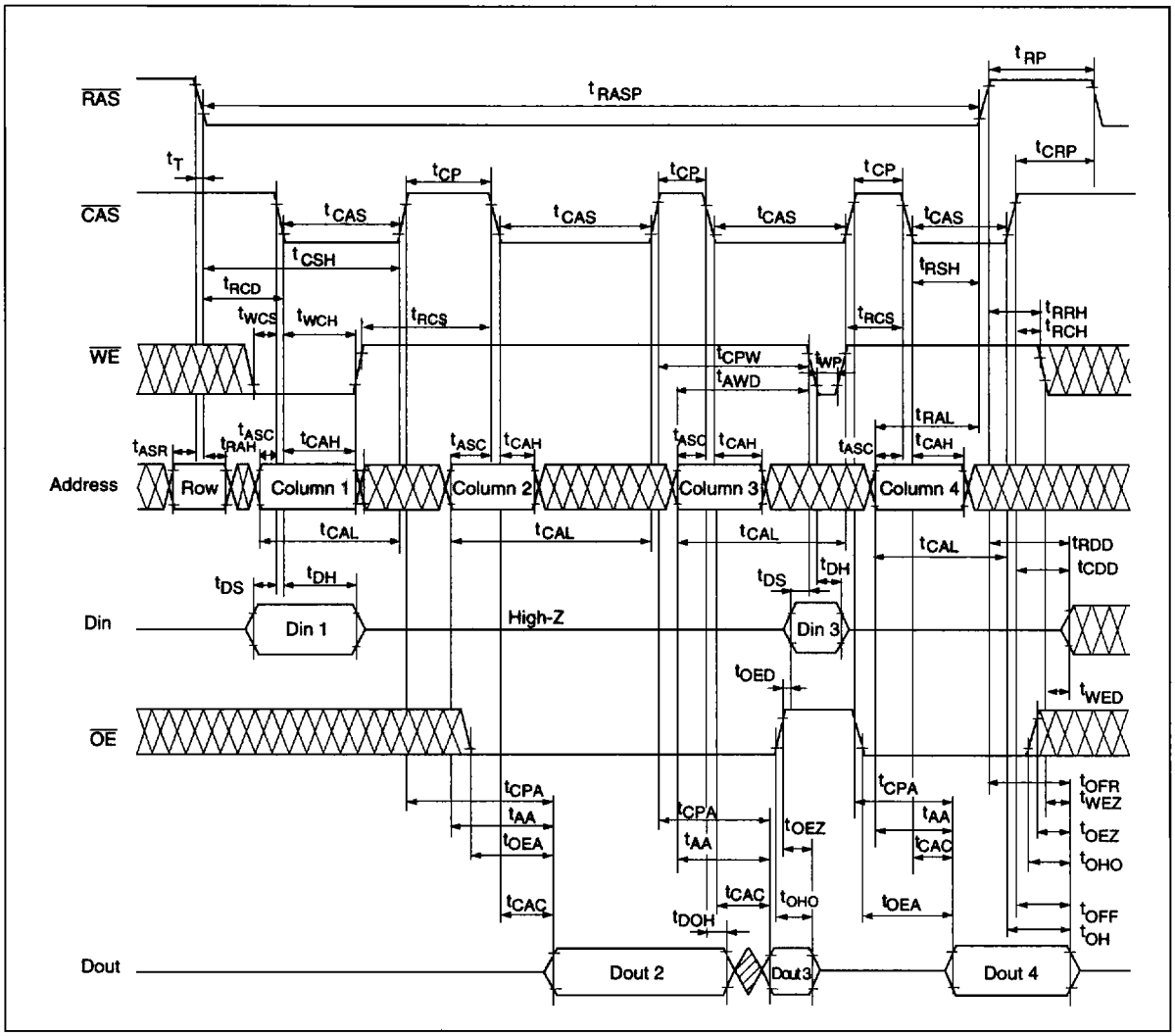
## EDO Page Mode Delayed Write Cycle



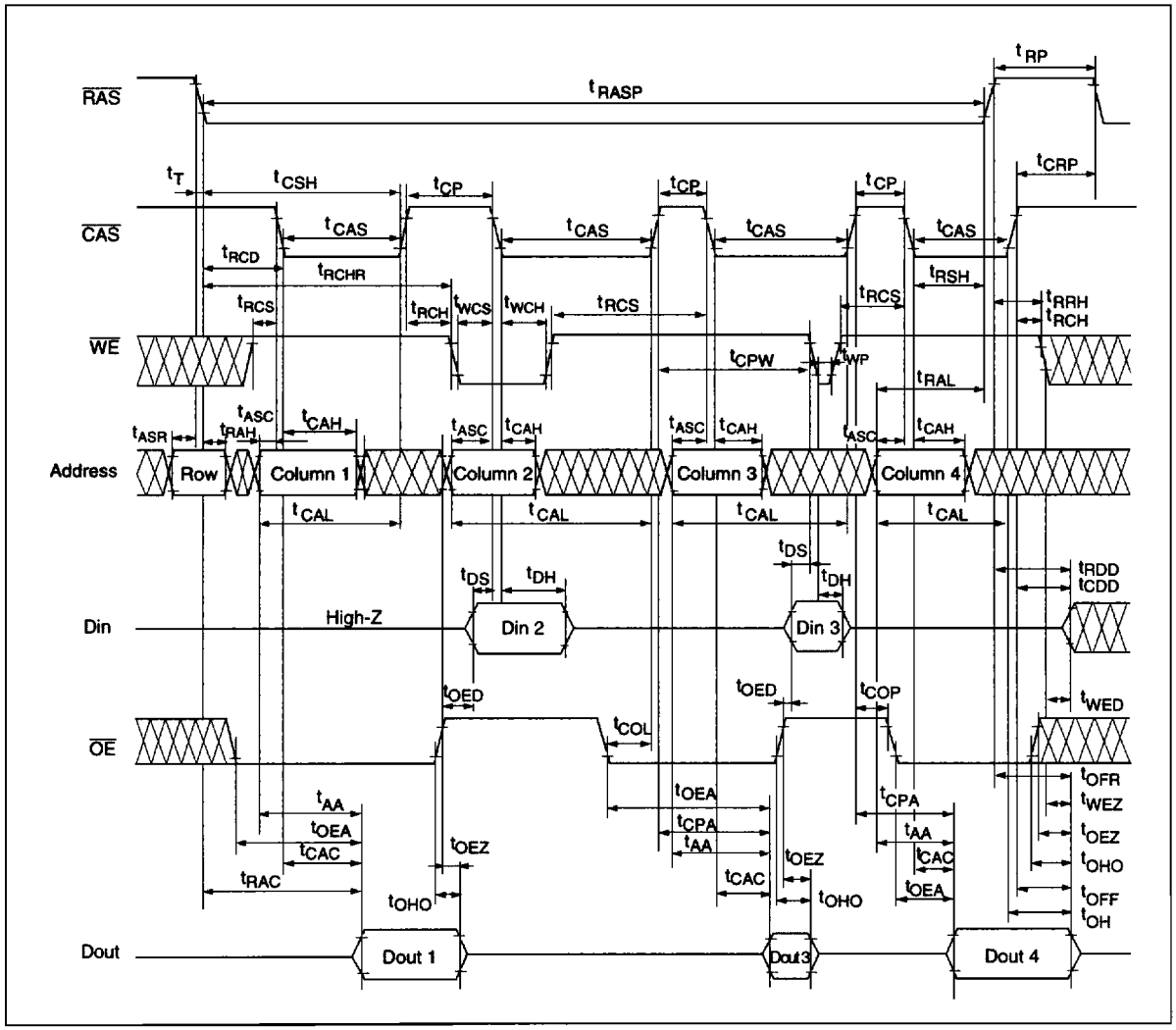
**EDO Page Mode Read-Modify-Write Cycle**



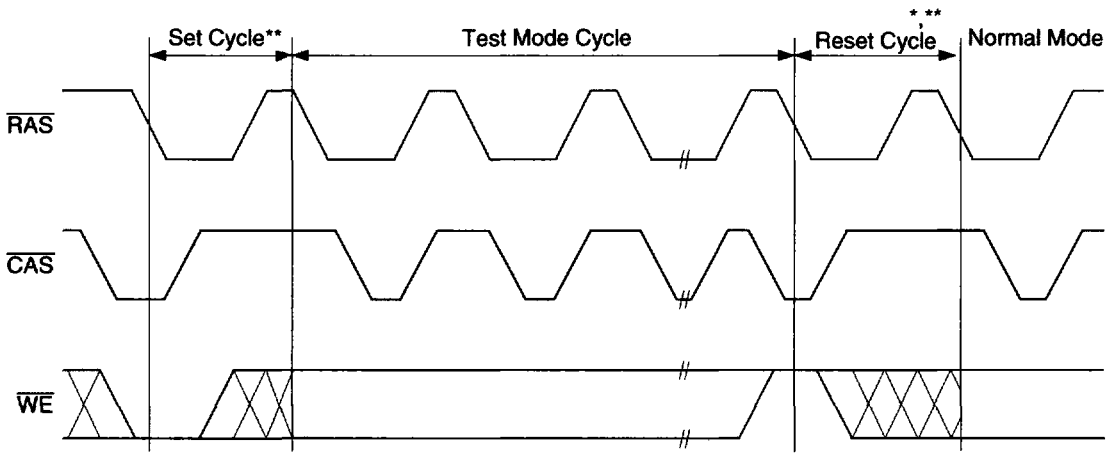
## EDO Page Mode Mix Cycle (1)



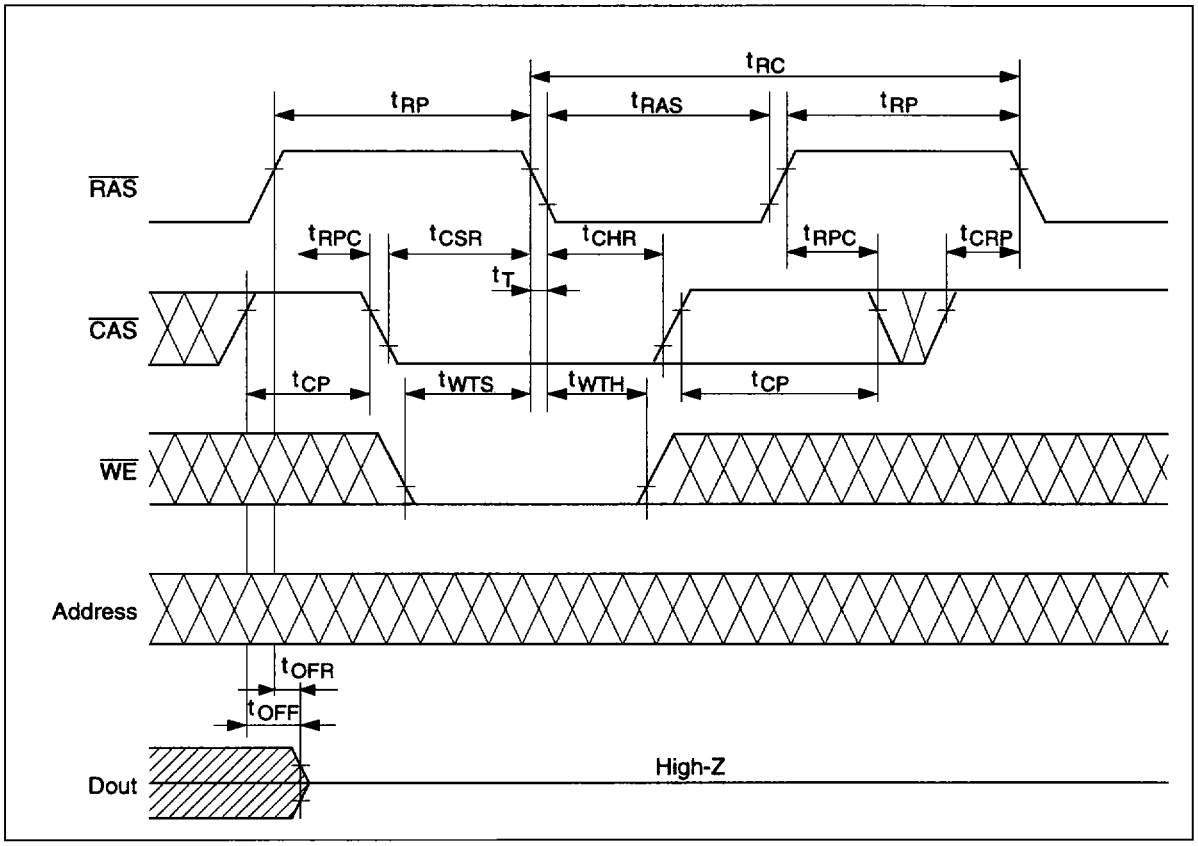
## EDO Page Mode Mix Cycle (2)



**Test Mode Cycle** *[18]



**Test Mode Set Cycle**



**Self Refresh Cycle** (L-version)*[21, 22, 23, 24]