MSM6308

SOLID STATE RECORDING LSI (FOR 256K-bit DRAM)

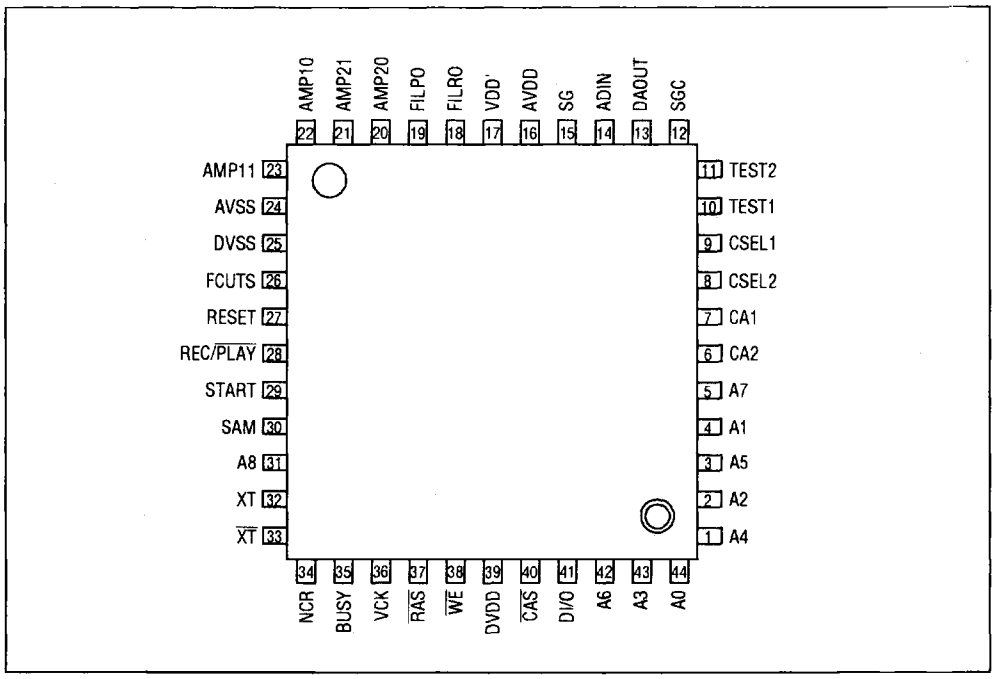
GENERAL DESCRIPTION

The MSM6308 is a solid-state recording LSI developed using the ADPCM (Adaptive Differential Pulse Code Modulation) technology. When an external microphone, speaker driving amplifier, speaker and a 256K-bit DRAM to store ADPCM data are connected to the MSM6308, it can be used to record and play back voice or other sounds in a manner similar to that of a tape recorder.

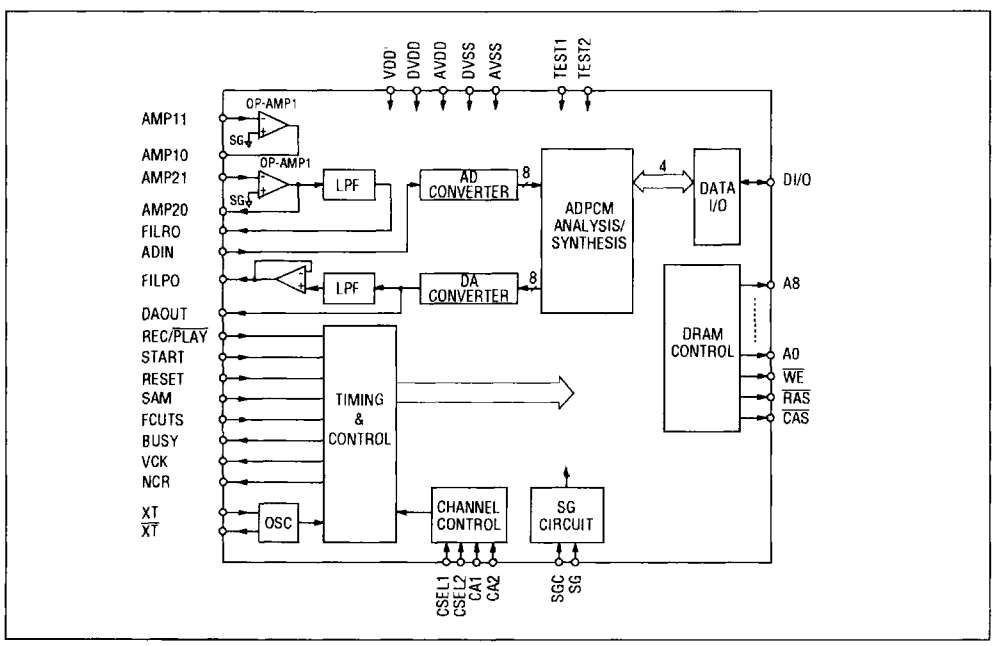
FEATURES

- 4-bit ADPCM technology
- Built-in 8-bit AD converter
- Built-in 8-bit DA converter
- Built-in microphone pre-amplifier
- Built-in low-pass filter
- One 256K-bit DRAM (MSM41256A) can be directly driven
  Attached with $\overline{CAS}$ before RAS refresh
- Sampling frequencies:
  4.0 and 8.0 kHz (when the oscillator operates at 4.096 MHz)
- Oscillator frequencies:
  4 to 6 MHz
- Number of words to be recorded:
  One, two, or four words can be selected
- Maximum recording time:
  16 sec (when the sampling frequency is 4 kHz)
- Power supply voltage:
  5V only
- 44-pin plastic QFP
  (QFP44-P-910-K)
- 44-pin V1 plastic QFP
  (QFP44-P-910-V1K)

PIN LAYOUT



CIRCUIT DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	T_a = 25°C	−0.3 ~ 7.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ V_{DD} +0.3	V
Storage temperature range	T_{stg}	–	−55 ~ + 150	°C

OPERATING RANGE

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	DVSS = AVSS = 0V	+4.0 ~ +6.0	V
Operating temperature range	T_{OP}	–	−40 ~ +85	°C
Oscillator frequency	f_{OSC}	–	4.0 ~ 6.0	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.5~5.5V DVSS = AVSS = 0V Ta = −40~ +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Input Voltage (Note 1)	V_{IH1}	–	3.6	–	–	V
High Input Voltage (Note 2)	V_{IH2}	–	0.8 x V_{DD}	–	–	V
Low Input Voltage	V_{IL}	–	–	–	0.8	V
High Output Voltage	V_{OH}	I_{OH} = −40μA	4.2	–	–	V
Low Output Voltage	V_{OL}	I_{OL} = 2mA	–	–	0.45	V
High Input Current (Note 3)	I_{IH1}	V_{IH} = V_{DD}	1	–	100	μA
High Input Current	I_{IH2}	V_{IL} = V_{DD}	–	–	10	μA
Low Input Current	I_{IL}	V_{IL} = V_{SS}	−10	–	–	μA
Operating Current (1)	I_{DD}	f_{OSC} = 4.0MHz Under no load and without signals	–	4	8	mA
Operating Current (2)	I_{PD}	f_{OSC} = 4.0MHz, RESET = "H"	–	0.5	1	mA

Note 1: Applies to the input pins excluding pin XT.
Note 2: Applies to pin XT.
Note 3: Applies to pin START.

ANALOG CHARACTERISTICS

AD converter, DA converter, operational amplifier 1, and operational amplifier 2

V_{DD}=4.5~5.5V DVSS=AVSS=0V Ta=−40~+85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Relative DA output precision	$\lvert V_{DAE} \rvert$	No load	–	–	60	mV
DA output impedance	R_{DA}	–	–	10	–	kΩ
Relative AD conversion precision	$\lvert V_{ADE} \rvert$	–	–	–	60	mV
AD conversion relative precision in 1/2 VDD point	$\lvert V_{ADE2} \rvert$	–	–	–	150	mV
ADIN input voltage	V_{AD}	–	0	–	AVDD	V
Amplifier open loop gain	G_{OP}	–	–	–	40	dB
Amplifier input impedance	R_{INA}	–	–	100	–	MΩ
Amplifier load resistance	R_{OUTA}	–	200	–	–	kΩ
Allowable amplifier input voltage range	V_{INA}	–	–	–	0.7 x V_{DD}	V_{P-P}
Amplifier output amplitude voltage range	V_{OUTA}	–	–	–	0.7 x V_{DD}	V_{P-P}
Low-pass filter input impedance	R_{IN}	–	–	30	–	MΩ
Low-pass filter load resistance	R_{OUT}	FILPO pin	50	–	–	kΩ
Optimum low-pass filter input voltage range	V_{IN}	–	–	0.6 x V_{DD}	–	V_{P-P}

AC ELECTRICAL CHARACTERISTICS

f_{OSC} = 4.096MHz, f_{SAMP} = 8.0kHz
V_{DD} = 4.5~5.5V DVSS = AVSS = 0V −40~+85°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse width	t_{STP}	2	–	–	µS
Time beginning when REC/$\overline{PLAY}$ is switched and ending when START is input	t_{RSS}	0	–	–	µS
Hold time beginning when BUSY goes low and ending when REC/$\overline{PLAY}$ is switched	t_{BRH}	35	–	–	mS
Time beginning when START is input and ending when BUSY goes high *	t_{SBR}	20	–	30	mS
Time beginning when BUSY gies high and ending when NCR goes low *	t_{BNF}	–	188	–	µS
Width while NCR is kept low *	t_{NCW}	–	188	–	µS
Setup time of CA1 or CA2 for the NCR falling edge	t_{CAS}	2	–	–	µS
Hold time of CA1 or CA2 for the NCR falling edge	t_{CAH}	2	–	–	µS
Setup time of CSEL1 or CSEL2 for the NCR falling edge	t_{CSS}	2	–	–	µS
Hold time of CSEL1 or CSEL2 for the BUSY falling edge	t_{CSH}	0	–	–	µS
Time beginning when BUSY goes high and ending when recording starts *	t_{BA}	–	250	–	mS
Time beginning when START goes low and ending when recording ends *	t_{SAR}	30	–	200	µS
Time beginning when recording ends and ending when BUSY GOES LOW *	t_{AB}	–	500	–	µS
Time beginning when BUSY goes high and ending when playback starts *	t_{BS}	–	500	–	µS
Time beginning when playback completes and ending when BUSY goes low *	t_{SB}	–	313	–	µS
Hold time of START for the NCR falling edge during repetitive playback *	t_{STH}	0	–	–	µS
Time beginning when playback of the previous word completes and ending when NCR goes low during repetitive playback *	t_{MNF}	–	250	–	µS
Time during which no sound is heard between a word and the next work during repetitive playback *	t_{MS}	–	563	–	µS
Time during which VCK is kept high *	t_{VH}	–	62.5	–	µS
Time during whick VCK is kept low *	t_{VL}	–	62.5	–	µS

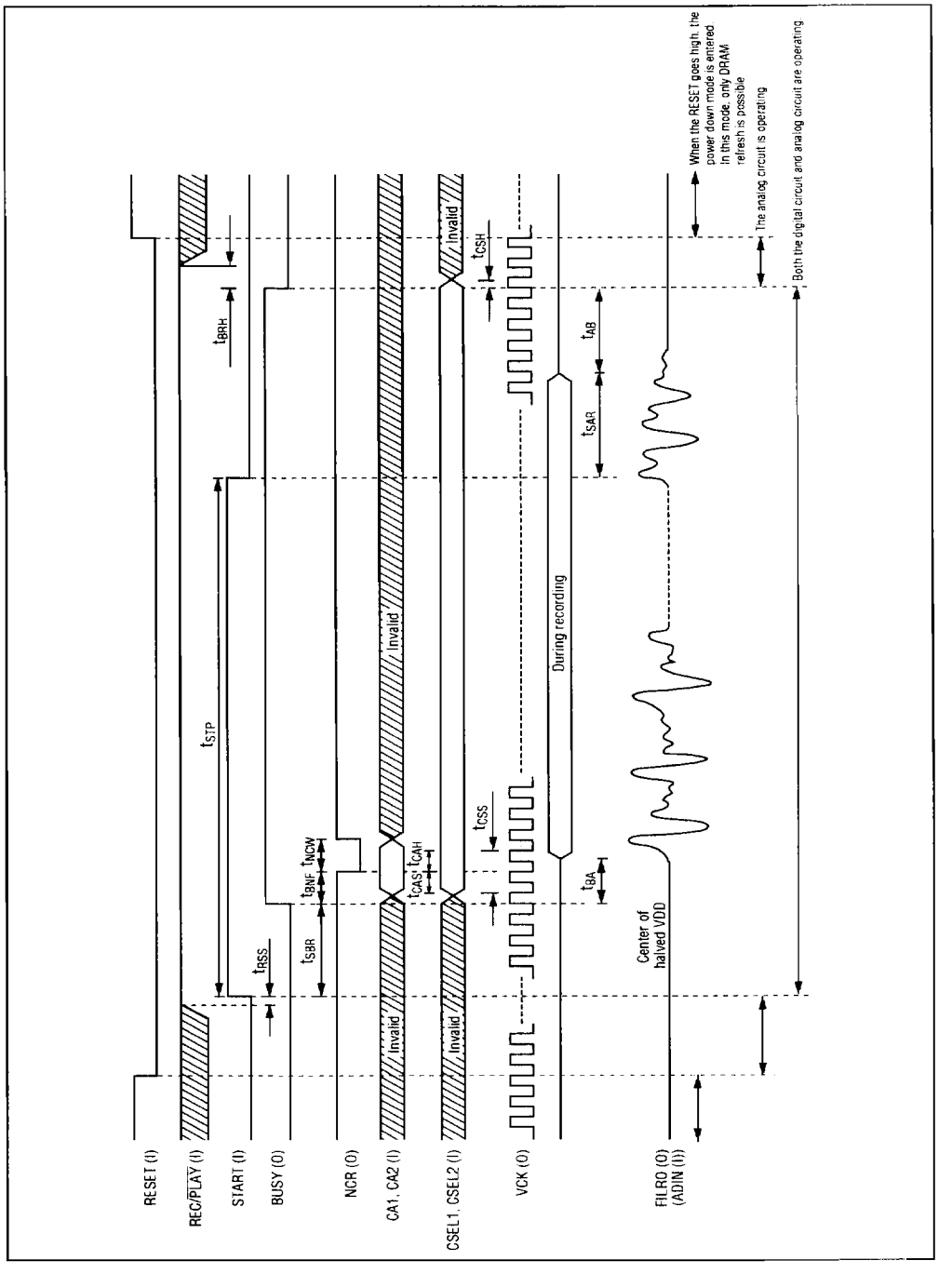
AC ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Time beginning when VCK goes high and ending when RAS goes low	t_{VRF}	–	3.9	–	µS
$\overline{RAS}$ pulse width	t_{RAS}	–	9.8	–	µS
Time begginning when VCK goes high and ending when CAS goes low	t_{VCF}	–	5.9	–	µS
$\overline{CAS}$ pulse width	t_{CAS}	–	1.0	–	µS
$\overline{CAS}$ precharge time	t_{CP}	–	1.0	–	µS
Refresh pulse cycle of $\overline{RAS}$ or $\overline{CAS}$ during DRAM refreshing	t_{RFW}	–	7.8	–	µS
$\overline{RAS}$ pulse width during DRAM refresh	t_{RRW}	–	0.5	–	µS
$\overline{CAS}$ pulse width during DRAM refresh	t_{RCW}	–	1.0	–	µS
Time beginning when VCK goes high and ending when the address pin changes from a row address to a column address	t_{RC}	–	4.9	–	µS
Time beginning when the VCK goes high and ending when the address pin changes from a column address to a row address	t_{CR}	–	36.1	–	µS
Time beginning when VCK goes high and ending with the address is incremented by one	t_{RCU}	–	58.6	–	µS

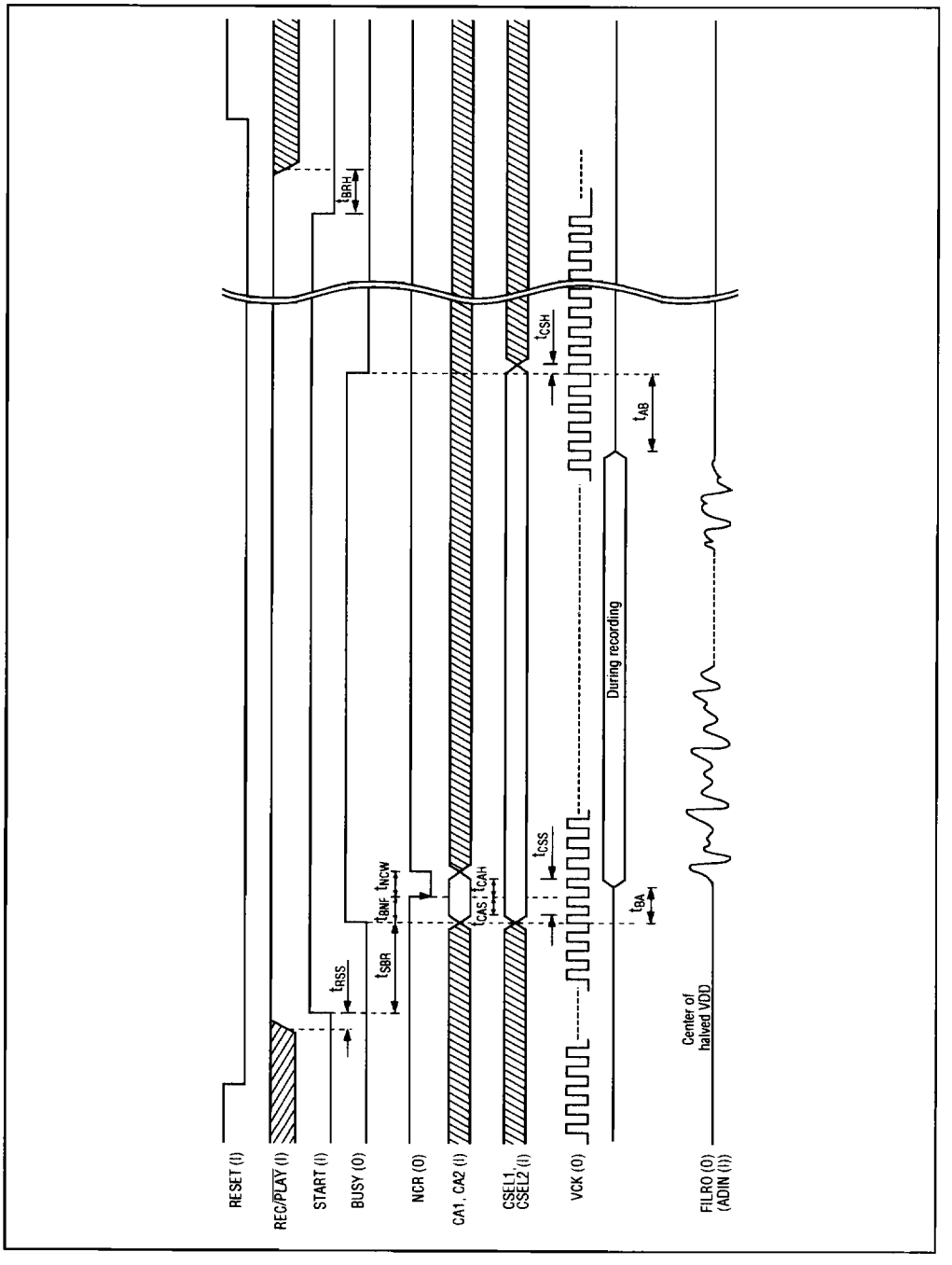
*: When the sampling frequency is 4kHz, the time is doubled.

1. RECORDING

1-1 When the recording preces is stopped before the capacity of the channel is exhausted

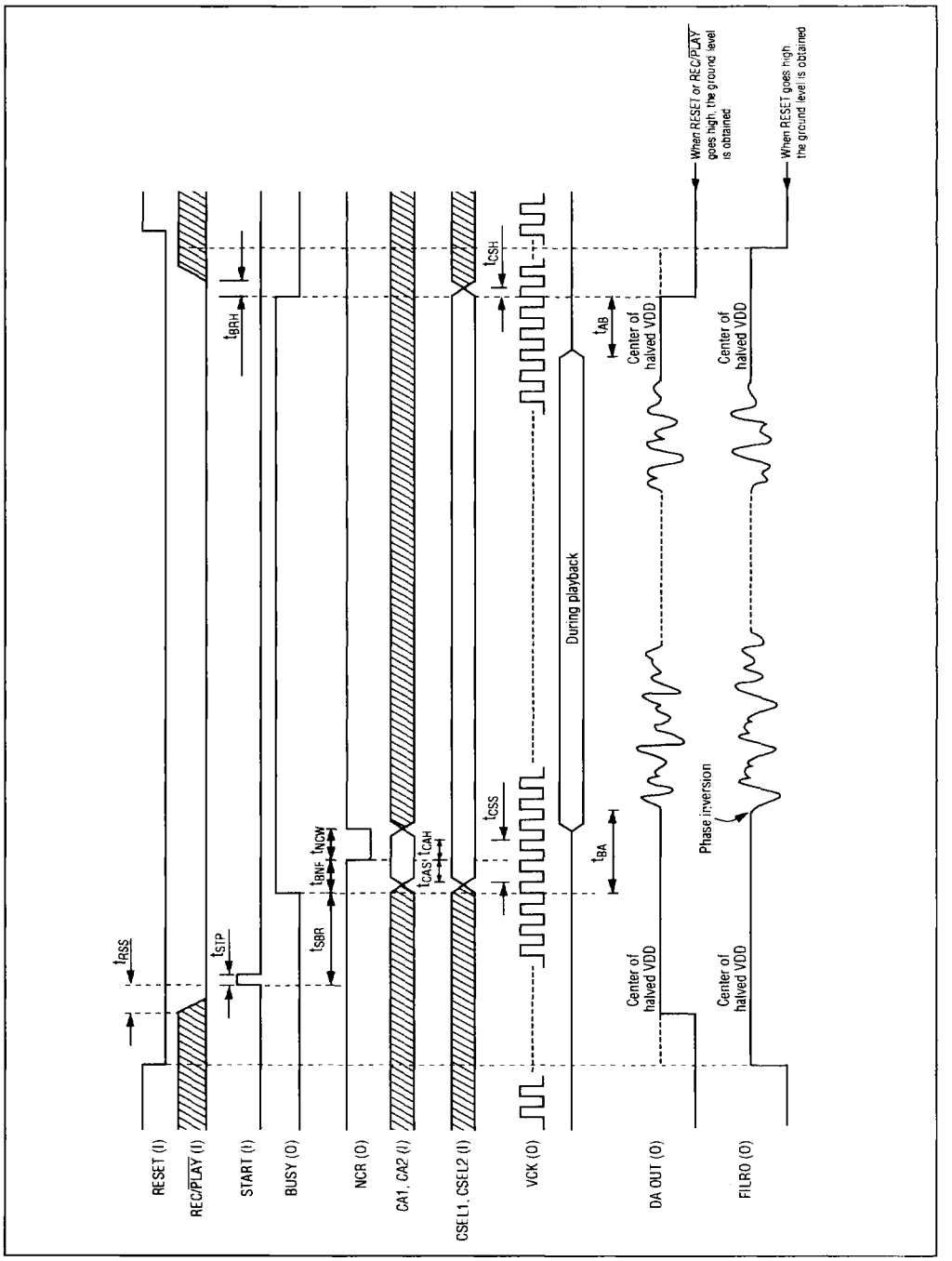


1-2 When recording process is continued until the capacity of the channel is exhausted

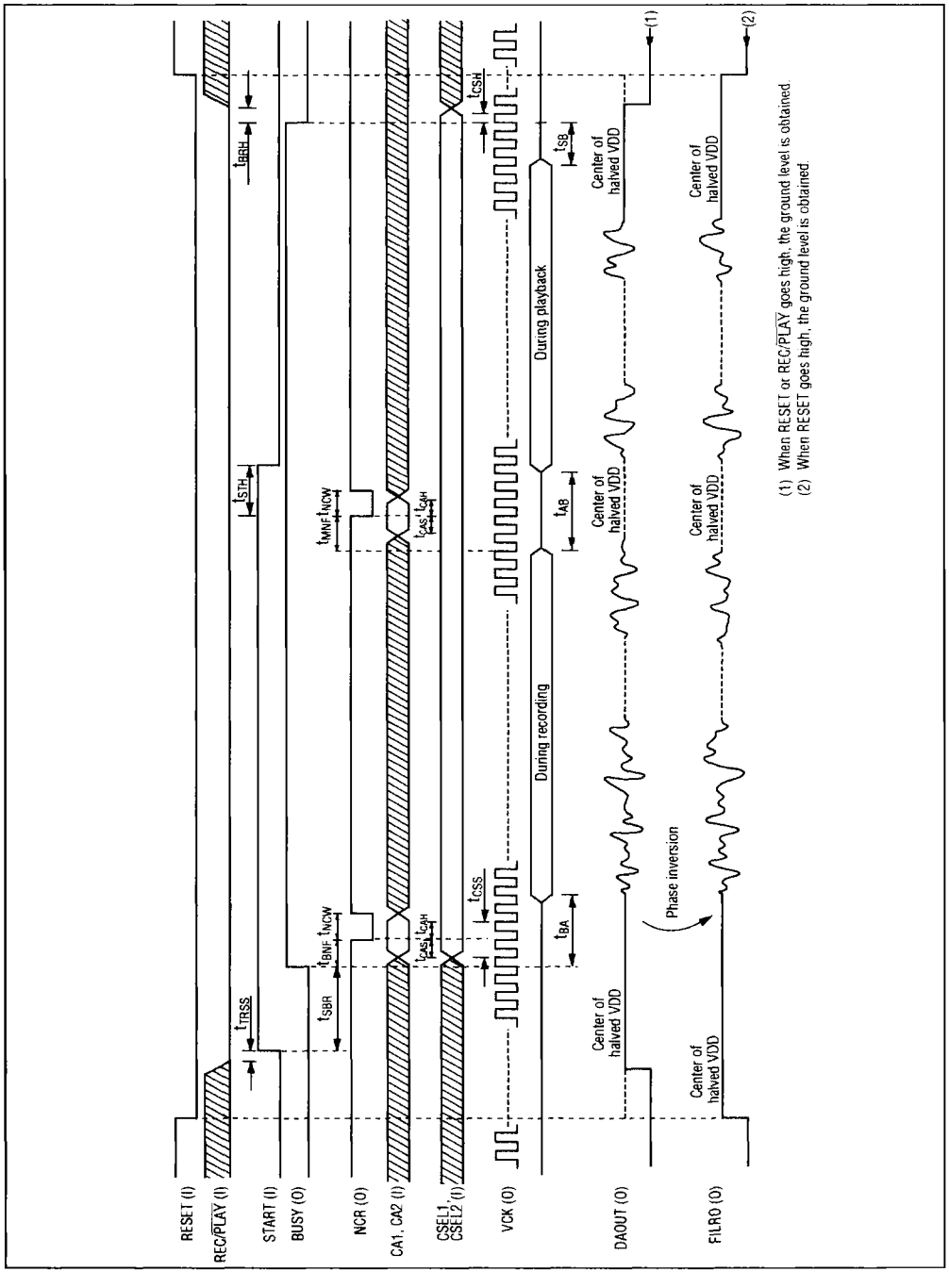


2. PLAYBACK

2-1 When playback is performed only once

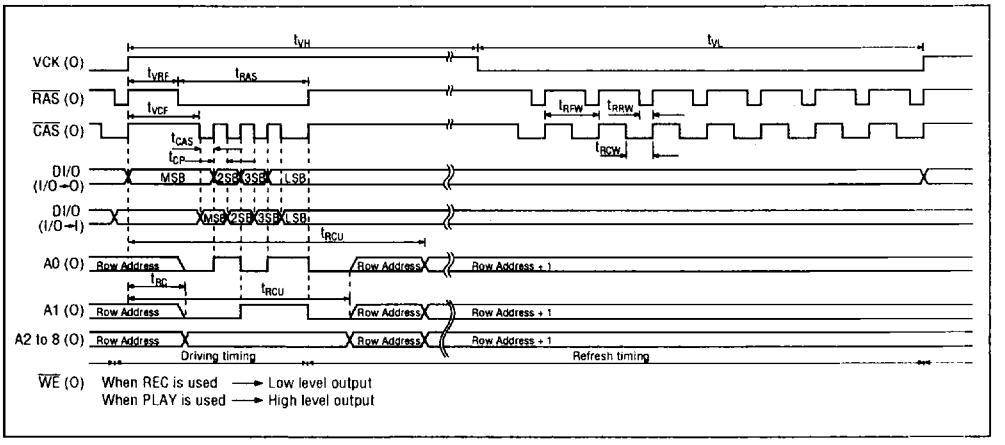


2-2 When playback is performed repeatedly

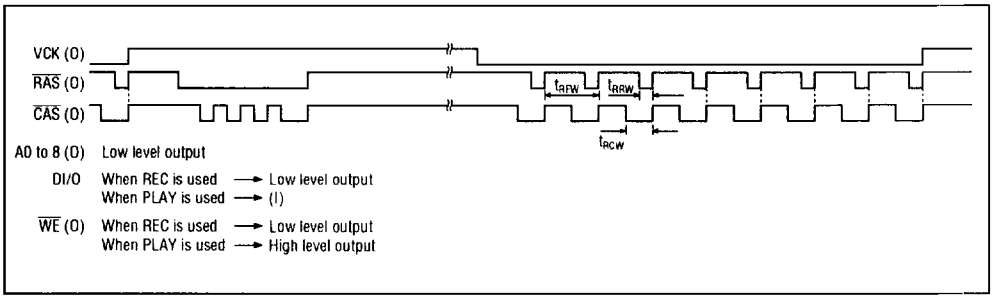


3. DRAM DRIVING TIMING CHARTS

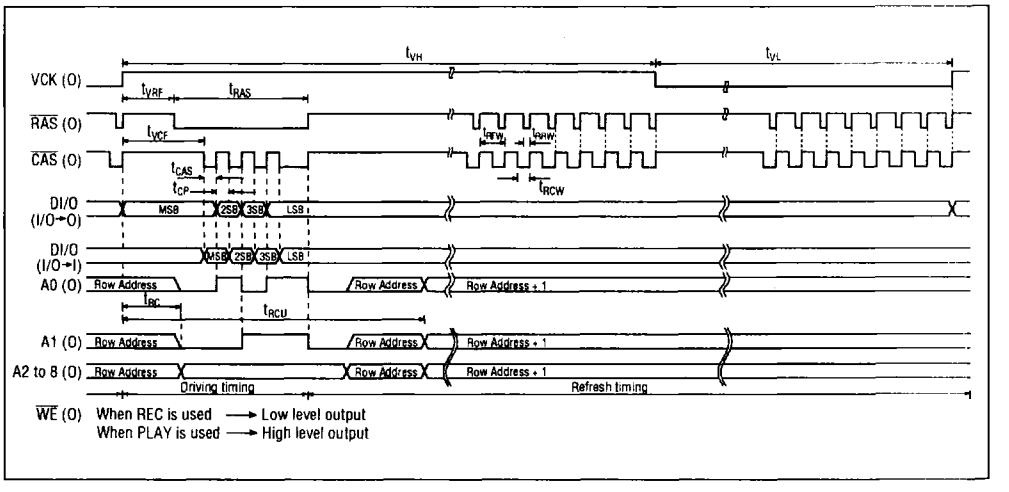
3-1 Timing chart to drive DRAM during recording or playback (SAM=High level)



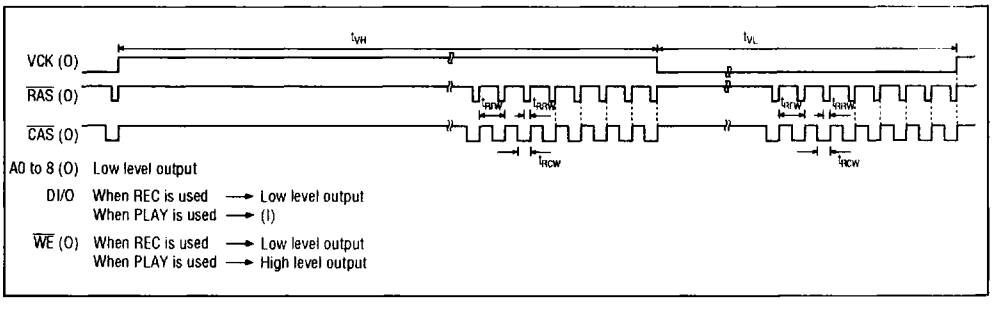
3-2 Timing chart to drive DRAM during standby or power down (SAM=High level)



3-3 Timing chart to drive DRAM during recording or playback (SAM=Low level)



3-4 Timing chart to drive DRAM during standby or power down (SAM=Low level)



PIN DEFINITION

Pin name	I/O	Function
DVDD	I	Digital power supply pin
AVDD	I	Analog power supply pin
VDD'	I	Power supply pin
DVSS	I	Digital ground pin
AVSS	I	Analog ground pin
SG	O	Signal ground (SG) pin. Its output is at the halved VDD level. A capacitors is connected to stabilize the output.
SGC	O	A capacitors is connected for SG stabilization.
AMP1I	I	Inverted input pin of operational amplifier 1. The non-inverted input pins are connected to the signal ground (SG) in the inside.
AMP1O	O	Output pin of operational amplifier 1.
AMP2I	I	Inverted input pin of operational amplifier 2. The non-inverted input pins are connected to the signal ground (SG) in the inside.
AMP2O	O	Output pin of operational amplifier 2. It is connected to the built-in low-pass filter.
ADIN	I	Input pin of the AD converter
DAOUT	O	Output pin of the DA converter. It is connected to the built-in low-pass filter.
FILPO	O	Output reproduced waveforms that passed through the low-pass filter during playback.
FILRO	O	Outputs waveforms to be recorded that passed through the low-pass filter. Connect this pin to ADIN.
RESET	I	When this pin goes high, the power down mode is entered.
REC/$\overline{\text{PLAY}}$	I	Selects either the recording mode or the playback mode. When this pin is high, the recording mode is entered.
START	I	When this pin goes high, recording or playback starts.
BUSY	O	Kept at the high level during recording or playback.
CSEL1	I	Selects the number of words to be registered together with CSEL2.
CSEL2	I	Selects the number of words to be registered together with CSEL1.
CA1	I	Specifies a channel when the number of words to be registered is set at 2 or 4.
CA2	I	Specifies a channel when the number of words to be registered is set at 4.
SAM	I	Selects a sampling frequency.
DI/O	I/O	Inputs or outputs 4-bit ADPCM data. This pin is connected to DRAM I/O.
A0~A8	O	Address output pins for 256K-bit DRAM
$\overline{\text{RAS}}$	O	DRAM control output pin
$\overline{\text{CAS}}$	O	DRAM control output pin

PIN DEFINITION (Continued)

Pin name	I/O	Function
$\overline{WE}$	O	DRAM control output pin
XT	I	Input pin connected to an oscillator. External clocks are input through this pin.
$\overline{XT}$	O	Output pin connected to an oscillator. When using external clocks, place this pin in the open state.
VCK	O	Outputs the selected sampling frequency.
NCR	O	Outputs pulses when recording or multi-channel playback starts.
FCUTS	I	Selects a cutoff frequency of the low-pass filter.
TEST1	I	Test pin. Be sure to keep this pin at the low level.
TEST2	I	Be sure to keep this pin at the low level.

EXPLANATION OF FUNCTIONS

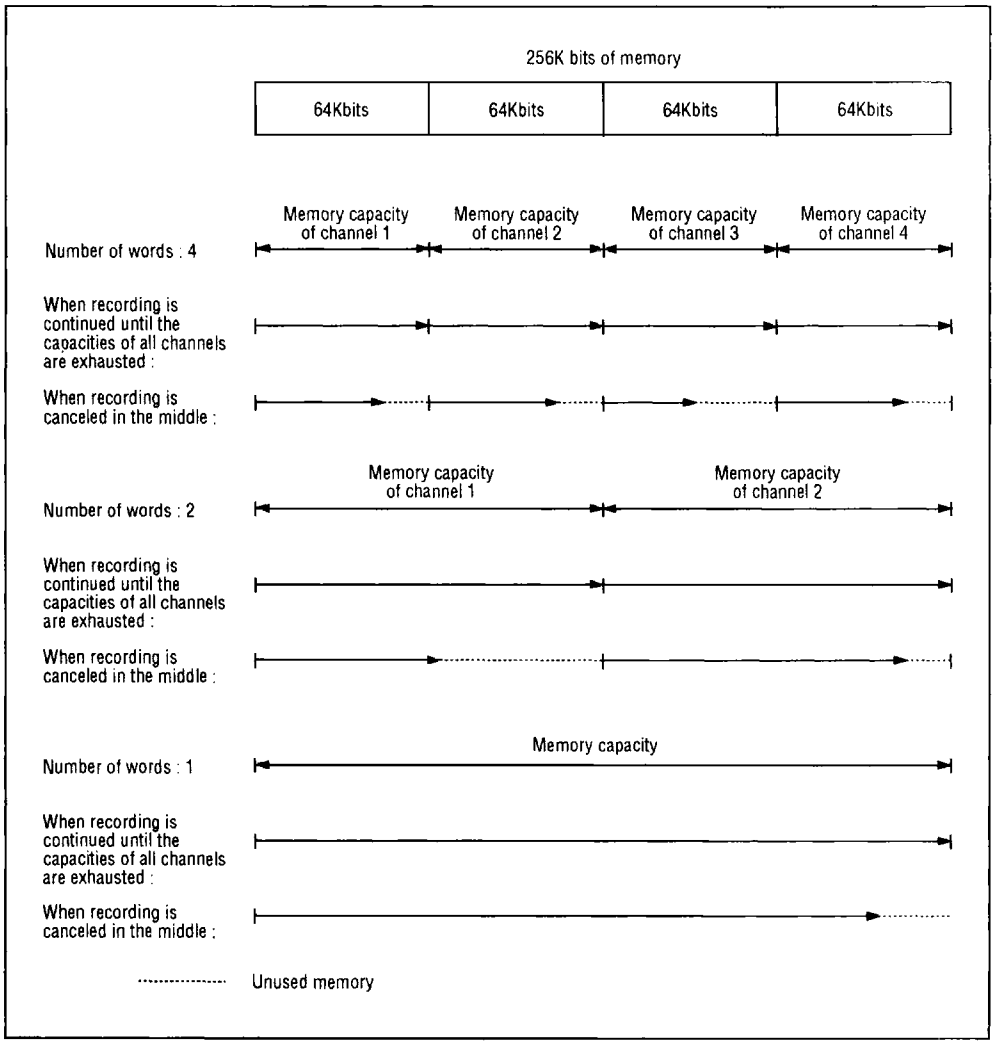
- **Selection of the Number of Words to be Recorded and Specification of a Channel (CSEL1, CSEL2, CA1, and CA2)**

Use the CSEL1 and CSEL2 input pins to select 1, 2, or 4 as the number of words to be recorded. When 1 is selected, up to 256K bits are assigned as the memory capacity. When 2 is selected, up to 128K bits are assigned to each channel as the memory capacity. When 4 is selected, up to 128K bits are assigned to each channel as the memory capacity. When 4 is selected, up to 64K bits are assigned to each channel. It is possible to record in each channel until that channel's memory allocation is exhausted. Channels can be specified for the assigned memory capacities by the CA1 and CA2 input pins.

The following table shows the relationship between the number of words and channels.

CSEL2	CSEL1	Number of words	CA1	CA2	Channel	Channel Capacity
L	–	4 words	L	L	CH1	64Kbits are assigned to each channel
			L	H	CH2	
			H	L	CH3	
			H	H	CH4	
H	L	2 words	L	–	CH1	128Kbits are assigned to each channel
			H	–	CH2	
H	H	1 word	–	–	CH1	256Kbits

Use of memory is explained below for each specified channel.



- **Selection of a Sampling Frequency (SAM)**

The relationships between the frequency of the oscillator (f_{OSC}) and the sampling frequency (f_{SAMP}) are as follows:

SAM	L	H
f_{SAMP}	f_{OSC}/1024(4kHz)	f_{OSC}/512(8kHz)

( ): The numbers in parentheses are true when the oscillator frequency is 4096 kHz.

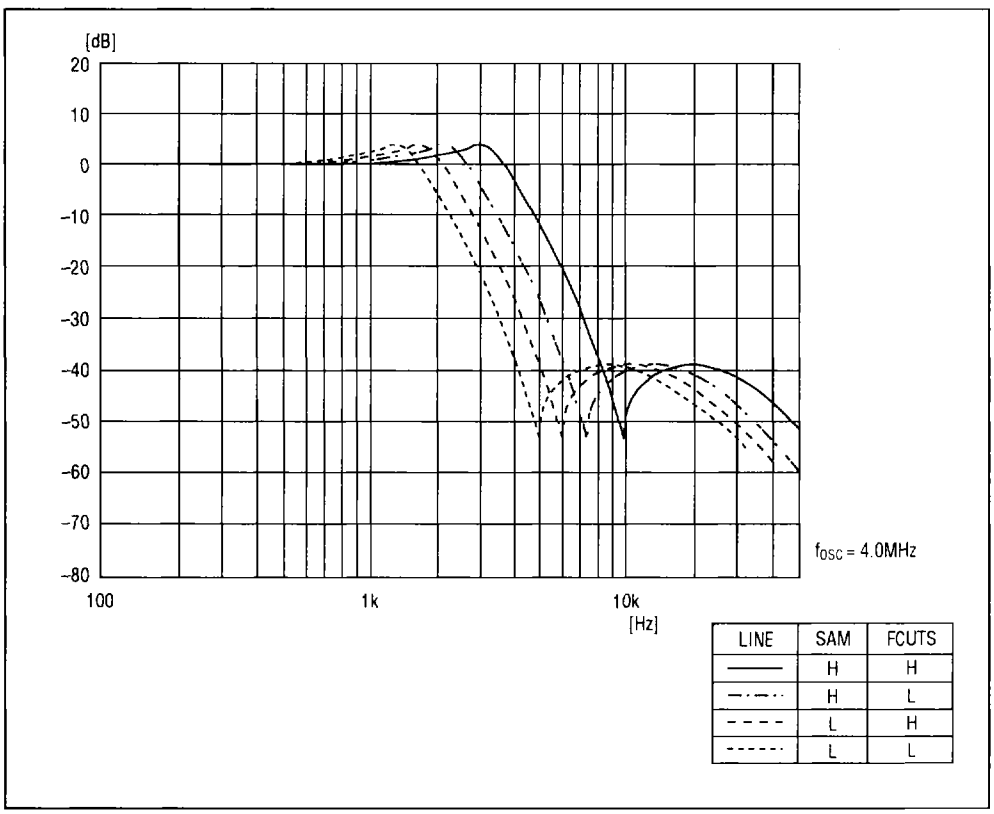
- **Selection of a Cutoff Frequency used by the Low-pass Filter(FCUTS)**

Use the FCUTS pin to select a cutoff frequency used by the low-pass filter as follows (the cutoff frequency is proportional to the oscillator frequency.)

Sampling Frequency		FCUTS	
SAM	f_{SAMP}	H	L
L	4kHz	2.3kHz	1.8kHz
H	8kHz	3.7kHz	2.8kHz

The oscillator frequency is 4096 kHz.

LOW-PASS FILTER FREQUENCY CHARACTERISTICS



- **Recording and Playback**

1. Recording

Set the REC/$\overline{\text{PLAY}}$ pin to a logic "1". Then select the number of words with the CSEL1 and CSEL2 pins and select a channel with the CA1 and CA2 pins.

To start recording, set the START pin high.

Recording is continued as long as the START pin is kept high. During recording, the BUSY output pin is at a "1". (See Figure 1.)

When the capacity of the specified channel is exhausted, recording stops. At the same time, the BUSY pin goes low ("0"). (See Figure 2.)

2. Playback

Set the REC/$\overline{\text{PLAY}}$ pin to a logical "0". Then select the number of words with the CSEL1 and CSEL2 pins and select a channel with the CA1 and CA2 pins.

To start playback, set the START pin high. Playback is continued for the time during which recording has been made. During playback, the BUSY output pin is high (See Figure 3.)

Repetitive playback is possible as long as the START input pin is kept high. For repetitive playback (by switching channels), see the explanation of the next channel request (NCR) function. During repetitive playback, the BUSY output pin is high as in the playback mode described above. (See Figure 4.)

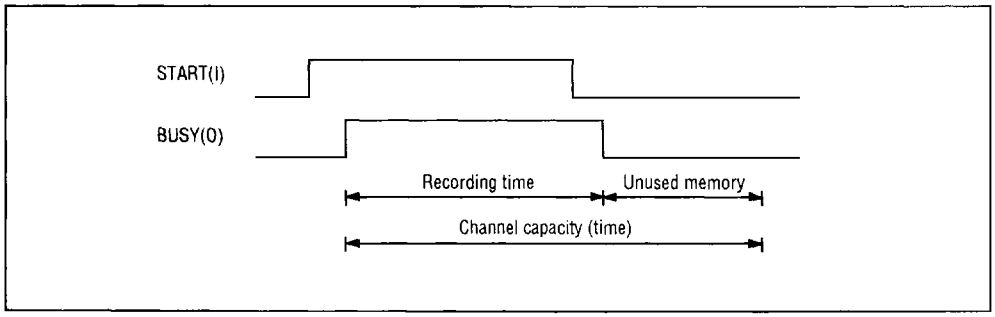


Figure 1 Timing Chart When Recording is Stopped in the Middle

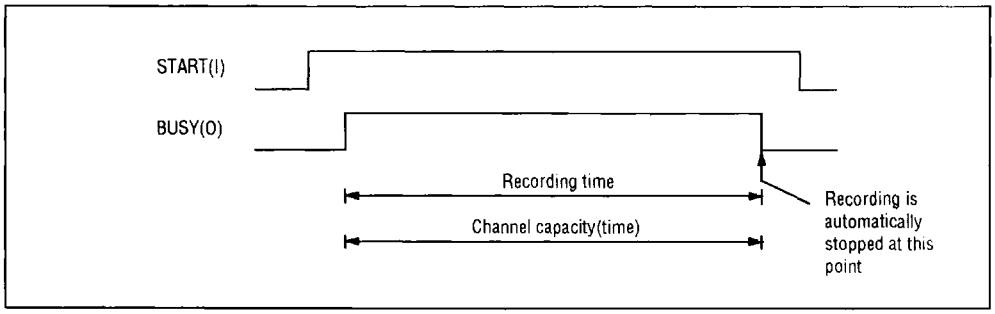


Figure 2 Timing Chart When Recording is Continued Up to the End of the Channel Capacity

Note: Since all bits of the stop bit are not controlled in the LSI, the recording time is extended up to 128 msec at a sampling frequency of 8 kHz. In addition, recording starts 20 to 30 msec after the START pin goes high.

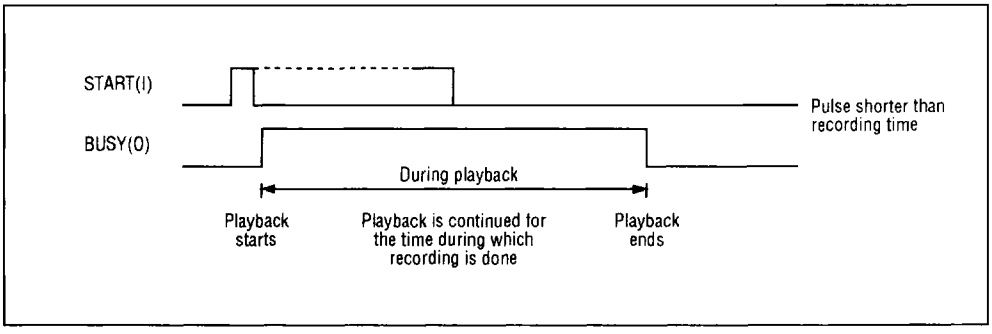


Figure 3 Timing Chart When Playback is Done Only Once

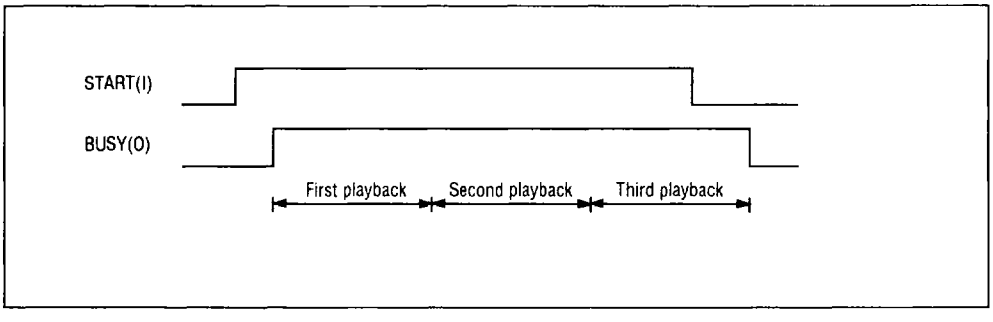


Figure 4 Timing Chart When Playback is Done Repeatedly

- **Next Channel Request (NCR) Functions**

The NCR pin output pulses as shown in the timing diagrams (Figures 7 and 8), when recording starts and playback starts for each word.

Repetitive playback is enabled as long as the START pin is kept high. When the NCR pin outputs a pulse, playback starts for a specified channel.

In the repetitive playback mode, the contents of each channels are stored in LSI on the falling edge of a pulse output from the NCR pin. When channels are switched by the CA1 and CA2 pins before the rising edge of a pulse from the NCR pin, therefore, the contents of multiple channels are played back continuously. (See Figure 9.)

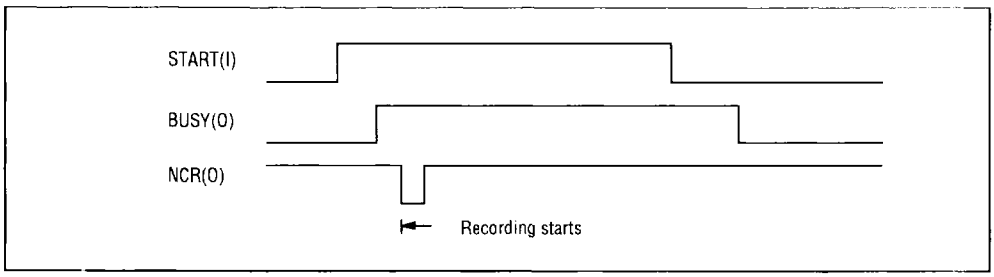


Figure 7 NCR Pin Output during Recording

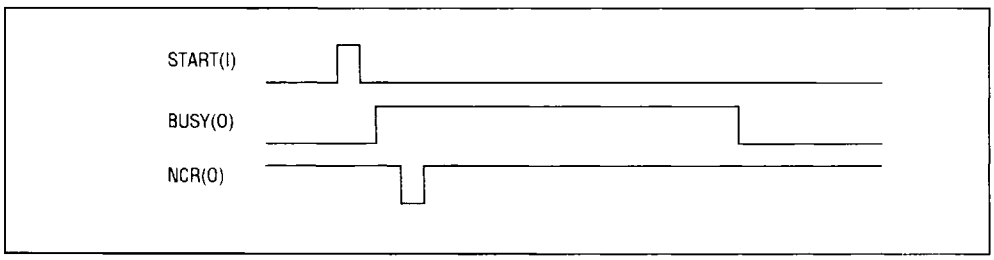


Figure 8 NCR Pin Output during Playback

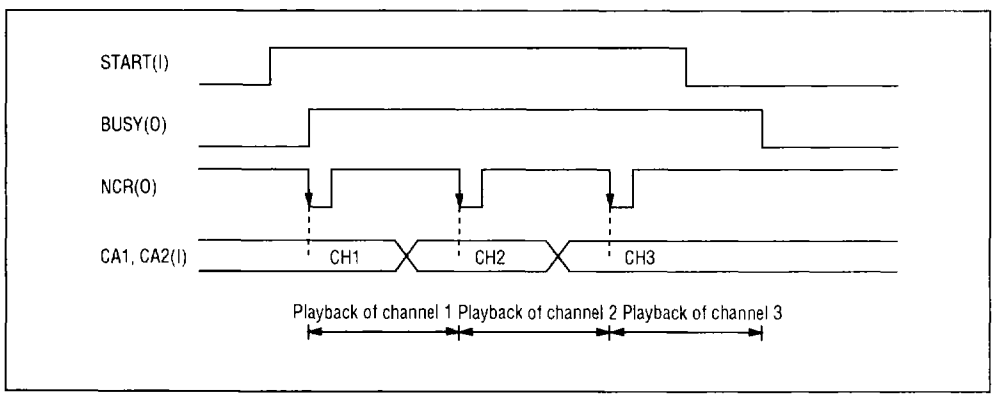


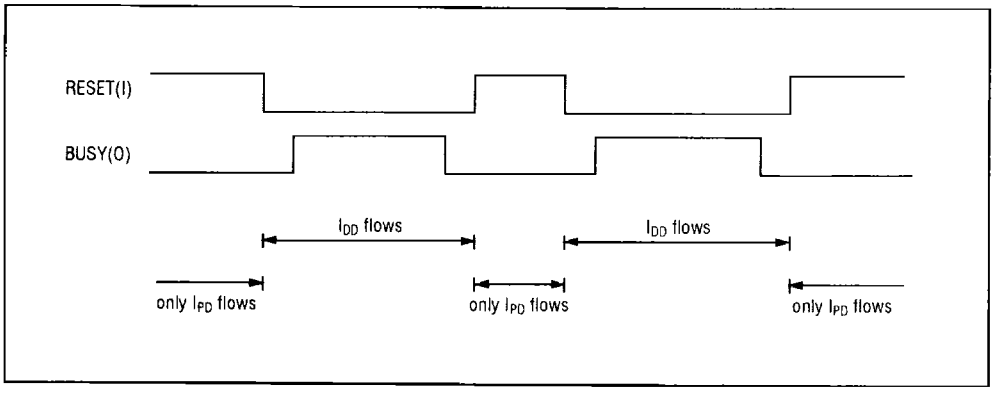
Figure 9 Relationships between CA1 and CA2 Pin Pulses and NCR Pin Pulse during Continuous Channel Playback

- **Power Down Function (RESET)**

This LSI goes, power-down when the RESET pin is set high. In addition to recording time and playback time, the analog circuit is operating while the RESET pin is low.

Status of LSI at power down
(The RESET pin is at the high level.)

- The analog circuit stops.
- Of the logic circuits, only the RAM refresh circuit is operating.
- The recorded contents are retained.



It may take 100 msec after the RESET pin goes low before the analog circuit operates.

(This time varies depending on the capacitance of the external capacitor of the SG or SGC.)

- **Analog Circuit**

1. Analog Input

This LSI incorporates two operational amplifiers for microphone output amplification. Each amplifier has an inverted input pin and an output pin. Non-inverted input is connected to the signal ground (SG) in the LSI.

For amplification to a speaker, the MSM6308GS requires an external amplifier. This amp is easily constructed from an operational amplifier configured as an inverting amp. The gain is adjusted with resistors in the op-amp's feedback loop. The relationship of these resistors to the amplification factors can represented by the following expressions:

C1 and C2 in Figure 10 are coupling capacitors.

If using the Oki AMP20, adjust gain of the amplifier so that the output of the AMP20 pin is about 0.6 x VDD (Vpp) due to the restrictions of input to the low-pass filter.

Connect the FILRO pin directly to the ADIN input pin of the A/D converter.

2. Analog Output

The output from the D/A converter is sent to the low-pass filter in the LSI. At the same time, the output is sent to the DAOUT pin.

Connect the amplifier for the speaker drive to the FILOP output pin of the low-pass filter.

The maximum output amplitude of the D/A converter is 255/256 x VDD. The D/A converter outputs stair step waveforms in synchronization with the sampling frequency. To suppress noise, insert a capacitor between the DAOUT pin and the analog ground pin.

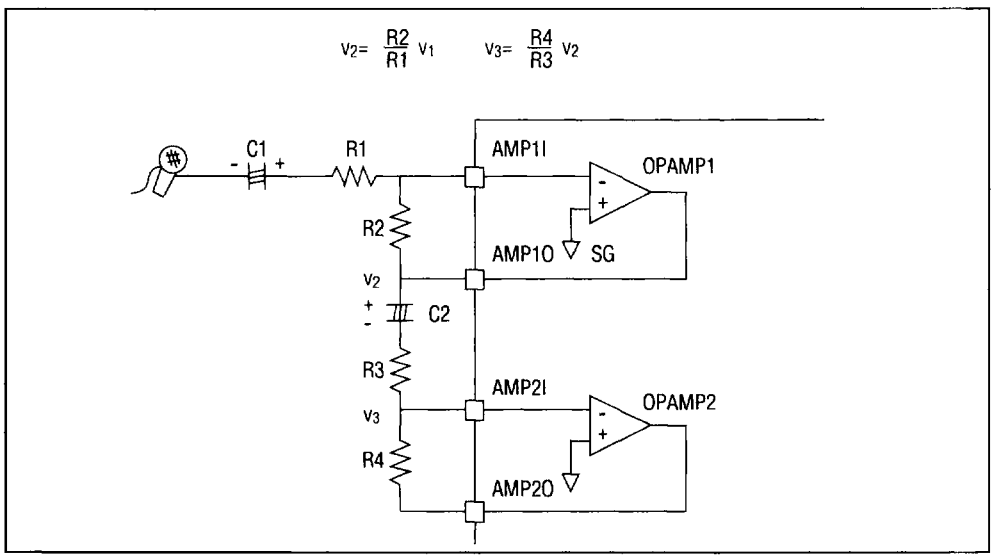


Figure 10 Analog Input Circuit and External Circuit

- **How to Connect the Oscillator**

Figure 11 shows how to connect the oscillator.

For reference, the ceramic resonator manufactured by Murata Seisakusho for connecting the $\overline{XT}$ and XT terminals is shown below.

Ceramic resonator		Optimum load capacity value	
Model Name	Frequency(MHz)	C_1(PF)	C_2(PF)
CSA4.00MG	4.00	30	30
CSA4.09MG	4.09	30	30
CSA5.00MG	5.00	30	30
CSA6.00MG	6.00	30	30

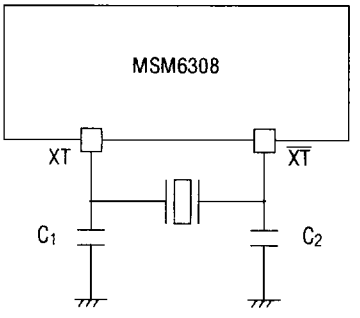


Figure 11 Oscillator Connection

EXAMPLE OF MSM6308 APPLICATION CIRCUIT

An example of the application circuit for using MSM6308 and 256K DRAM is shown in the figure below.

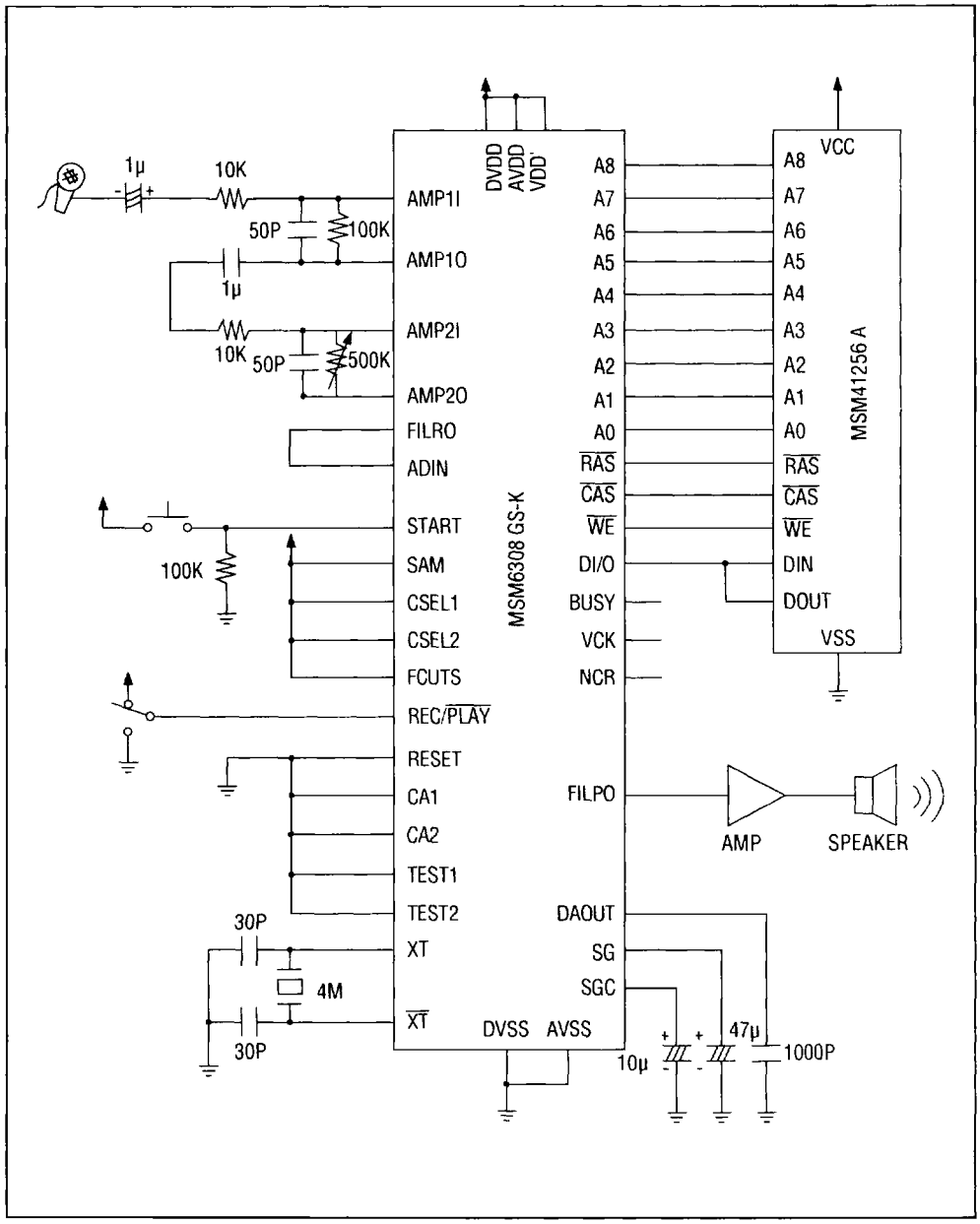


Figure 12 Example of Application Circuit with 256K DRAM