GD4015B
DUAL 4-BIT STATIC SHIFT REGISTER

DESCRIPTION – The 4015B is a Dual Edge-Triggered 4-Bit Static Shift Register (Serial-to-Parallel Converter). Each Shift Register has a Serial Data Input (D), a Clock Input (CP), four fully buffered parallel Outputs (Q_0–Q_3) and an overriding asynchronous Master Reset Input (MR).

Information present on the serial Data Input (D) is shifted into the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

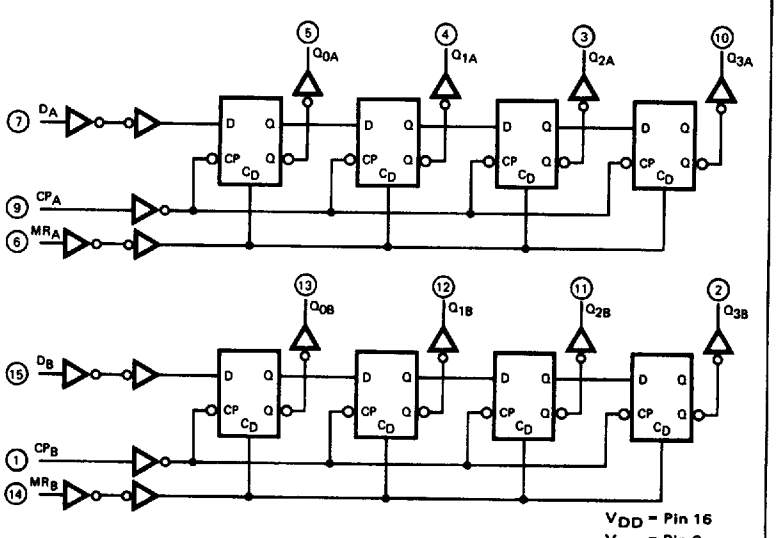
A HIGH on the Master Reset Input (MR) clears the register and forces the Outputs (Q_0 - Q_3) LOW, independent of the Clock and Data Inputs (CP and D).

- **TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **SERIAL-TO-PARALLEL DATA TRANSFER**
- **FULLY BUFFERED OUTPUTS FROM EACH STAGE**

PIN NAMES

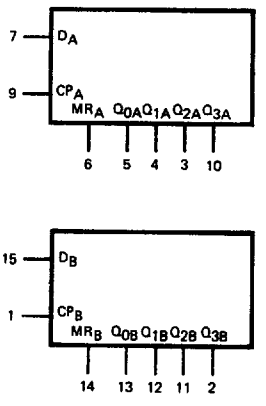
D_A, D_B	Serial Data Input
MR_A, MR_B	Master Reset Input (Active HIGH)
CP_A, CP_B	Clock Input (L→H Edge-Triggered)
Q_{0A}, Q_{1A}, Q_{2A}, Q_{3A}	Parallel Outputs
Q_{0B}, Q_{1B}, Q_{2B}, Q_{3B}	Parallel Outputs

LOGIC DIAGRAM

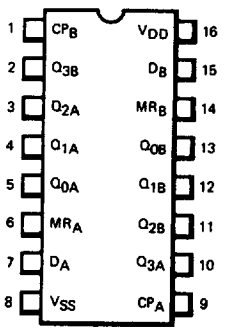


LOGIC SYMBOL

4015B



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

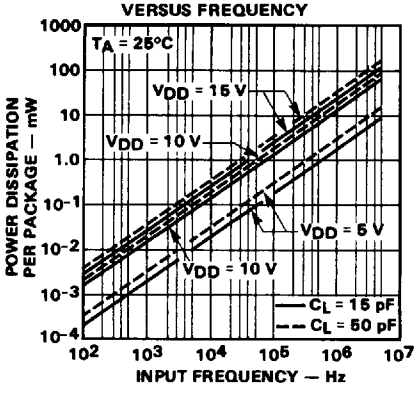
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q		165	300		85	150		50	120	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			165	300		85	150		50	120	ns	
t_{PHL}	Propagation Delay, MR to Q		180	325		90	160		60	128	ns	
t_{TLH}	Output Transition Time		85	150		45	85		30	50	ns	
t_{THL}			85	150		45	85		30	50	ns	
t_s	Set-Up Time, D to CP	150	70		50	30		40	25		ns	
t_h	Hold Time, D to CP	0	–5		0	-20		0	-10		ns	
$t_{W}CP(L)$	Minimum Clock Pulse Width	120	60		70	35		56	25		ns	
$t_{W}MR(H)$	Minimum MR Pulse Width	75	40		45	25		36	20		ns	
t_{rec}	MR Recovery Time	300	160		120	60		96	45		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	4	8		7	14		8	16		MHz	

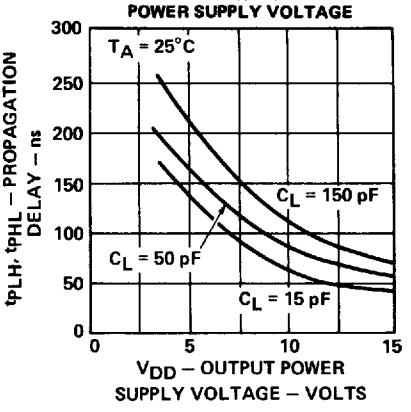
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

TYPICAL ELECTRICAL CHARACTERISTICS

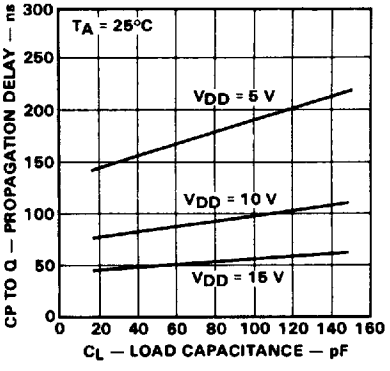
POWER DISSIPATION VERSUS FREQUENCY



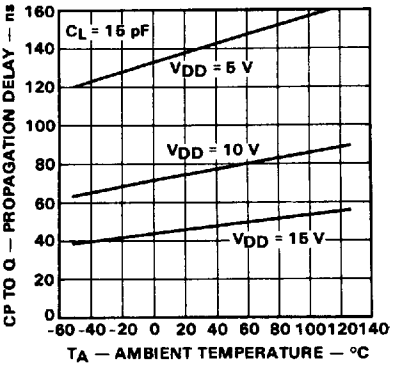
PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



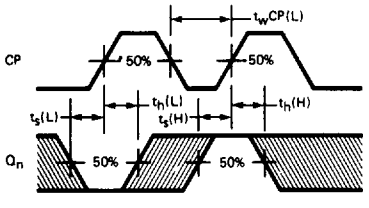
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



PROPAGATION DELAY VERSUS TEMPERATURE



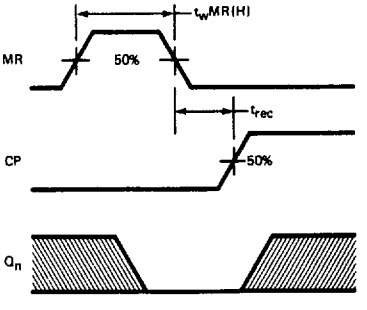
SWITCHING WAVEFORMS



SET-UP TIMES, HOLD TIMES AND MINIMUM CLOCK PULSE WIDTH

NOTE:

t_s and t_h are shown as positive values but may be specified as negative values.



RECOVERY TIME FOR MR AND MINIMUM MR PULSE WIDTH