NEC

TRANSISTOR ARRAY

UPA104B
UPA104G

FEATURES

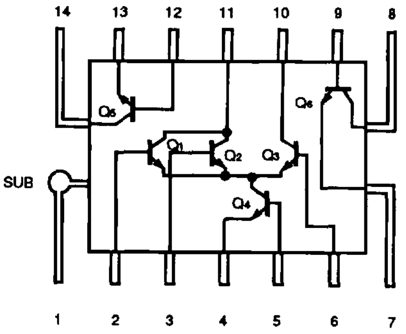
- 9 GHz CONFIGURABLE TRANSISTOR BASED OR/ NOR CIRCUITRY
- OUTSTANDING h_{FE} LINEARITY
- TWO PACKAGE OPTIONS:
  UPA104B: Superior thermal dissipation due to studded ceramic package
  UPA104G: Reduced circuit size due to 14-pin mini-flat package for surface mounting
- EXCELLENT FOR ANALOG ADDITIONS & FORMATION OF 2-INPUT OR/NOR GATES

DESCRIPTION

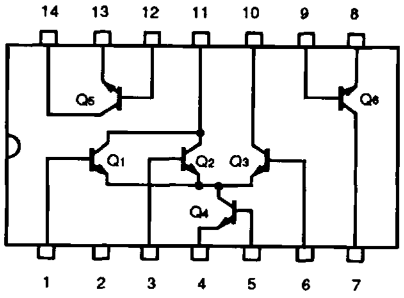
The UPA104 is a user configurable, Silicon bipolar transistor array for formation of high speed OR/NOR gates. Its internal transistor configuration and external connection options allow the user considerable flexibility in its application. Its high gain bandwidth product (f_T = 9 GHz) make it applicable for electro-optical, signal processing, cellular telephone systems, instrumentation, and high speed gigabit logic circuits.

CONNECTION DIAGRAM (Top View)

UPA104B



UPA104G



Note: Substrate should be connected to the lowest voltage point in order to prevent latch-up.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE			UPA104B, UPA104G BS14, G14		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{CBO}	Collector Cutoff Current at V_{CB} = 5 V, I_E = 0 (All Transistors)	µA			1.0
I_{EBO}	Emitter Cutoff Current at V_{EB} = 1 V, I_C = 0 (Q4, Q5, Q6)	µA			1.0
h_{FE}	Direct Current Amplification at V_{CE} = 3 V, I_C = 5 mA (Q4 and Q6)		40	100	250
C_{CB}	Collector to Base Capacitance at V_{CB} = 3 V, f = 1 MHz (Q3, Q5, Q6)	pF		0.9	1.8
C_{EB}	Emitter to Base Capacitance at V_{EB} = 0, f = 1 MHz (Q4, Q5, Q6)	pF		1.4	2.8
C_{CS}	Collector/Substrate Capacitance at V_{CS} = 3 V, f = 1 MHz (Q3, Q5, Q6)	pF		1.4	2.8
f_T[1]	Gain Bandwidth Product at V_{CE} = 3 V, I_C = 10 mA	GHz		9.0	
R_{TH}	Thermal Resistance, Single Transistor, G14 Package Whole Device, G14 Package	°C/W °C/W			40 25

Note:
1. Measured by installing a single transistor in a Micro-X package: the value shown is a reference value.

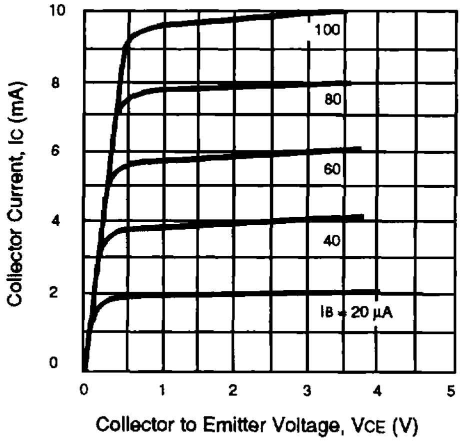
ABSOLUTE MAXIMUM RATINGS[1] (TA = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CBO}[2]	Collector to Base Voltage	V	15
V_{CEO}[2]	Collector to Emitter Voltage	V	6
V_{EBO}[2]	Emitter to Base Voltage	V	2.5
I_C[2]	Collector Current	mA	40
P_T	Total Power Dissipation UPA104B UPA104G	 mW mW	 650 350
T_J	Junction Temperature UPA104B UPA104G	 °C °C	 200 125
T_{STG}	Storage Temperature UPA104B UPA104G	 °C °C	 -55 to +200 -55 to +125

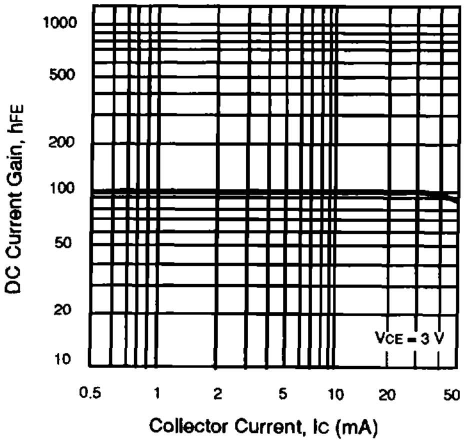
Notes:
1. Operation in excess of any one of these conditions may result in permanent damage.
2. Absolute maximum ratings for each transistor.

TYPICAL PERFORMANCE CURVES (TA = 25°C)

COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE

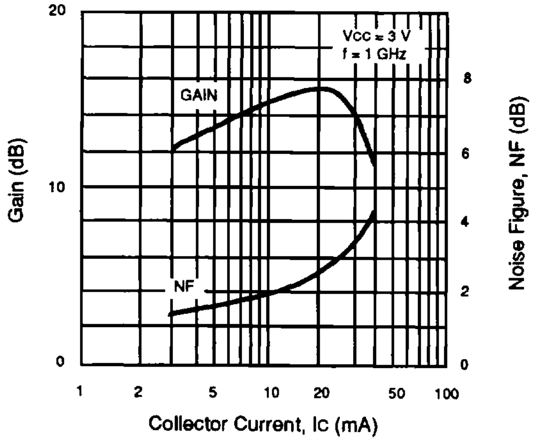


DC CURRENT GAIN vs. COLLECTOR CURRENT

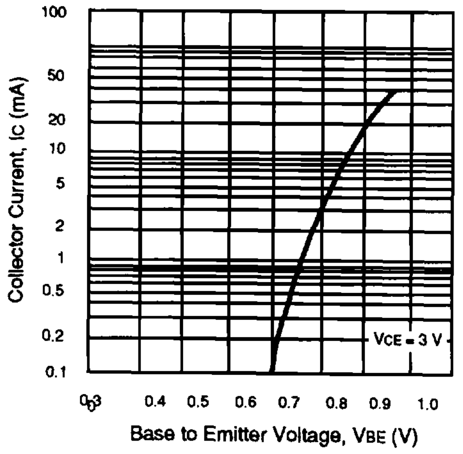


TYPICAL PERFORMANCE CURVES (TA = 25 °C)

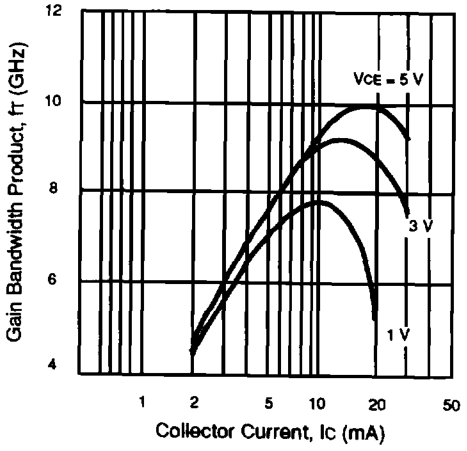
GAIN AND NOISE FIGURE OF INDIVIDUAL TRANSISTOR



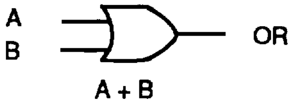
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE

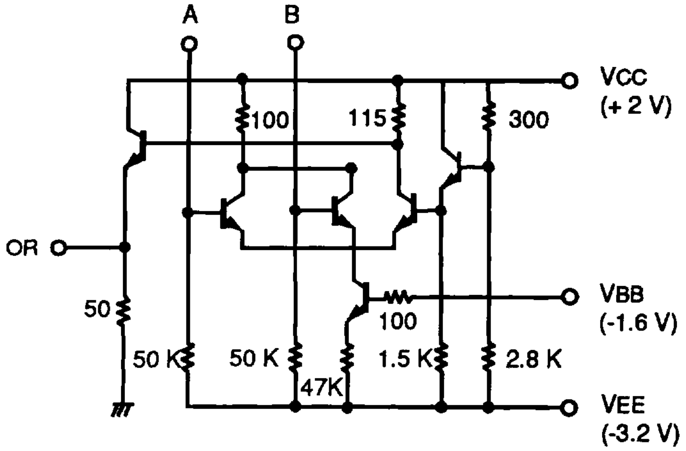


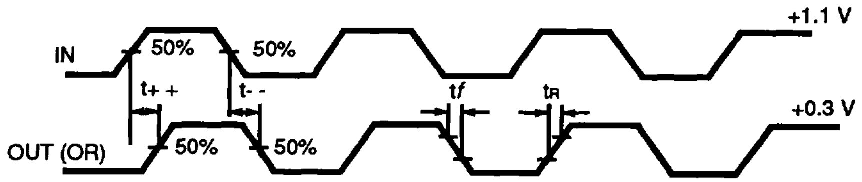
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



TYPICAL OR GATE





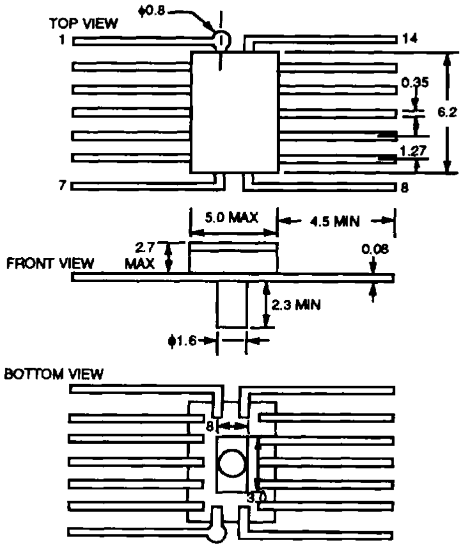


tf = 500 psec.
tr = 750 psec.

t+ + = 500 psec.
t- - = 250 psec.

OUTLINE DIMENSIONS (Units in mm)

UPA104B
PACKAGE OUTLINE BS14



See Connection Diagram for description of leads.

UPA104G
PACKAGE OUTLINE G14