CY7B180
CY7B181

CYPRESS SEMICONDUCTOR

4K x 18 Cache Tag

Features

- **Supports 66-MHz cache for all major high-speed processors**
- **4K x 18 tag organization**
- **BiCMOS for optimum speed/power**
- **High speed**
  - **— 10-ns match delay**
  - **— 13-ns tag SRAM access**
- **Selectable clock and latch modes**
- **Input address and data latches**
- **Supports multiprocessing (CY7B180) with two cache status bits per entry**
- **Supports dirty and valid bits (CY7B181)**
  - **— Dirty-bit set on write hit**
  - **— Two cycles to invalidate entire tag array**
  - **— Match qualified by valid bit**
- **Write output to cache RAM asserted during write hit**
- **Cascadeable**
  - **— up to four cache tags with no external logic**
- **Can be used as 4K x 18 SRAM**

Functional Description

The CY7B180 and CY7B181 are high-performance BiCMOS cache tag RAMs organized as 4096 words by 18 bits. Each word contains a 16-bit address tag field and a 2-bit status field. Because the CY7B180 is optimized for multiprocessor applications where cache coherency is important, the two status bits are unassigned and can be used to store multiprocessing cache status information. Uniprocessor applications implementing write-through or copy-back cache policies are best supported by the CY7B181. The two status bits are assigned as the valid bit and the dirty bit. To simplify the cache controller logic, the dirty bit is set automatically during a write hit. The tag field and the status field can be loaded separately via a dedicated I/O data port.

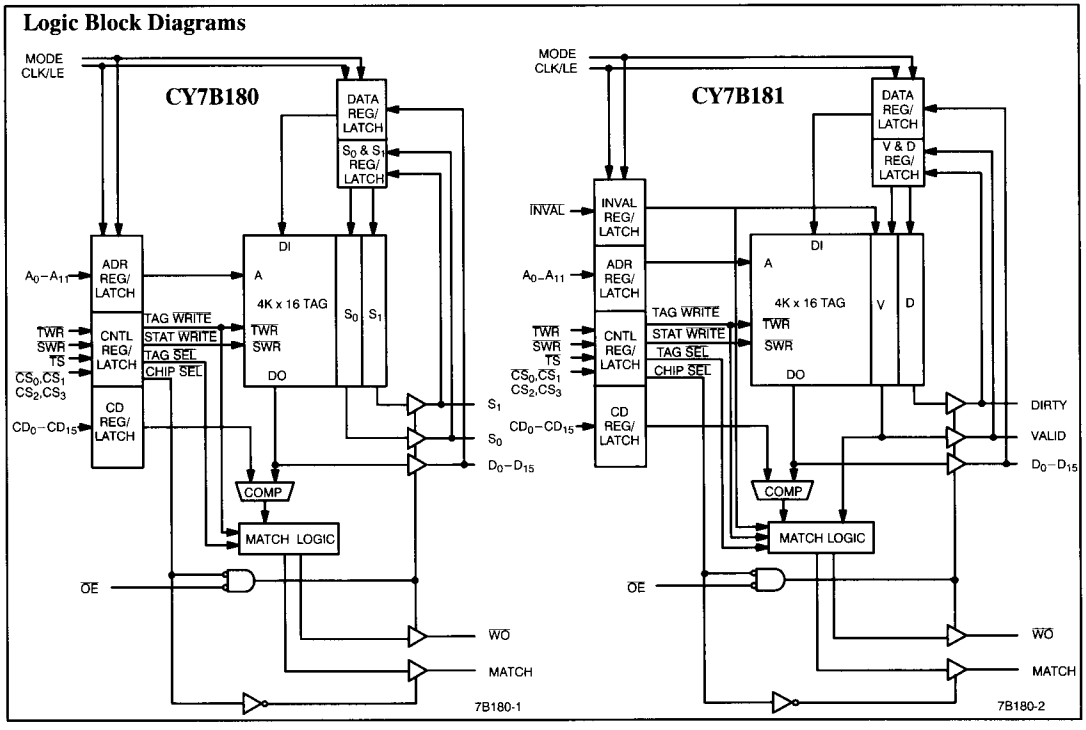
The twelve address lines select one of the 4096 words in the tag RAM. The 16-bit tag address is matched against data presented at the Compare Data inputs. In the CY7B181, the match output is qualified by the valid bit of the chosen word. Match is asserted only if the comparison is successful and the valid bit is set. The contents of the tag and status fields in the selected entry are available to external logic as direct output pins.

In many cache systems, generating the write signal to the cache RAMs is a time-consuming process because the write signal must be qualified with the match signal from the cache tag. The CY7B180/CY7B181 incorporates this function on-chip by asserting the write output ($\overline{WO}$) whenever a write hit is detected.

Tag invalidation in the CY7B181 is controlled by the $\overline{INVAL}$ input. Holding this input low for two consecutive cycles will invalidate the entire tag RAM. Individual entries can be invalidated by writing a zero into the valid bit of that entry.

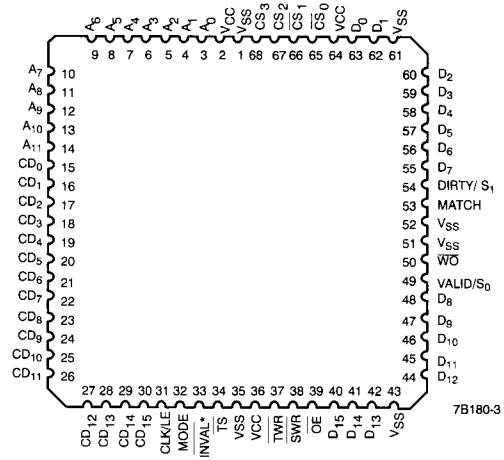
With a match delay of 10 ns and selectable clock or latch mode, the CY7B180 and CY7B181 can be used with all major high-speed microprocessors currently offered. The 13-ns address access of these parts also allows them to be used as 4K by 18 cache data RAMs.

Logic Block Diagrams



Pin Configurations

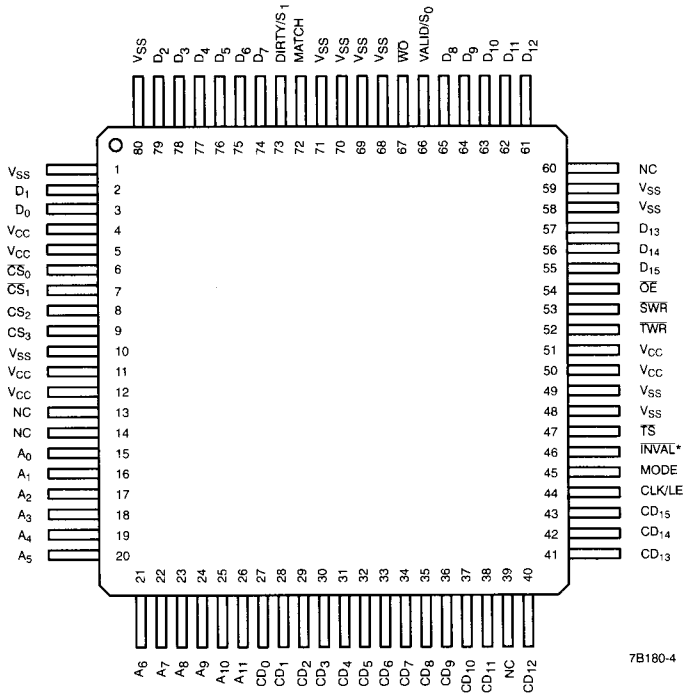
LCC & PLCC
Top View



* The $\overline{\text{INVAL}}$ input is only available on the CY7B181

Pin Configurations (continued)

PQFP
Top View



* Note: INVAL not supported in CY7B180.

Selection Guide

		7B180–10 7B181–10	7B180–12 7B181–12	7B180–15 7B181–15	7B180–20 7B181–20
Match Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	340	325	315	
	Military			390	390

Shaded area contains preliminary information.

Functional Description (continued)

Clock Mode

The CLOCK mode is selected when the MODE input is LOW. The address, compare data, chip select, and tag select are sampled at the rising edge of CLK. Write data is sampled on the falling edge of CLK. The tag write and status write inputs are different in that they are level sampled by CLK. If CLK is HIGH, the input latches associated with the tag write and status write inputs are transparent, and these inputs are allowed to ripple into the CY7B180/CY7B181. These inputs are latched when CLK goes LOW.

Latch Mode

The LATCH mode is selected when the MODE input is HIGH. All inputs are level sampled by LE. If LE is high, the input latches are transparent and the inputs are allowed to ripple into the CY7B180/CY7B181. When LE goes LOW, the inputs are latched and are no longer sampled. However, $\overline{LE}$ must still be strobed low to initiate a self-timed write.

Tag Storage

The CY7B180/CY7B181 provides 4096 cache tag entries. Each 7B181 entry contains a 16-bit cache tag address, a valid (V) bit, and a dirty (D) bit. The same two bits in the CY7B180 are generic status bits, and their meanings must be interpreted and controlled by the external processor.

On the CY7B181, the valid bit specifies the validity of the tag entry. A match is detected only when the 16-bit tag of the selected entry matches the 16 compare inputs and the valid bit is set. The dirty bit on the CY7B181 indicates whether the cache line associated with the tag entry has been modified and its value is available to external logic as the DIRTY output. The D bit in a selected entry on the CY7B181 is set if the current access is a write and a hit is detected. The valid bit in the selected entry is also available as the VALID output so that external logic can determine the cause of a miss:

- If the V bit is HIGH, then the miss is caused by tag mismatch.
- If the V bit is LOW, then the miss is caused by either a tag mismatch or an invalid, or both.

The cache tag entry format is shown in *Figure 1*.

Tag Compare

A tag compare cycle is initiated if tag select ($\overline{TS}$) is HIGH. $\overline{TS}$ is sampled at the rising edge of CLK (in the clock mode) or captured by the positive level of LE (in the latch mode). Once a tag entry is selected by A_0 through A_{11}, its 16-bit tag address is compared against CD_0 through CD_{15}. The compare result is delivered to the match logic.

The match output of the CY7B180 is driven HIGH if the compare is successful. For the CY7B181, the compare result is qualified by the state of the valid (V) bit in the selected entry. MATCH is driven HIGH only when the compare is successful and the valid bit is set.

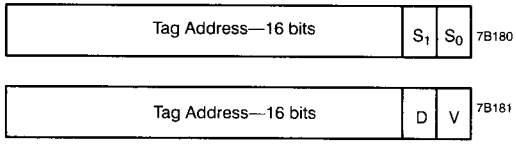


Figure 1. Cache Tag Entry Format

In addition, the write output ($\overline{WO}$) of the CY7B180/CY7B181 is asserted whenever a match is detected in a CPU write cycle ($\overline{TS}$ = 1 and $\overline{TWR}$ = 0). In some applications, this signal may be connected directly to the write input of the cache RAM.

Tag Access

The tag access cycle is initiated by asserting the tag select ($\overline{TS}$) input. Reading and writing is controlled by the tag write ($\overline{TWR}$) and status write ($\overline{SWR}$) inputs. In both clock and latch modes, the state of $\overline{TWR}$ and $\overline{SWR}$ are captured by the positive level of the CLK/LE input. The MATCH and $\overline{WO}$ outputs remain HIGH during tag access cycles.

If $\overline{TWR}$ is HIGH, the tag address field of the selected entry is driven onto data lines D_0 through D_{15} provided output enable ($\overline{OE}$) is LOW. For the CY7B180, the state of the two generic status bits are available at the S_0 and S_1 outputs if $\overline{SWR}$ is HIGH. For the CY7B181, the valid and dirty bits of the chosen entry are driven onto the valid and dirty outputs if $\overline{SWR}$ is HIGH.

Changing the tag content is accomplished by asserting the $\overline{TWR}$ and $\overline{SWR}$ inputs. $\overline{TWR}$ controls the loading of the tag address field while $\overline{SWR}$ controls the loading of the status field (S_0, S_1 in the CY7B180, valid and dirty in the CY7B181). Because the CY7B180/CY7B181 are common I/O devices, $\overline{OE}$ must be driven HIGH before data is placed on the data inputs and the status inputs.

Cascade Operation

Up to four CY7B180/CY7B181s can be used in a system by connecting appropriate address lines to the four chip select inputs. A cache tag is selected only if $\overline{CS_0} = \overline{CS_1} = 0$ and $CS_2 = CS_3 = 1$. Once selected, the CY7B180/CY7B181 will either execute a tag comparison cycle or a tag access cycle (depending on the state of the $\overline{TS}$ input). If a cache tag is deselected, it disables the comparison logic and three-states match, valid, dirty, $\overline{WO}$, and D_{15} through D_0 outputs.

The four chip selects are sampled at the positive edge of CLK (in clock mode) or sampled by the positive level of LE (in latch mode). By connecting the chip selects to the appropriate address bits or logic levels (see *Table 1* and *Figure 2*), four CY7B180/1s can be cascaded to provide 16,384 tag entries with no external logic.

Pin Descriptions

The cache tag RAM is packaged in a 68-pin PGA, PLCC, and LCC and in an 80-pin PQFP. The following sections are brief descriptions of the pin functions:

Supplies

V_{CC}—3 pins, connected to the +5V power supply (6 in the PQFP package).

GND—6 pins, connected to ground (11 in the PQFP package).

Input Signals

$A_{11} - A_0$—Address from the processor, 12 pins. These inputs are registered/latched and are controlled by CLK/LE. In the clock mode, the register is positive-edge triggered. In the LATCH mode, the latch is positive-level triggered. While in LATCH mode, if the LE input is HIGH, the latch is transparent and the addresses are allowed to ripple into the CY7B180/CY7B181 to start a new access. These 12 address inputs are used to select one of the 4096 cache tag entries.

Table 1. Chip Select Connections for Cascading Four Cache Tags

Tag 1				Tag 2			
CS_3	CS_2	$\overline{CS_1}$	$\overline{CS_0}$	CS_3	CS_2	$\overline{CS_1}$	$\overline{CS_0}$
H	H	Adr X+1	Adr X	H	Adr X	L	Adr X+1
Tag 3				**Tag 4**			
CS_3	CS_2	$\overline{CS_1}$	$\overline{CS_0}$	CS_3	CS_2	$\overline{CS_1}$	$\overline{CS_0}$
H	Adr X+1	L	Adr X	Adr X+1	Adr X	L	L

Tag 1 is selected when Adr X+1, Adr X = LL
Tag 2 is selected when Adr X+1, Adr X = LH
Tag 3 is selected when Adr X+1, Adr X = HL
Tag 4 is selected when Adr X+1, Adr X = HH

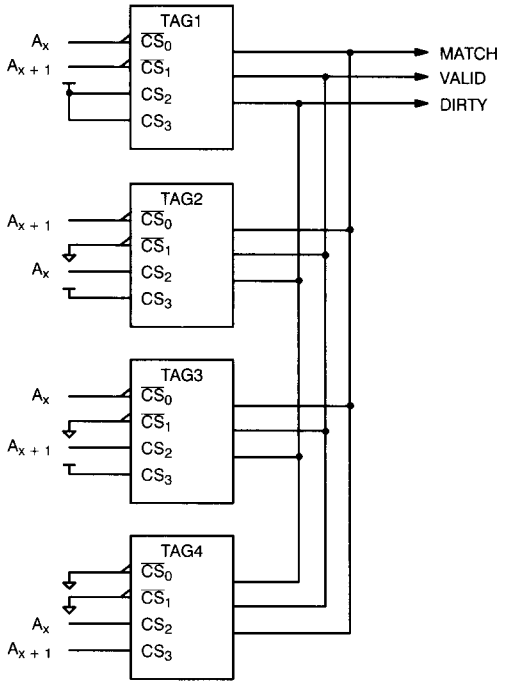


Figure 2. Cascading the CY7B180 and CY7B181

Pin Summary

Signal	Dir.	# of Pins	Description
V_{CC}		3	+5V
GND		6	Ground
$A_{11} - A_0$	I	12	Tag Address
CLK/LE	I	1	Clock/Latch
MODE	I	1	Mode Select
$CD_{15} - CD_0$	I	16	Compare Data
$\overline{CS_1} - \overline{CS_0}$	I	2	Chip Selects 1 & 0
$CS_3 - CS_2$	I	2	Chip Selects 3 & 2
$\overline{TS}$	I	1	Tag Select
$\overline{TWR}$	I	1	Tag Write Signal
$\overline{SWR}$	I	1	Status Write Signal
$\overline{INVAL}$	I	1	Tag Invalidate (CY7B181 only)
MATCH	O	1	Cache Match
$\overline{WO}$	O	1	Cache Write Match
VALID/S_0	I/O	1	Valid/Status Bit 0
DIRTY/S_1	I/O	1	Dirty/Status Bit 1
$D_{15} - D_0$	I/O	16	Processor Data
$\overline{OE}$	I	1	Output Enable

Pin Descriptions (continued)

MODE—Mode select, 1 pin. The clock mode is selected by strapping the MODE input LOW. The latch mode is selected by strapping this input HIGH.

CLK/LE—Clock/Latch input, 1 pin. This input controls all input registers and latches.

$CD_{15} - CD_0$—Compare data, 16 pins. These inputs are registered/latched by CLK/LE. In the clock mode, the register is positive-edge triggered. In the latch mode, the latch is positive-level triggered. While in the latch mode, if the LE input is HIGH, the latch is transparent and the compare data is allowed to ripple into the CY7B180/CY7B181 to the comparison logic. The contents of the compare register/latch are compared with the 16-bit tag address in the selected tag entry.

$\overline{CS_0} - \overline{CS_1}$—Chip select 0 – 1, active LOW, 2 pins. These inputs are registered/latched by CLK/LE. In the clock mode, the register is positive-edge triggered. In the LATCH mode, the latch is positive-level triggered. While in the LATCH mode, if the LE input is HIGH, the latch is transparent and the chip select inputs are allowed to ripple into the CY7B180/CY7B181. If $\overline{CS_1}$, $\overline{CS_0}$ are LOW and CS_2, CS_3 are HIGH, the comparison logic and output drivers are enabled, otherwise, the comparison logic will be disabled and all output drivers will be three-stated.

CS_2, CS_3—Chip select 2 – 3, active HIGH, 2 pins. These inputs are registered/latched CLK/LE. In the clock mode, the register is positive-edge triggered. In the latch mode, the latch is positive-level triggered. While in the latch mode, if the LE input is HIGH, the latch is transparent and the chip select inputs are allowed to ripple into the CY7B180/CY7B181. If CS_2, CS_3 are HIGH and $\overline{CS_1}$, $\overline{CS_0}$

are LOW, the comparison logic and output drivers are enabled, otherwise, the comparison logic will be disabled and all output drivers will be three-stated.

$\overline{TS}$—Tag select, active LOW, 1 pin. This input is registered/latched by CLK/LE. In the clock mode, the register is positive-edge triggered. In the latch mode, the latch is positive-level triggered. While in the latch mode, if LE is HIGH, the latch is transparent and the $\overline{TS}$ is allowed to ripple into the CY7B180/CY7B181. If $\overline{TS}$ is LOW, external logic is allowed to modify (read or write) the tag entries. If $\overline{TS}$ is HIGH, the tag entries are available only for address comparisons.

$\overline{TWR}$—Tag write indicator, active LOW, 1 pin. This input is latched and is controlled by CLK/LE. In both the clock and latch modes, the latch is positive-level triggered. While CLK/LE is HIGH, the latch is transparent and $\overline{TWR}$ is allowed to ripple into the CY7B180/CY7B181. $\overline{TWR}$ is handled according to the access mode: tag access mode or tag compare mode. In the tag access mode ($\overline{TS}$ = 0), $\overline{TWR}$ controls the access direction of the tag: a HIGH indicates a read while a LOW indicates a write. Assertion of $\overline{TWR}$ will store data on D_{15} through D_0 into the 16-bit tag address field of the selected entry. In the tag compare mode ($\overline{TS}$ = 1) of the CY7B181, $\overline{TWR}$ determines the setting of the dirty bit in the selected tag entry; the D bit is set if a tag match is detected and $\overline{TWR}$ is LOW. The $\overline{TWR}$ input of the CY7B180 is ignored in the tag compare mode; the status bits S_0 and S_1 are not modified.

$\overline{SWR}$—Status write indicator, active LOW, 1 pin. This input is latched by CLK/LE. In both the clock and latch modes, the latch is positive-level triggered. While CLK/LE is HIGH, the latch is transparent and $\overline{SWR}$ is allowed to ripple into the CY7B180/CY7B181. $\overline{SWR}$ is handled according to the access mode: tag access mode or tag compare mode. In the tag access mode ($\overline{TS}$ = 0), $\overline{SWR}$ controls the access direction of the status bits in the selected tag: a HIGH indicates a read while a LOW indicates a write. Assertion of $\overline{SWR}$ will store the data presented at the status inputs into the status bits of the selected entry. In the tag compare mode ($\overline{TS}$ = 1), the state of $\overline{SWR}$ is ignored.

$\overline{INVAL}$—Tag invalidate input, active LOW, 1 pin. This input is only available in the CY7B181. It is registered at the rising edge of CLK/LE. Assertion of $\overline{INVAL}$ overrides all other operations and clears all of the valid bits in the tag storage. The CY7B181 does not have to be selected to do an invalidation. An invalidation requires two cycles to complete; therefore, the $\overline{INVAL}$ input must be held for two rising edges of the CLK or LE signal. If the $\overline{INVAL}$ input is asserted, MATCH is forced LOW, $\overline{WO}$ is forced HIGH, VALID is forced LOW, DIRTY goes to an unknown state, and the data outputs (D_0 through D_{15}) go to an unknown state. The $\overline{INVAL}$ input must be asserted during power-up to ensure that all of the valid bits in the tag are cleared. The contents of the tag may be modified as a result of invalidation.

$\overline{OE}$—Output enable, 1 pin. When $\overline{OE}$ is HIGH, all outputs except match will be placed in a three-state condition. This pin must be asserted before the beginning of a tag write cycle to allow the external processor to drive data into the CY7B180/CY7B181.

Output Signals

MATCH—Cache match signal, active HIGH, 1 pin. A HIGH at this pin indicates a cache hit while a LOW indicates a cache miss. This output is HIGH during all tag access cycles ($\overline{TS}$ = 0), except on the CY7B181 when the $\overline{INVAL}$ input is asserted. If the $\overline{INVAL}$ input on the CY7B181 is asserted, the match output is forced LOW. Match is placed in a three-state condition when the tag is deselected via the chip select signals. $\overline{OE}$ has no effect on the match output.

$\overline{WO}$—Cache write match signal, active LOW, one pin. A LOW at this pin indicates a cache hit during a memory write. A HIGH indicates a cache miss during a memory write. If the $\overline{INVAL}$ input on the CY7B181 is asserted, the $\overline{WO}$ output is forced HIGH. This output is HIGH during all tag access cycles ($\overline{TS}$ = 0). $\overline{WO}$ is placed in a three-state condition when the tag is deselected via the chip select signals or when $\overline{OE}$ is HIGH.

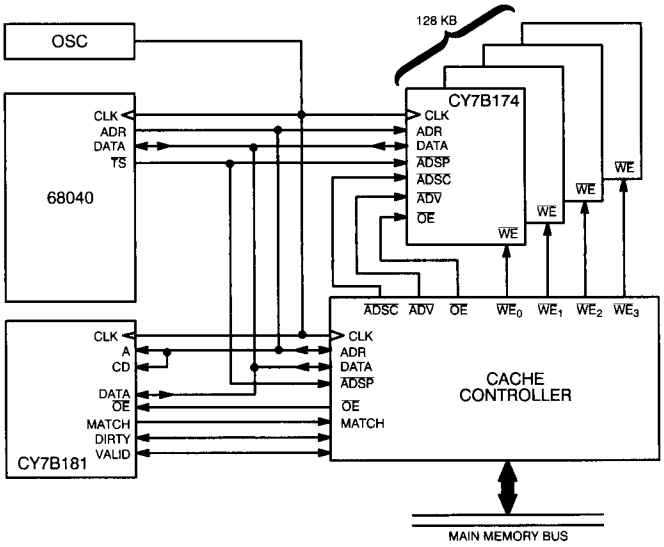
Input/Output Signals

D_{15}–D_0—Data lines to/from the processor, 16 pins. These pins are used during both tag access ($\overline{TS}$ = 0) and tag compare ($\overline{TS}$ = 1) cycles. During tag reads or tag compares, the tag address field of the selected tag entry is driven onto these lines. If the $\overline{INVAL}$ input on the CY7B181 is asserted, the data outputs will go to an unknown state. During tag writes, the $\overline{OE}$ input must be deasserted to three-state the output drivers so that these pins may be driven by the external processor. The data inputs are registered/latched by the CY7B180/CY7B181. In the clock mode, the register is negative edge triggered. In the latch mode, the latch is positive level triggered. While in the latch mode, if LE is HIGH, the latch is transparent and the data is allowed to ripple into the CY7B180/CY7B181. All 16 outputs will be placed in a three-state condition if the $\overline{OE}$ input is deasserted (HIGH) or when the cache tag is deselected via the four chip select inputs.

VALID/S_0—Valid bit (active HIGH) in CY7B181, status bit S_0 in CY7B180, 1 pin. During tag comparison and status read cycles, this pin reflects the state of the Valid bit (in CY7B181) or status bit S_0 (in CY7B180) of the selected entry. During status write cycles ($\overline{TS}$ and $\overline{SWR}$ LOW), data presented at this pin is registered/latched. In the clock mode, the register is negative-edge triggered. In the latch mode, the latch is positive-level triggered. This pin can be placed in a three-state condition via the chip select and output enable signals. If the $\overline{INVAL}$ input of the CY7B181 is asserted, the VALID output is forced LOW.

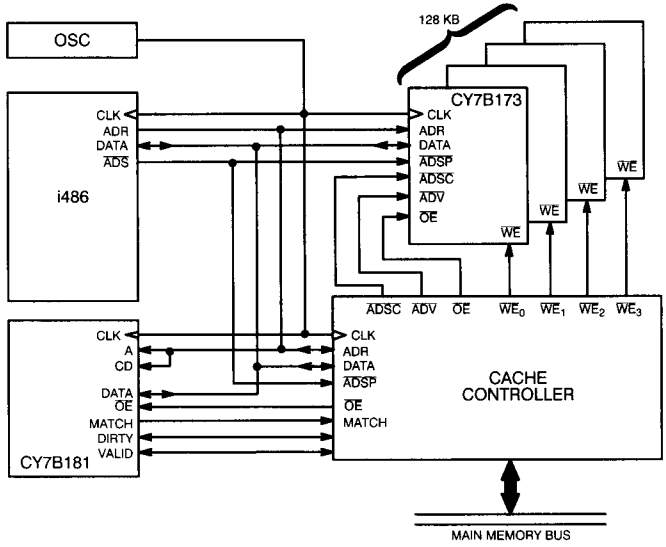
DIRTY/S_1—Dirty bit (active HIGH) in CY7B181, status bit S_1 in CY7B180, 1 pin. During tag comparison and status read cycles, this pin reflects the state of the Dirty bit (in CY7B181) or status bit S_1 (in CY7B180) of the selected entry. In copy-back caches using the CY7B181, the cache controller can examine this output to determine whether the cache line to be replaced should be copied back to the main memory. During status write cycles ($\overline{TS}$ and $\overline{SWR}$ LOW), data presented at this pin is registered/latched. In the clock mode, the register is negative-edge triggered. In the latch mode, the latch is positive-level triggered. This pin can be placed in a three-state condition via the chip select and output enable signals. If the $\overline{INVAL}$ input of the CY7B181 is asserted, the Dirty output will enter an unknown state.

Application Examples



7B180-7

A 128-Kbyte cache for a single 68040 using four CY7B174 cache RAMs and a CY7B181 cache tag. The complexity of the cache controller is reduced because the CY7B181 generates the write enable signal to the RAM automatically during write hits.



7B180-6

A 128-Kbyte secondary cache for a single i486 using four CY7B173 cache RAMs and a CY7B181 Cache Tag. Address from the i486 is checked by the cache tag at the beginning of each access. Match result is delivered to the cache controller after 10 ns.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to +V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7B180−10 7B181−10 Min.	7B180−10 7B181−10 Max.	7B180−12 7B181−12 Min.	7B180−12 7B181−12 Max.	7B180−15, 20 7B181−15, 20 Min.	7B180−15, 20 7B181−15, 20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage[1]			− 0.5	0.8	− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+10	− 10	+10	− 10	+10	µA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{OH} = 2.4V		− 2.0		− 2.0		− 2.0		mA
I_{OL}	Output LOW Current	V_{CC} = Max., V_{OL} = 0.4V		4.0		4.0		4.0		mA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+10	− 10	+10	− 10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max, V_{OUT} = GND			− 300		− 300		− 300	mA
I_{CC}	V_{CC} Operating Supply Current[4]	V_{CC} = Max., I_{OUT} MATCH = 0 mA, $\overline{OE}$ HIGH, f = f_{MAX} = $1/t_{CYC}$	Com'l		340		325		315	mA
			Mil						390	

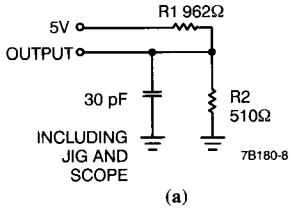
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	6.5	pF
C_{OUT}	Output Capacitance		10	pF

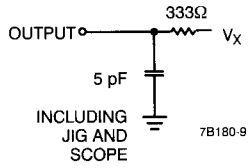
Notes:

1. $V_{IL\,(min.)}$ = − 1.5V for pulse durations of less than 20 ns.
2. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.
4. Assumes 67% read cycles and 33% write cycles (50% cache hit rate).
5. Tested initially and after any design or process changes that may affect these parameters.

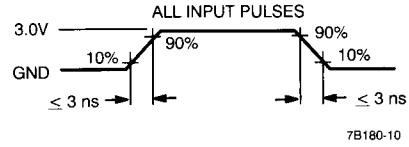
AC Test Loads and Waveforms



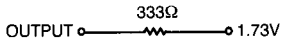
(a)



(b) Three-State Delay Load



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[6]

Parameter	Description	7B180–10 7B181–10		7B180–12 7B181–12		7B180–15 7B181–15		7B180–20 7B181–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	15		20		24		33		ns
t_{CH}	Clock HIGH	7		8		10		13		ns
t_{CL}	Clock LOW	7		8		10		13		ns
t_{OEDZ}	$\overline{OE}$ HIGH to Output High Z[7]		6		7		9		12	ns
t_{OEDV}	$\overline{OE}$ LOW to Output Valid[8]		8		9		11		13	ns
CLOCK MODE (RE = Rising Edge, FE = Falling Edge)										
t_{MCH}	Match Valid After CLK RE		10		12		15		20	ns
t_{MHLD}	Match Hold After CLK RE	2		2		2		2		ns
t_{CSD}	Status Valid After CLK RE		10		12		15		20	ns
t_{SHLD}	Status Hold After CLK RE	2		2		2		2		ns
t_{TWRWO}	Write Output Valid After $\overline{TWR}$ LOW		8		9		11		13	ns
t_{WO}	Write Output Valid After CLK RE		10		12		15		20	ns
t_{WOHLD}	Write Match Hold After CLK RE	2		2		2		2		ns
t_{AD}	Access Delay from CLK RE		13		15		18		25	ns
t_{DOH}	Output Data Hold After CLK RE	3		3		3		3		ns
t_{DIS}	Input Data Set-Up Before CLK FE	4		4		5		6		ns
t_{DIH}	Input Data Hold After CLK FE	2		2		3		4		ns
t_{TSS}	$\overline{TS}$ Set-Up Before CLK RE	3		3		4		5		ns
t_{TSH}	$\overline{TS}$ Hold After CLK RE	3		3		4		5		ns
t_{AS}	Address Set-Up Before CLK RE	3		3		4		5		ns
t_{AH}	Address Hold After CLK RE	3		3		4		5		ns
t_{CDS}	Compare Data Set-Up Before CLK RE	3		3		4		5		ns
t_{CDH}	Compare Data Hold After CLK RE	3		3		4		5		ns
t_{CSS}	Chip Select Set-Up Before CLK RE	3		3		4		5		ns
t_{CSH}	Chip Select Hold After CLK RE	3		3		4		5		ns

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7B180–10 7B181–10		7B180–12 7B181–12		7B180–15 7B181–15		7B180–20 7B181–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CSHZ}	Output High Z After CLK RE (chip deselected via CS inputs)[7, 9]		8		9		11		13	ns
t_{CSLZ}	Output Low Z After CLK RE (chip deselected via CS inputs)[8, 9]	2		2		2		2		ns
t_{WRS}	$\overline{WR}$ Set-Up Before CLK FE	3		3		4		5		ns
t_{WRH}	$\overline{WR}$ Hold After CLK FE	3		3		4		5		ns
t_{INVS1}	$\overline{INVAL}$ Set-Up Before CLK RE	3		3		4		5		ns
t_{INVH1}	$\overline{INVAL}$ Hold After CLK RE	3		3		4		5		ns
t_{MCHL1}	MATCH LOW After CLK RE Due to $\overline{INVAL}$ LOW		7		9		11		13	ns
t_{WOH1}	$\overline{WO}$ HIGH After CLK RE Due to $\overline{INVAL}$ LOW		7		9		11		13	ns
t_{VALL1}	VALID LOW After CLK RE Due to $\overline{INVAL}$ LOW		7		9		11		13	ns
LATCH MODE										
t_{LRLR}	LE Rise to Next LE Rise	15		20		24		33		ns
t_{LW}	Width of LE Pulse	5		5		6		8		ns
t_{LFLR}	LE Fall to LE Rise	8		8		10		13		ns
t_{ASLC}	Address Set-Up Before Latch Close	3		3		4		5		ns
t_{AHLC}	Address Hold After Latch Close	3		3		4		5		ns
t_{CSLC}	Chip Select Set-Up Before Latch Close	3		3		4		5		ns
t_{CHLC}	Chip Select Hold After Latch Close	3		3		4		5		ns
t_{TSLC}	Tag Select Set-Up Before Latch Close	3		3		4		5		ns
t_{THLC}	Tag Select Hold After Latch Close	3		3		4		5		ns
t_{WSLC}	Write Set-Up Before Latch Close	3		3		4		5		ns
t_{WHLC}	Write Hold After Latch Close	3		3		4		5		ns
t_{CDSLC}	Comp Data Set-Up Before Latch Close	3		3		4		5		ns
t_{CDHLC}	Comp Data Hold After Latch Close	3		3		4		5		ns
t_{DSLC}	Data In Set-Up Before Latch Close	4		4		5		6		ns
t_{DHLC}	Data In Hold After Latch Close	2		2		3		4		ns
t_{CDMCH}	Comp Data Valid to Match Valid		10		12		15		20	ns
t_{TSMCH}	Tag Select Valid to Match Valid		10		12		15		20	ns
t_{CSMCH}	Chip Select Valid to Match Valid		10		12		15		20	ns
t_{AMCH}	Address Valid to Match Valid		10		12		15		20	ns
t_{LOMCH}	Latch Open to Match Valid		10		12		15		20	ns
t_{LOMX}	Latch Open to Match Change	2		2		2		2		ns
t_{TSSV}	Tag Select Valid to Status Valid		10		12		15		20	ns
t_{CSSV}	Chip Select Valid to Status Valid		10		12		15		20	ns
t_{ASV}	Address Valid to Status Valid		10		12		15		20	ns

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7B180–10 7B181–10		7B180–12 7B181–12		7B180–15 7B181–15		7B180–20 7B181–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{LOSV}	Latch Open to Status Valid		10		12		15		20	ns
t_{LOSX}	Latch Open to Status Change	2		2		2		2		ns
t_{TWRWO}	$\overline{TWR}$ VALID to $\overline{WO}$ Valid		8		9		11		13	ns
t_{CDWO}	Comp Data Valid to $\overline{WO}$ Valid		10		12		15		20	ns
t_{TSWO}	Tag Select Valid to $\overline{WO}$ Valid		10		12		15		20	ns
t_{CSWO}	Chip Select Valid to $\overline{WO}$ Valid		10		12		15		20	ns
t_{AWO}	Address Valid to $\overline{WO}$ Valid		10		12		15		20	ns
t_{LOWO}	Latch Open to $\overline{WO}$ Valid		10		12		15		20	ns
t_{LOWOX}	Latch Open to $\overline{WO}$ Change	2		2		2		2		ns
t_{CSDV}	Chip Select Valid to Data Out Valid		13		15		18		25	ns
t_{ADV}	Address Valid to Data Out Valid		13		15		18		25	ns
t_{LODV}	Latch Open to Data Out Valid		13		15		18		25	ns
t_{LODX}	Latch Open to Data Out Change	2		2		2		2		ns
t_{TSLMH}	Tag Select LOW to Match HIGH		8		9		11		13	ns
t_{TSLWOH}	Tag Select LOW to $\overline{WO}$ HIGH		8		9		11		13	ns
t_{CSHZ}	Output High Z After the Tag is Deselected via Chip Select Inputs[7, 9]		8		9		11		13	ns
t_{CSLZ}	Output Low Z After the Tag is Selected via Chip Select Inputs[8, 9]	2		2		2		2		ns
t_{INVS2}	$\overline{INVAL}$ Set-Up Before LE RE	3		3		4		5		ns
t_{INVH2}	$\overline{INVAL}$ Hold After LE RE	3		3		4		5		ns
t_{MCHL2}	MATCH LOW After LE RE Due to $\overline{INVAL}$ LOW		7		8		10		13	ns
t_{WOH2}	$\overline{WO}$ HIGH After LE RE Due to $\overline{INVAL}$ LOW		7		8		10		13	ns
t_{VALL2}	VALID LOW After LE RE Due to $\overline{INVAL}$ LOW		7		8		10		13	ns

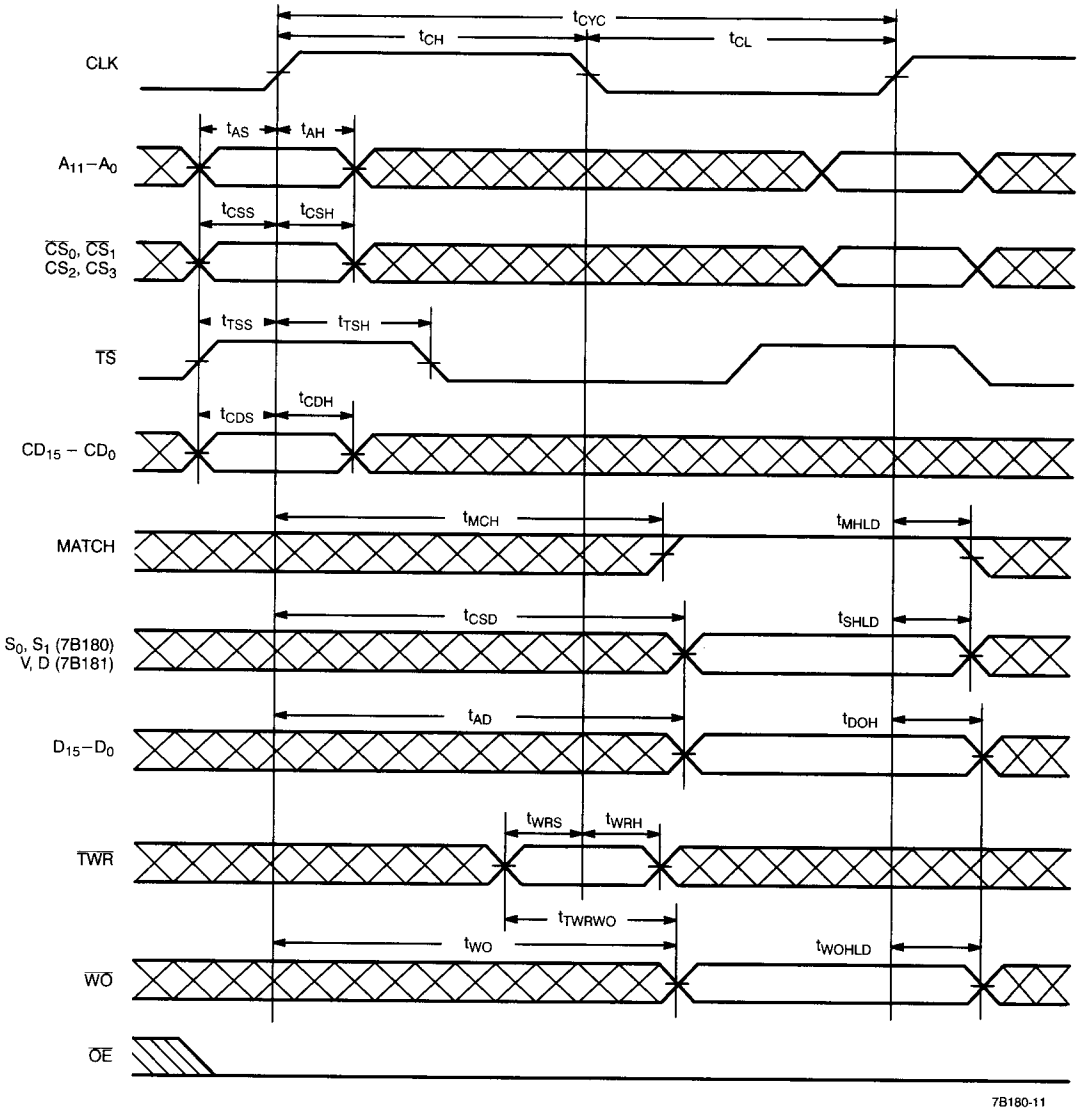
Shaded area contains preliminary information.

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 35-pF load capacitance, as in part (a) of AC Test Loads and Waveforms, unless otherwise specified.
7. t_{OEDZ} and t_{CSHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured at ±500 mV from steady-state voltage. This parameter is sampled and not 100% tested.
8. t_{OEDV} and t_{CSLZ} are tested using part (a) of AC Test Loads and Waveforms. This parameter is sampled and not 100% tested.
9. At any voltage and temperature combination, t_{CSHZ} max. is guaranteed to be smaller than t_{CSLZ} min. for a given device.

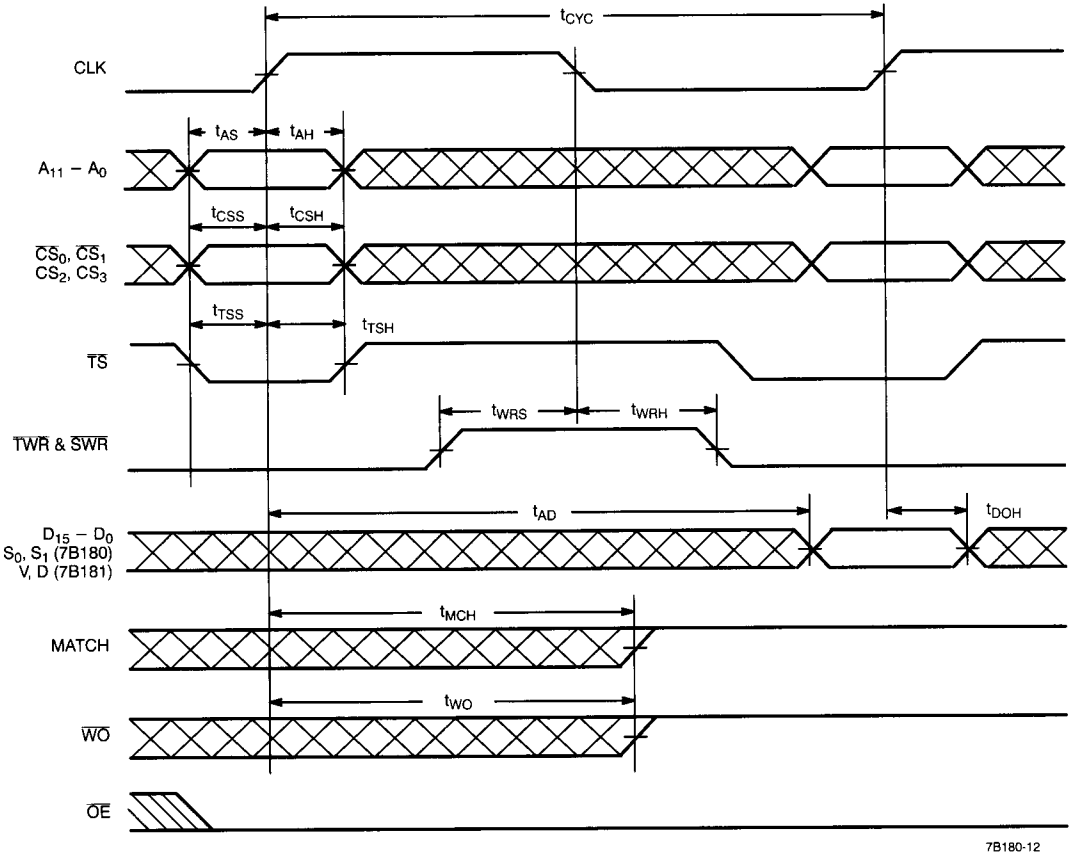
Switching Waveforms

Tag Match Timing in Clock Mode (Showing a Hit)



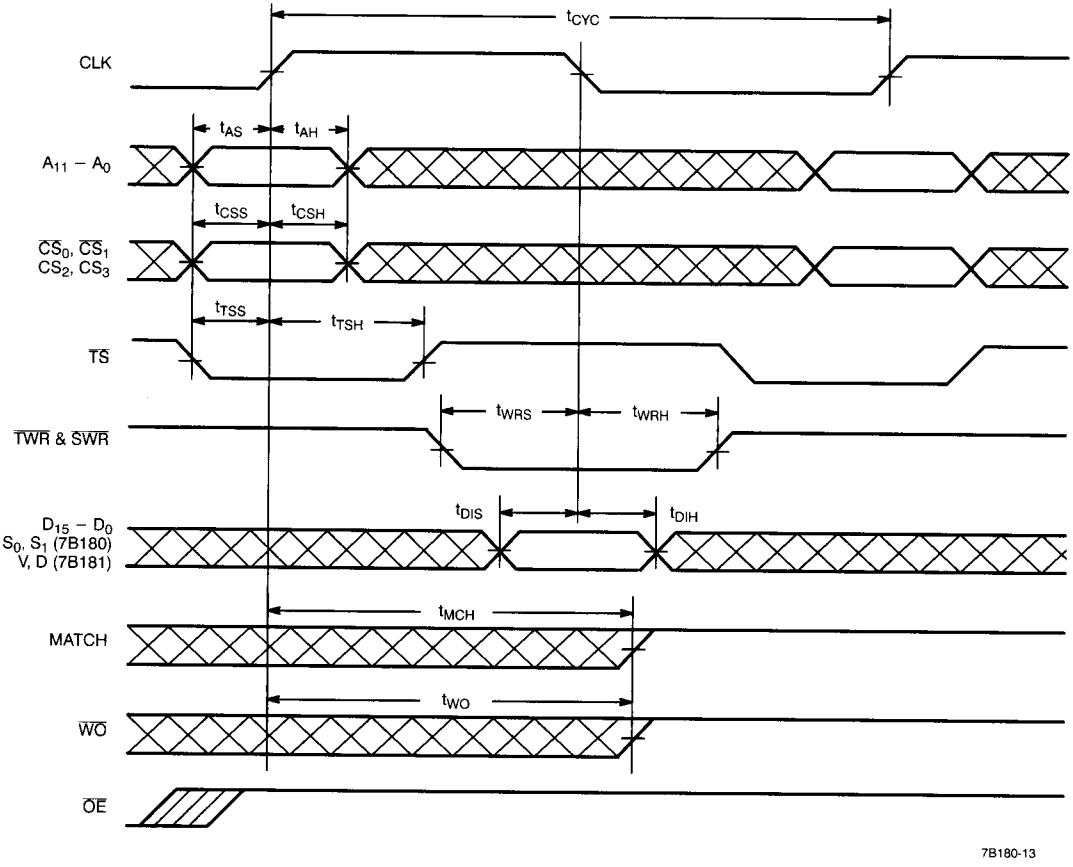
Switching Waveforms (continued)

Tag Read Timing in Clock Mode



Switching Waveforms (continued)

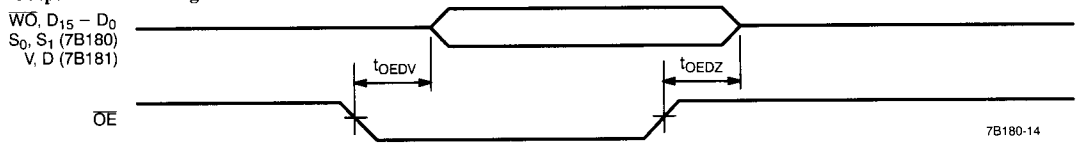
Tag Write Timing in Clock Mode



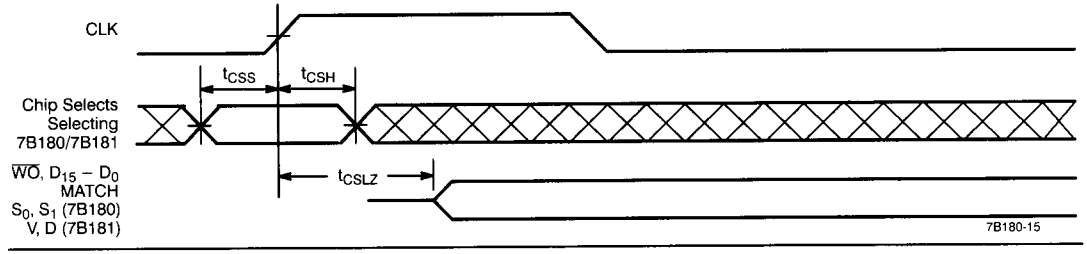
7B180-13

Switching Waveforms (continued)

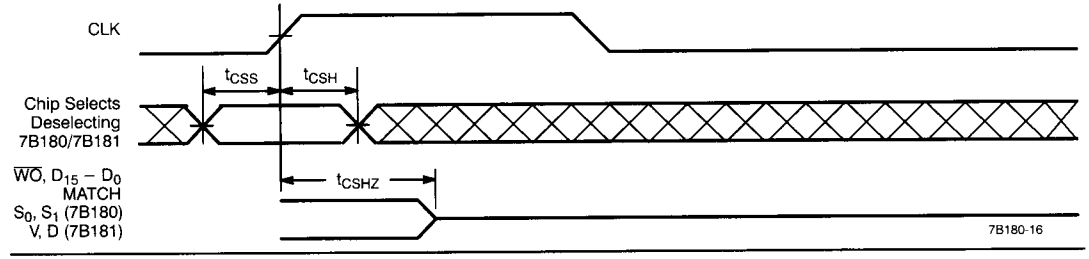
Output Enable Timing



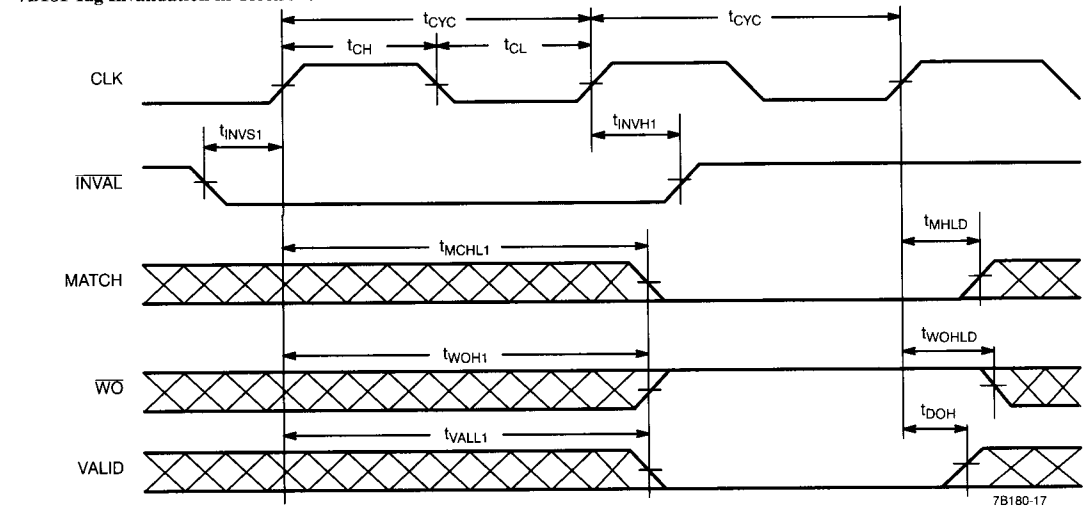
Chip Select Timing in Clock Mode



Chip Deselect Timing in Clock Mode

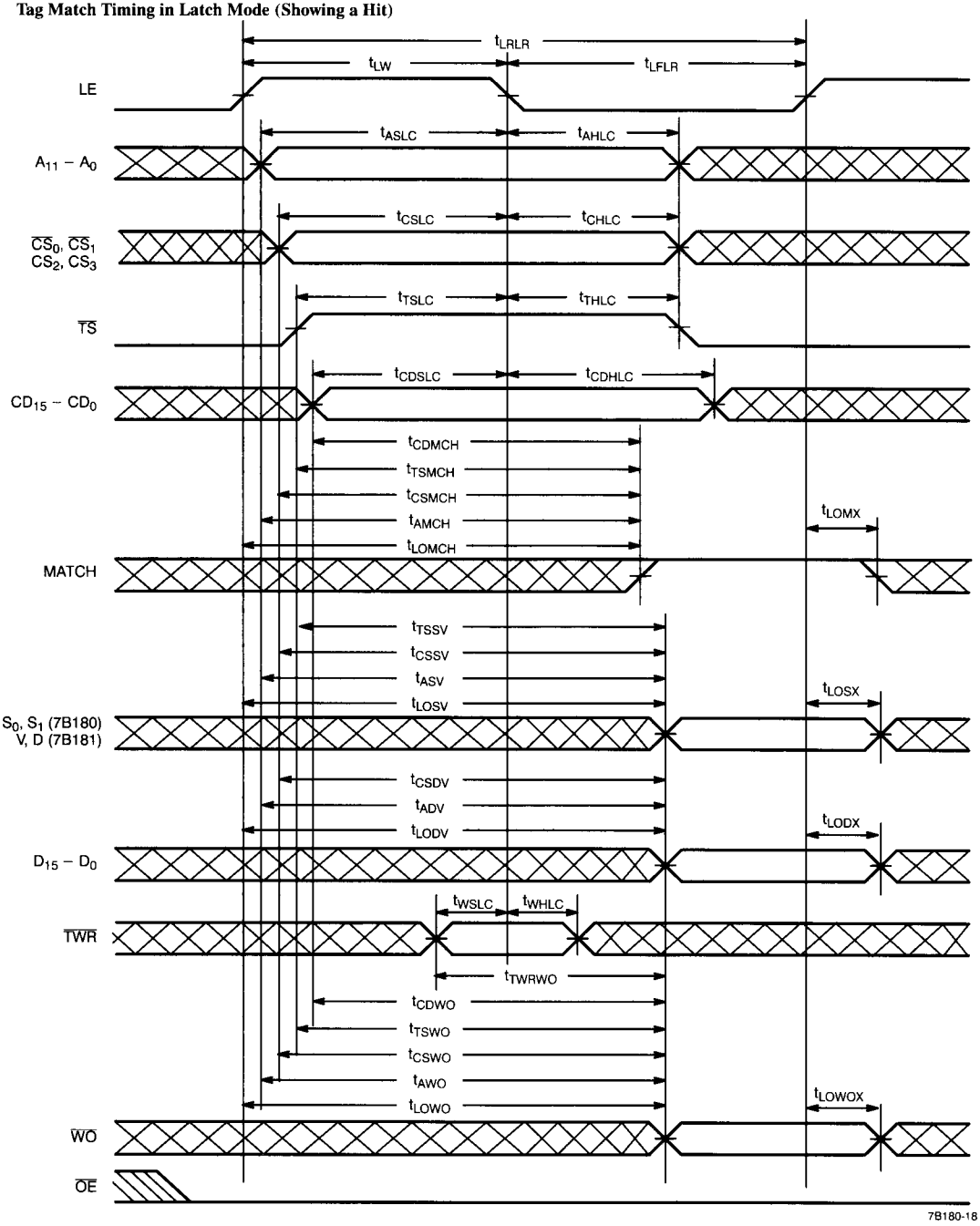


7B181 Tag Invalidation in Clock Mode



Switching Waveforms (continued)

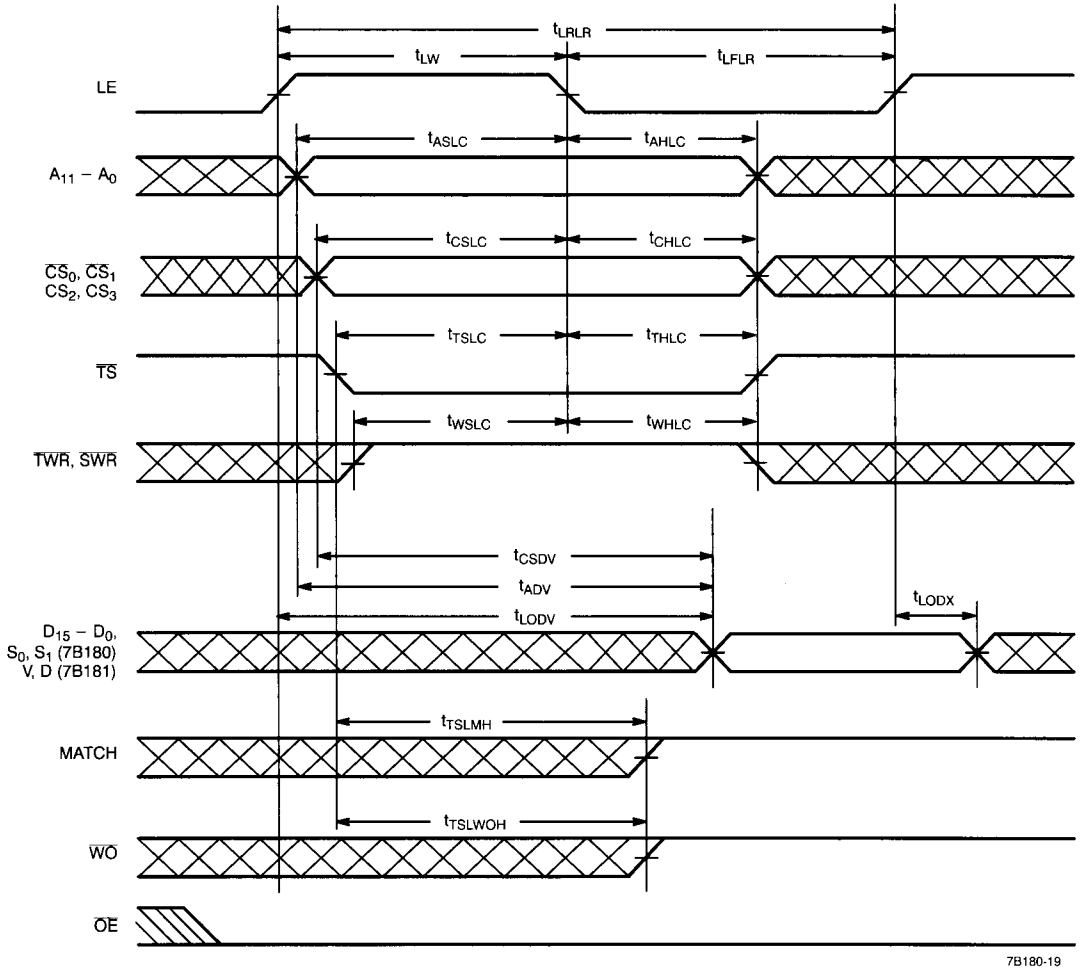
Tag Match Timing in Latch Mode (Showing a Hit)



7B180-18

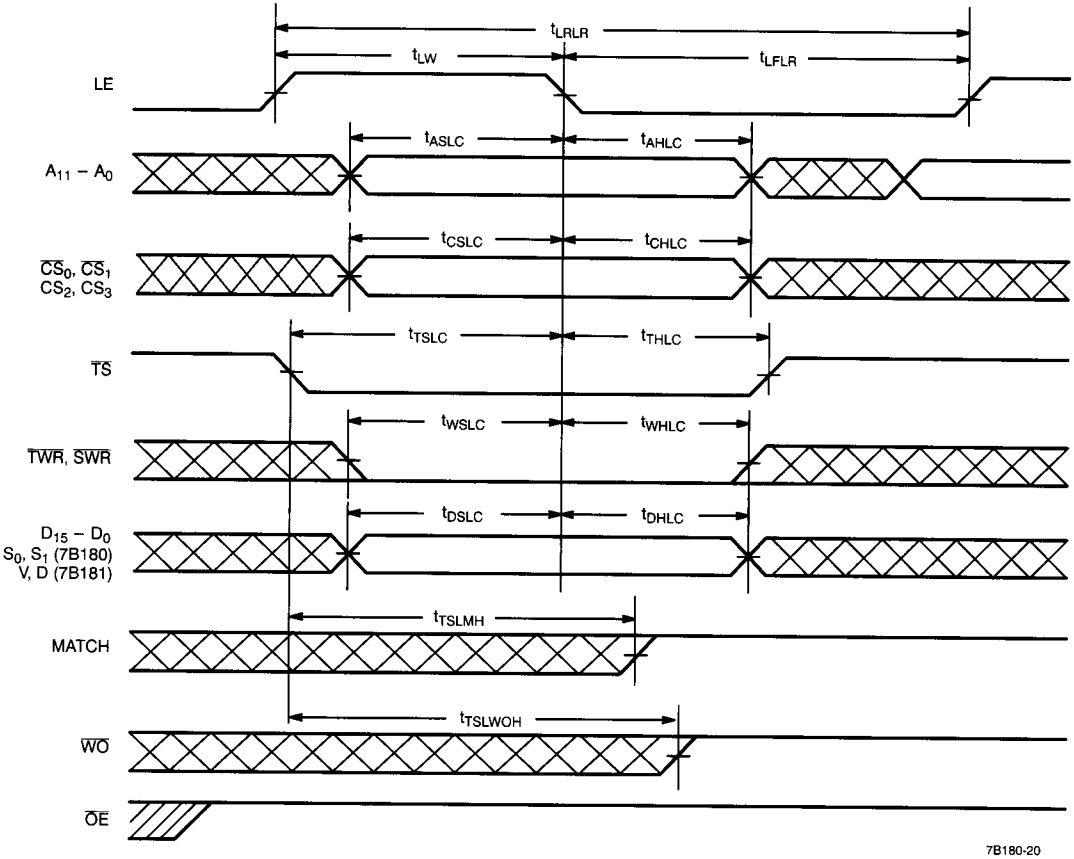
Switching Waveforms (continued)

Tag Read Timing in Latch Mode



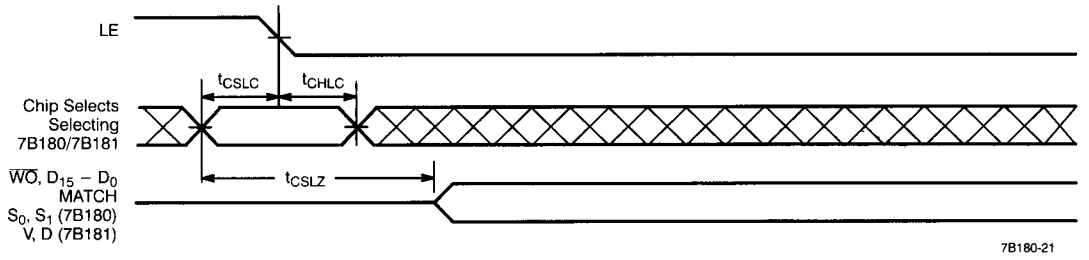
Switching Waveforms (continued)

Tag Write Timing in Latch Mode

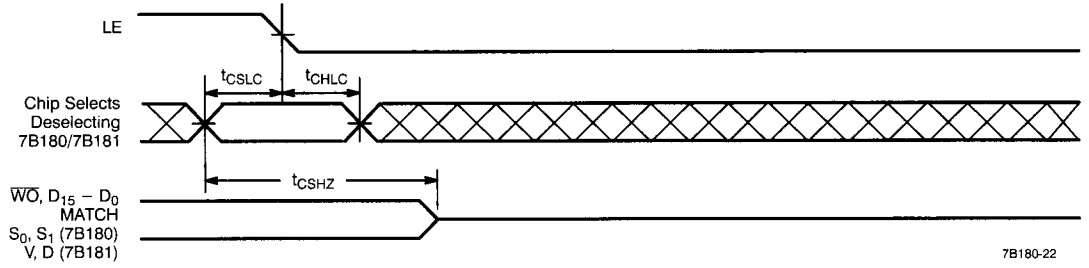


Switching Waveforms (continued)

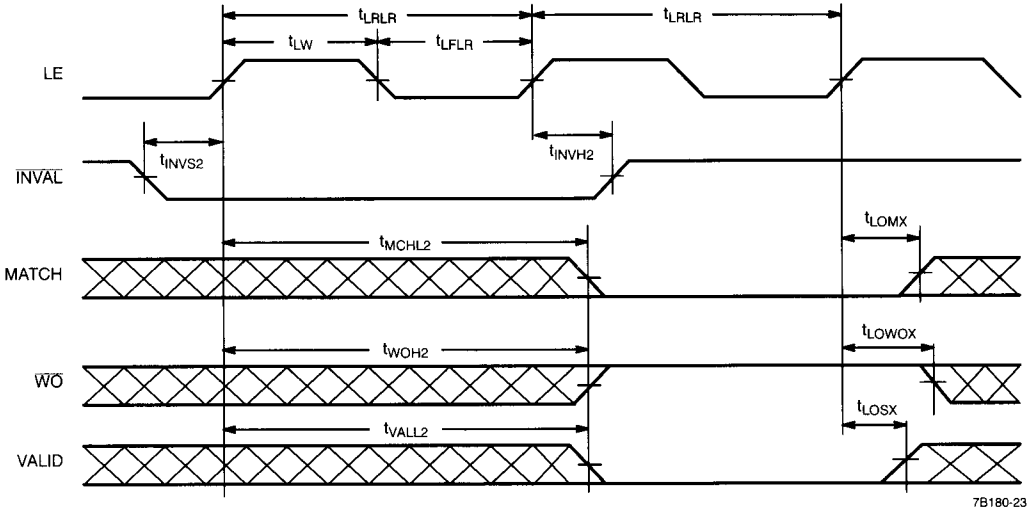
Chip Select Timing in Latch Mode



Chip Deselect Timing in Latch Mode



7B181 Tag Invalidation in Latch Mode



Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7B180–10JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B180–10NC	N80	80-Lead Plastic Quad Flatpack	
12	CY7B180–12JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B180–12NC	N80	80-Lead Plastic Quad Flatpack	
15	CY7B180–15JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B180–15NC	N80	80-Lead Plastic Quad Flatpack	
	CY7B180–15LMB	L81	68-Square Leadless Chip Carrier	Military
20	CY7B180–20LMB	L81	68-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
10	CY7B181–10JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B181–10NC	N80	80-Lead Plastic Quad Flatpack	
12	CY7B181–12JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B181–12NC	N80	80-Lead Plastic Quad Flatpack	
15	CY7B181–15JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B181–15NC	N80	80-Lead Plastic Quad Flatpack	
	CY7B181–15LMB	L81	68-Square Leadless Chip Carrier	Military
20	CY7B181–20LMB	L81	68-Square Leadless Chip Carrier	Military

Shaded area contains preliminary information.

Document #: 38–00155–D