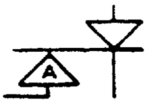
9/1/88

SPCO

High Power
53mm Silicon Controlled Rectifier
1300A / 2000V

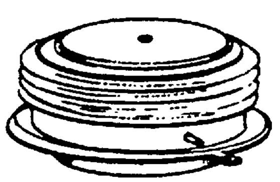
C701



AMPLIFYING GATE

The C701 Reverse Blocking Thyristor now has extended voltage blocking capability through unique multi-diffusion processing of 53 mm nominal silicon without sacrificing essential ratings and characteristics.

The C701 is designed specifically for phase control applications like DC motor control, power supplies, cycloconverters and load commutated inverters.


THYRISTOR (SCR) PRESSPAK

FEATURES

- Optimized pilot gate for high di/dt rating
- Excellent withstand to high dv/dt voltage fronts
- Enhanced surge and I²t ratings for fuse coordination
- Glazed-fluted ceramic with metal — metal welded seal 1.0 in., 25.4 mm creepage ⅝ in., 15.9 mm clearance

MAXIMUM ALLOWABLE RATINGS

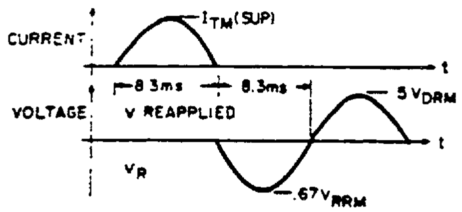
TYPE	REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE, V_{DRM}/V_{RRM}[1] T_J = -40°C to +125°C	REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE, V_{DRM}/V_{RRM}[1] T_J = 0°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE (NON-RECURRENT < 5 MILLISEC.), V_{RSM} T_J = -40°C to +125°C
C701PA	1100 Volts	1200 Volts	1200 Volts
C701PB	1200	1300	1300
C701PC	1300	1400	1400
C701PD	1400	1500	1500
C701PE	1500	1600	1600
C701PM	1600	1700	1700
C701PS	1700	1800	1800
C701PN	1800	1900	1900
C701PT	1900	2000	2000
C701L	2000	2100	2100

Average Forward Current, On-State @ T_{case} = 70°C, $I_{T(AV)}$ 1300A
Peak One-Cycle Surge On-State Current, I_{TSM} 8.3ms 20KA
10.0ms 18KA
Maximum Repetitive Rate-of-Rise of Anode Current @ 1500V bias 100A/µs
(Switching Rates ≤ 60 Hz; snubber discharge ≤ 50A; see required gate drive)
I²t (for fusing) (at 8.3 milliseconds)
Peak Gate Power Dissipation, P_{GM} .... 200 W @ 40µs pulse
Average Gate Power Dissipation, $P_{G(AV)}$ 20W
Peak Reverse Gate Voltage, V_{GRM} 20V
Peak Gate Current 15A
Storage Temperature, T_{STG} .... -40°C to +150°C
Operating Temperature, T_J .... -40°C to +125°C
Mounting Force Required .... 5000 - 6000 lb.
22.4 - 26.7 KN

NOTE
1. Half sine pulse. 10ms MAXIMUM pulse width, non repetitive
Assume presspak mounted to heat dissipator of less than 0.3 °C W
All ratings and tests in accordance with NEMA-EIA JEDEC Standard RS-397

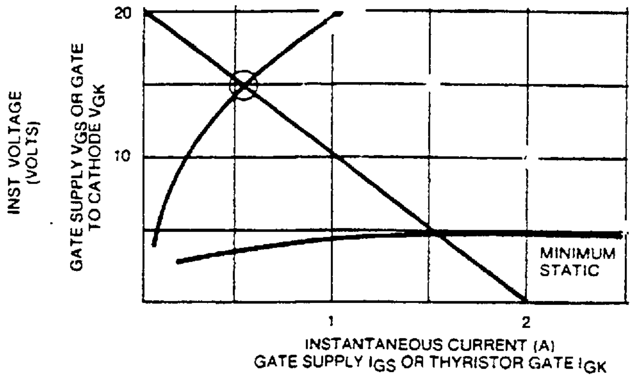
CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Reverse and Off-State Blocking Current	I_{DRM} and I_{RRM}	–	10	15	mA	T_J = +25°C, V = V_{DRM} = V_{RRM}
Peak Reverse and Off-State Blocking Current	I_{DRM} and I_{RRM}	–	45	65	mA	T_J = +125°C, V = V_{DRM} = V_{RRM}
Effective Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	–	–	.023	°C/Watt	Junction-to-Case – Double Side Cooled (DC)
Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	500		–	V/μsec	T_J = +125°C, V_{DRM} = .80 Rated, Gate Gate Open.
Holding Current	I_H	–	–	500	mAdc	T_C = +25°C, Anode supply = 20 Vdc. Initial On-State Current = 500 amps.
Latching Current	I_L	–	–	1.5	Adc	T_C = +25°C, Anode voltage = 24 Vdc. Load resistance 12 ohms max.
Delay Time	t_d	–	1.5	–	μsec	Switching From 300 Volts. 20 volt, 10 ohm Gate. 0.5 μsec Rise Time, T_J = 25°C
Gate Pulse Width Necessary to Trigger		–	–	10	μsec	0.5A, 15V minimum to support ratings
Gate Trigger Current	I_{GT}	–	60	150	mAdc	T_C = 25°C, V_D = 10 Vdc. R_L = 3 ohms
nonoperational		5.0	15	50		T_C = +125° C, V_D = .5 x Rated, R_L = 1000 ohms
Gate Trigger Voltage	V_{GT}	–	2.5	4.5	Vdc	T_C = 0°C to +125°C, V_D = 10 Vdc, R_L = 1000 ohms
nonoperational		.3	–	–		T_C = +125°C, V_D = .5 x Rated, R_L = 1000 ohms
Peak On-State Voltage	V_{TM}	–	–	1.21	Volts	I_T = 1000A T_j = 125°C
Circuit Commutated Turn-Off Time	t_q	–	125	250	μsec	(1) T_C = +125°C (2) I_T = 1000 Amps. (3) V_R = 75 Volts min. (4) 0.5 V_{DRM} Reapplied (5) Rate-of-rise of reapplied forward blocking voltage = 50V/μsec. (linear) (6) Gate bias during turn-off interval, Duty cycle ≤ 0.01%
Suppressible Surge Current	$I_{TM(SUP)}$	–	18	–	KA	(1) T_C = 115°C (2) V_R = .67 V_{DRM} (3) .67 V_{RRM} Applied, 8.3 msec after completion of surge. (see waveforms below)



SUPPRESSIBLE SURGE CURRENT TEST

U2



Thyristor Gate Impedance

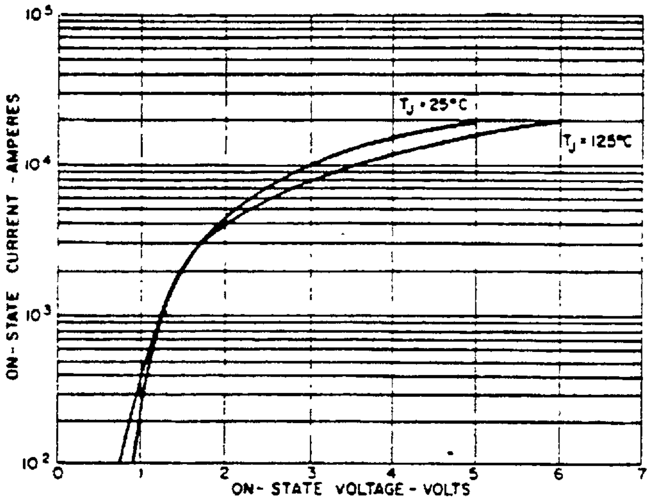
- This is enhanced by fast rising gate voltage, increasing anode bias and temperature.
- It is shown at a minimum for dc voltage, zero bias and low temperature.
- It is shown at a maximum for operating bias and recommended gate drive.

Gate Supply

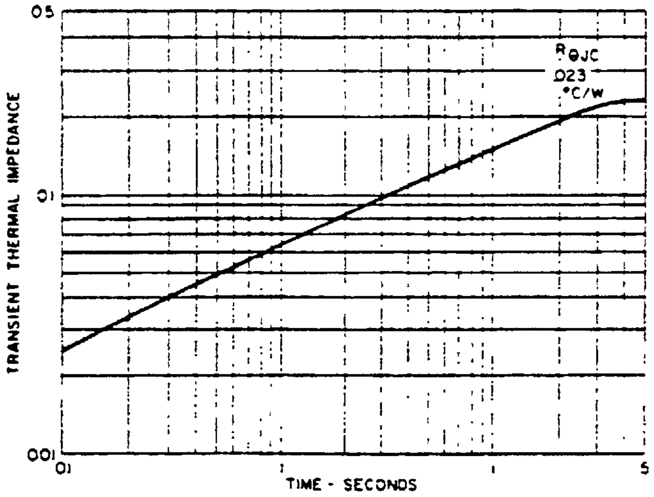
- The short circuit current rise time should be approximately 0.5μs and the duration longer than the delay time expected for the thyristor.

Minimum Acceptable Gate Current

- The intersection of load line and gate characteristic (encircled) indicates the minimum value of actual current flowing into the gate that is required during the delay time interval needed for the published di/dt and snubber discharge ratings.



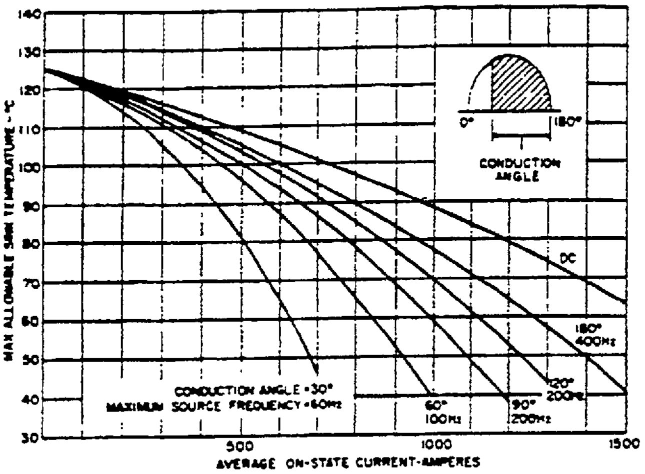
MAXIMUM ON-STATE CHARACTERISTICS



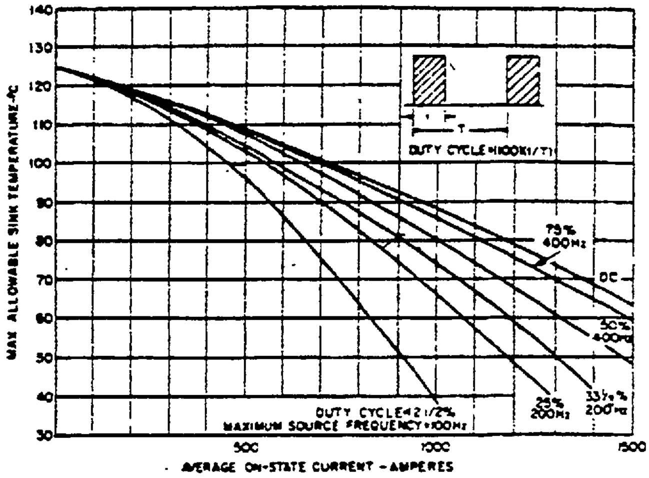
TRANSIENT THERMAL RESISTANCE –
JUNCTION-TO-HEATSINK

NOTES:

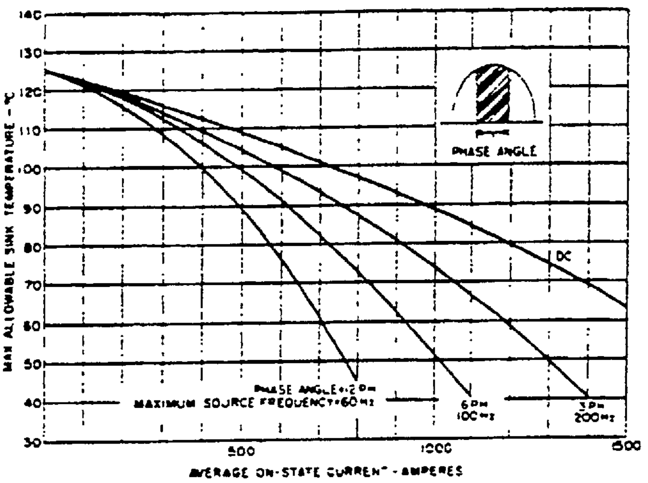
1. Add .006°C/W to account for both case to dissipator interfaces when properly mounted; e.g., $R_{\theta JS}$ = .029°C/W. See Mounting Instructions.
2. DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
   - end of conducting portion of cycle
     - 120° sq. wave add .0025°C/W along entire curve
     - 180° sq. wave add .0018°C/W along entire curve
     - 180° sine wave add .0010°C/W along entire curve
   - end of full cycle
     - any wave, subtract .001°C/W along entire curve.



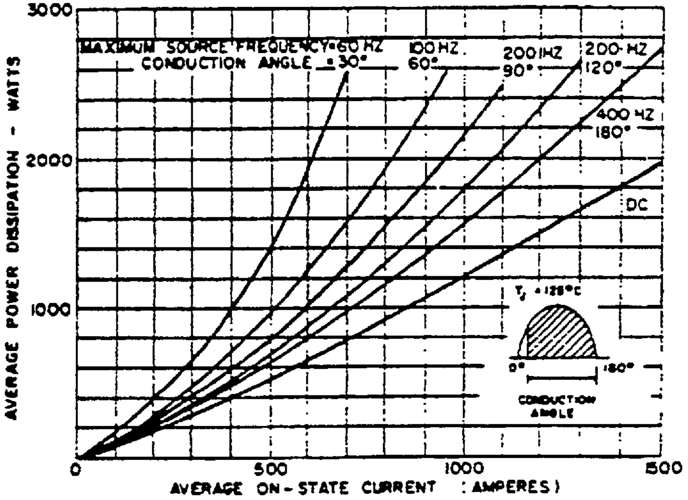
1. MAXIMUM ALLOWABLE HEATSINK TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM – DOUBLE-SIDE COOLING



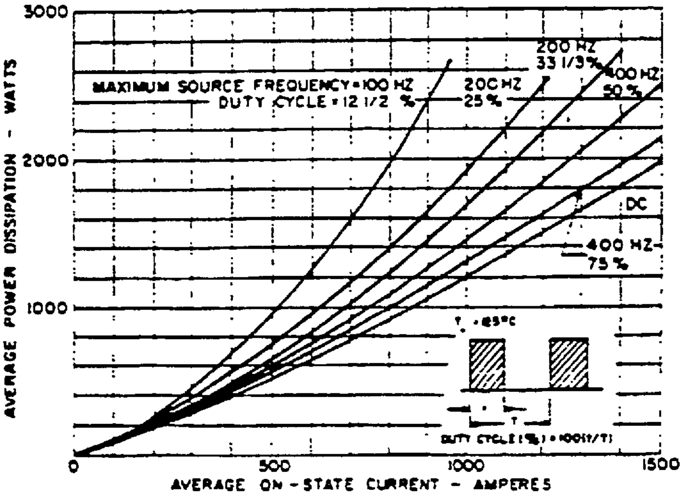
2. MAXIMUM ALLOWABLE HEATSINK TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM – DOUBLE-SIDE COOLING



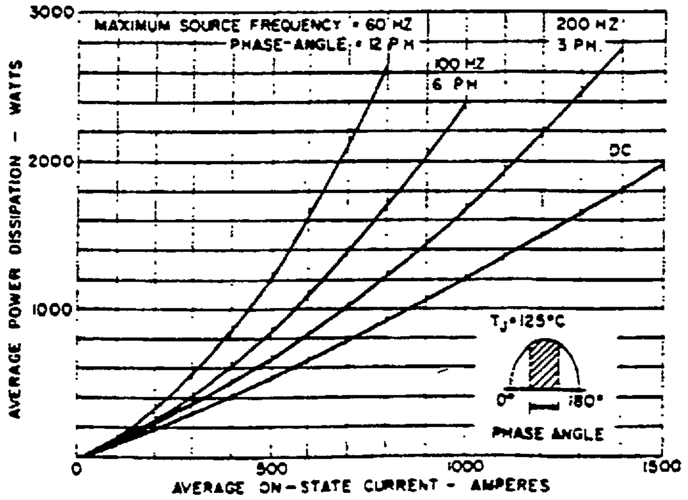
3. MAXIMUM ALLOWABLE HEATSINK HEATSINK TEMPERATURE – CIRCUIT PHASE CURRENT WAVEFORM – DOUBLE-SIDE COOLING



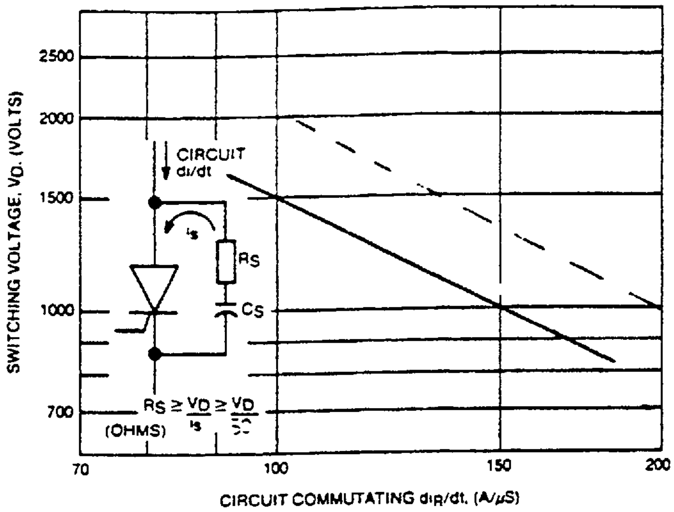
4. AVERAGE FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



5. FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



6. AVERAGE FORWARD POWER DISSIPATION



NOTES:

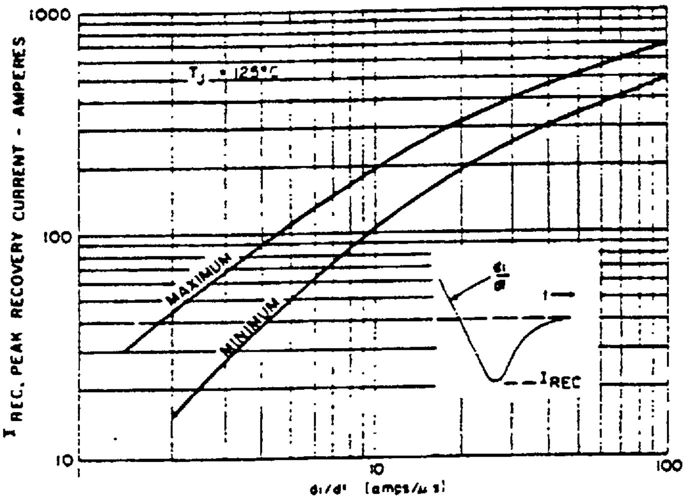
Code: — — — Non-Repetitive High Gate Drive
——— Repetitive High Gate Drive

	High Gate Drive
Source	20V/10 ohms
Pulse Width, t_p	≥10 μs
Current Rise Time, t_r	≤0.5 μs

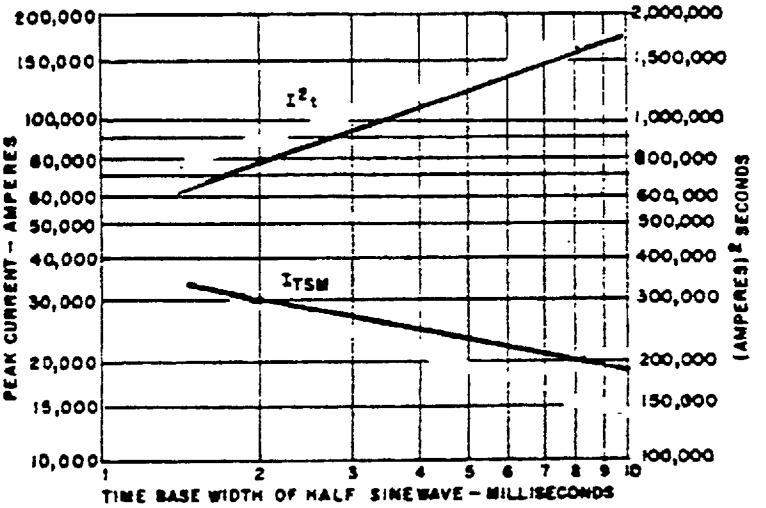
*Permissible circuit di/dt excluding snubber discharge. Repetitive di/dt is SPCO recommended maximum condition to achieve most industrial requirements for service life. It meets or exceeds the JEDEC test requirements for certification set forth in NEMA Std. Sk. 516 (1972). Non-repetitive di/dt meets the JEDEC 5 second rating.

**Snubber discharge, i_s, is treated separately using the minimum value of snubber resistance indicated. This applies for long industrial life (20 — 30 years) in combination with circuit di/dt.

ALLOWABLE DI/DT AND SNUBBER RESISTANCE

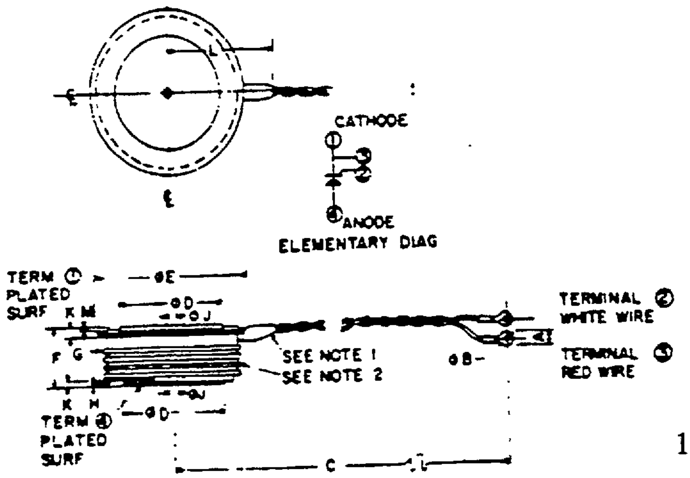


PEAK RECOVERY CURRENT



NON-REPETITIVE I_{TSM} AND I^2t CAPABILITY FOR FUSE COORDINATION

OUTLINE DRAWING



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0 200	0 240	5.08	6.10	1
Φ B	0 140		3 56		
C	16 000	20 000	406 40	508 00	
Φ C	1 700	1 900	43.18	48.26	
Φ E		2 960		75.18	
F	1.000	1.070	25 40	27.18	
G					2
H	.005	067	013	1 70	
ΦJ	0 136	0 146	3.45	3 71	
K	070		1 78		
L		2.500		63.50	
M	030		0 76		

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