Signetics

8X411
Priority Interrupt Encoder

Objective Specification

Microprocessor Products

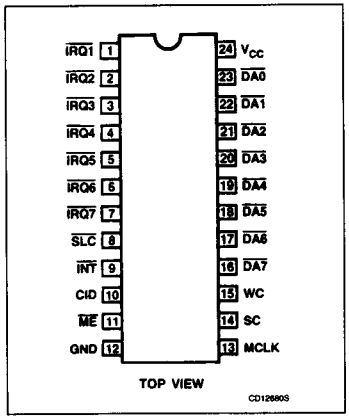
DESCRIPTION

The 8X411 Priority Interrupt Encoder provides a simple method to allow multiple interrupt sources to be connected to a single microprocessor interrupt input. Interfacing directly to the 8X401 microcontroller, the 8X411 generates an interrupt output in response to one of its own seven interrupt inputs, and provides the means by which the host processor determines which of the interrupts is pending. Two modes of operation allow interrupts to be processed either by predetermined priority or by a software controlled method. Two 8X411s can be cascaded together to expand the total number of interrupts to fourteen. The cascading is implemented in such a way that no additional time is expended to respond to the interrupts on the second 8X411.

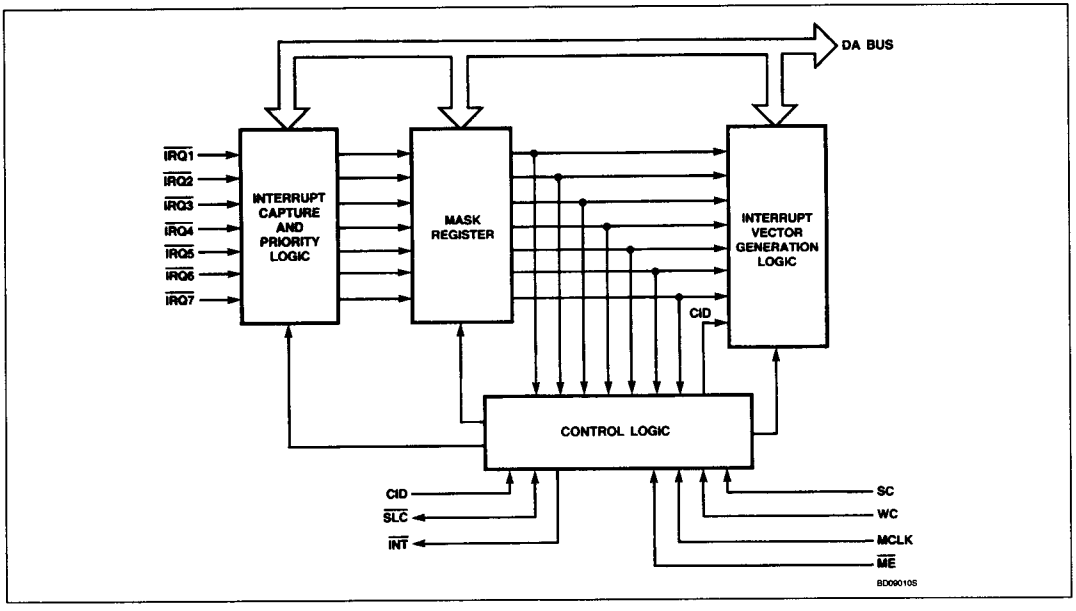
FEATURES

- **One chip controls up to seven prioritized interrupt inputs.**
- **Can be cascaded for up to 14 prioritized interrupts.**
- **Uses a single interrupt vector address when cascaded.**
- **A mask register individually masks each interrupt.**
- **Prioritized and nonprioritized interrupt vector modes.**
- **Direct bus compatibility with the 8X401 microcontroller.**
- **24-pin slim line package.**
- **Single +5V supply.**

PIN CONFIGURATION



BLOCK DIAGRAM



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ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin DIL plastic	N8X411N

PIN DESCRIPTION

PIN NO.	IDENTIFIER	FUNCTION
1 – 7	$\overline{IRQ1}$ – $\overline{IRQ7}$	**Interrupt Request:** User interrupt request lines. Active low.
8	$\overline{SLC}$	**Slave Control:** This pin is provides the handshaking between two cascaded 8X411s.
9	$\overline{INT}$	**Interrupt Output:** This active low, open collector output is the Interrupt output to the host processor.
10	CID	**Chip ID:** Input on this pin determines the 8X411 operation as either a Master or a Slave.
11	$\overline{ME}$	**Master Enable:** Controls operations on the DA bus, in conjunction with SC, WC, and MCLK.
12	GND	**Ground.**
13	MCLK	**Master Clock:** The system clock from the host microprocessor.
14	SC	**Select Command:** When high, indicates that an address is being output on the DA bus.
15	WC	**Write Command:** When high, indicates that data is being output on the DA bus.
16 – 23	$\overline{DA7}$ – $\overline{DA0}$	**DA Bus:** Bidirectional, 3-State, data and address bus.
24	V_{CC}	+5V power supply.