TRIQUINT SEMICONDUCTOR, INC.

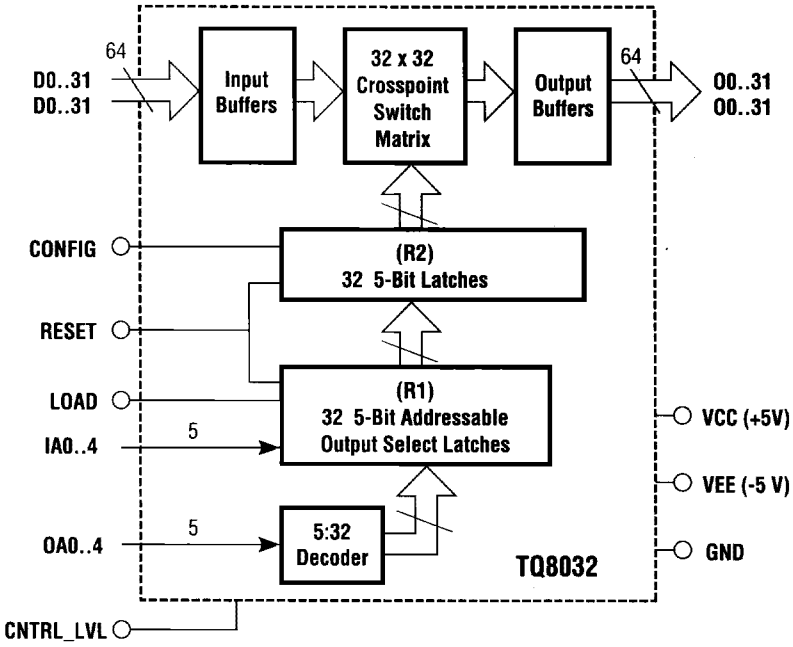
TQS

DIGITAL COMMUNICATIONS
AND SIGNAL PROCESSING

PRELIMINARY

TQ8032

32 x 32 Digital Crosspoint Switch



The TQ8032 is a 32 x 32 differential digital crosspoint switch capable of handling 800 Mbit/s data rate (min.). The high data rate and exceptional signal fidelity is made possible with TriQuint's fully differential Source-Coupled FET Logic (SCFL) standard cells. The symmetrical switching characteristic inherent in differential logic results in low signal skew and crosstalk for maximum signal fidelity.

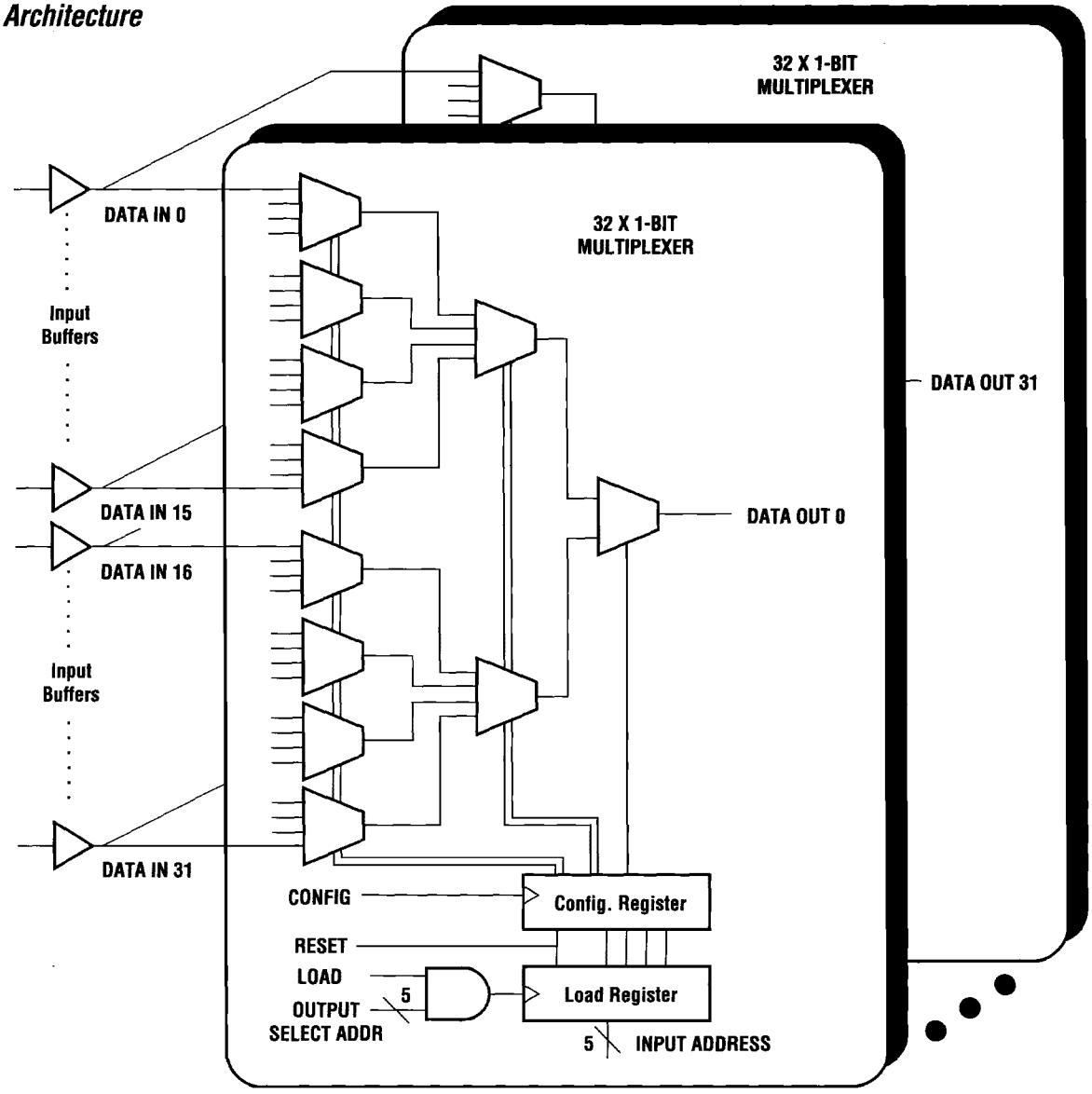
The user can independently configure any switch output to any input, including an input chosen by another output. To configure the switch, the 5-bit output address (OA0..4) is decoded to enable the loading of the 5-bit input selection data (IA0..4) on the falling edge of the LOAD signal. The process is repeated until all desired connections are programmed. By bringing the CONFIG signal HIGH, the contents of the Output Select Latches are transferred in parallel to a second row of 5-bit latches (R2), causing the switch reconfiguration. This double row architecture minimizes the time to completely reconfigure the switch, since a new set of addresses can be loaded to the Output Select Latches (R1) while the switch is active (transmitting). At the time of reconfiguration, no data drop-out occurs for any output whose input connection does not change. For applications which do not require synchronous configuration of the switch, the LOAD and CONFIG inputs may be tied together.

Features

- *800 Mbits/s data rate (min.)*
- *Non-blocking architecture*
- *±280 ps delay match (one input to all outputs)*
- *ECL-level data inputs/outputs; selectable CMOS/TTL-level control inputs*
- *Low crosstalk*
- *Fully differential data path*
- *Double row of output select latches minimizes reconfiguration time*
- *Available in 196-pin leaded chip carrier*

TQNTS015

TQ8032 Architecture



Pin Descriptions

Pin Name	Levels	Description
D0-D31	ECL	Differential Data Inputs
$\overline{D0-D31}$	ECL	Differential Data Inputs
O0-O31	ECL	Differential Data Outputs
$\overline{O0-O31}$	ECL	Differential Data Outputs
IA0-IA4	CMOS/TTL	Input Address
OA0-OA4	CMOS/TTL	Output Address
CNTRL_LVL	GND/OPEN	Control Input Level Select

Pin Name	Levels	Description
CONFIG	CMOS/TTL	Switch Reconfiguration
RESET	CMOS/TTL	Pass-Through or Broadcast Mode
LOAD	CMOS/TTL	Loads Input Address
GND	0 V.	Ground Reference
VEE	-5 V.	Power Supply
VCC	+5 V.	Power Supply

Absolute Maximum Ratings[4]

Symbol	Parameter	Absolute Max. Rating	Notes
T_{STOR}	Storage Temperature	-65° C to +150° C	
T_J	Junction Temperature	-55° C to +150° C	
T_C	Case Temperature Under Bias	-55° C to +125° C	1
V_{CC}	Supply Voltage	0 V to +7 V	2
V_{EE}	Supply Voltage	-7 V to 0 V	2
V_{TT}	Load Termination Supply Voltage	V_{EE} to 0 V	3
V_{IN}	Voltage Applied to Any ECL Input; Continuous	V_{EE} -0.5 V to +0.5 V	
I_{IN}	Current Into Any ECL Input; Continuous	-1.0 mA to +1.0 mA	
V_{IN}	Voltage Applied to Any TTL/CMOS Input; Continuous	-0.5 V to V_{CC} +0.5 V	
I_{IN}	Current Into Any TTL/CMOS Input; Continuous	-1.0 mA to +1.0 mA	
V_{OUT}	Voltage Applied to Any ECL Output	V_{EE} -0.5 V to +0.5 V	3
I_{OUT}	Current From Any ECL Output; Continuous	-40 mA	
P_D	Power Dissipation per Output $P_{OUT} = (GND - V_{OUT}) \times I_{OUT}$	50 mW	

Notes: 1. T_C is measured at case top.
2. All voltages specified with respect to GND, defined as 0V.
3. Subject to I_{OUT} and power dissipation limitations.
4. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified in the Recommended Operating Conditions table, below.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_C	Case Operating Temperature	0	25	85	°C	1
GND	Ground Reference Voltage		0		V	
V_{CC}	Supply Voltage	4.5		5.5	V	
V_{EE}	Supply Voltage	-5.5		-4.5	V	
V_{TT}	Load Termination Supply Voltage		-2.0		V	2
R_{LOAD}	Output Termination Load Resistance		50		Ω	2

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.

DC Characteristics[1] $T_C = 0°C$ to $85°C$, $V_{CC} = 4.5$ V to 5.5 V, $V_{EE} = -5.5$ V to -4.5 V, GND = 0 V, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Test Cond.	Notes
V_{IH}	ECL Input Voltage High	-1100		-500	mV		
V_{IL}	ECL Input Voltage Low	V_{TT}		-1500	mV		
I_{IH}	ECL Input Current High			+30	µA	$V_{IH} = 0.7$ V	
I_{IL}	ECL Input Current Low			-30	µA	$V_{IL} = -2.0$ V	
V_{ICM}	ECL Input Common Mode Voltage	-1500		-1100	mV		
V_{IDIF}	ECL Input Differential Voltage (P-P)	400		1200	mV		
V_{IH}	CMOS/TTL Input Voltage High	3.5/2.0		V_{CC}/V_{CC}	V		3
V_{IL}	CMOS/TTL Input Voltage Low	0/0		1.5/0.8	V		3
I_{IH}	CMOS/TTL Input Current High			+100	µA	$V_{IH} = V_{CC}$	3
I_{IL}	CMOS/TTL Input Current Low	-100			µA	$V_{IL} = 0$ V	3
V_{OCM}	ECL Output Common Mode	-1500		-1100	mV		
V_{ODIF}	ECL Output Differential Voltage	600			mV		
V_{OH}	ECL Output Voltage High	-1000		-600	mV		
V_{OL}	ECL Output Voltage Low	V_{TT}		-1600	mV		
I_{OH}	ECL Output Current High	20	23	27	mA		
I_{OL}	ECL Output Current Low	0	5	8	mA		
I_{CC}[2]	Power Supply Current		15	20	mA		
I_{EE}[2]	Power Supply Current		-1500	-1950	mA		

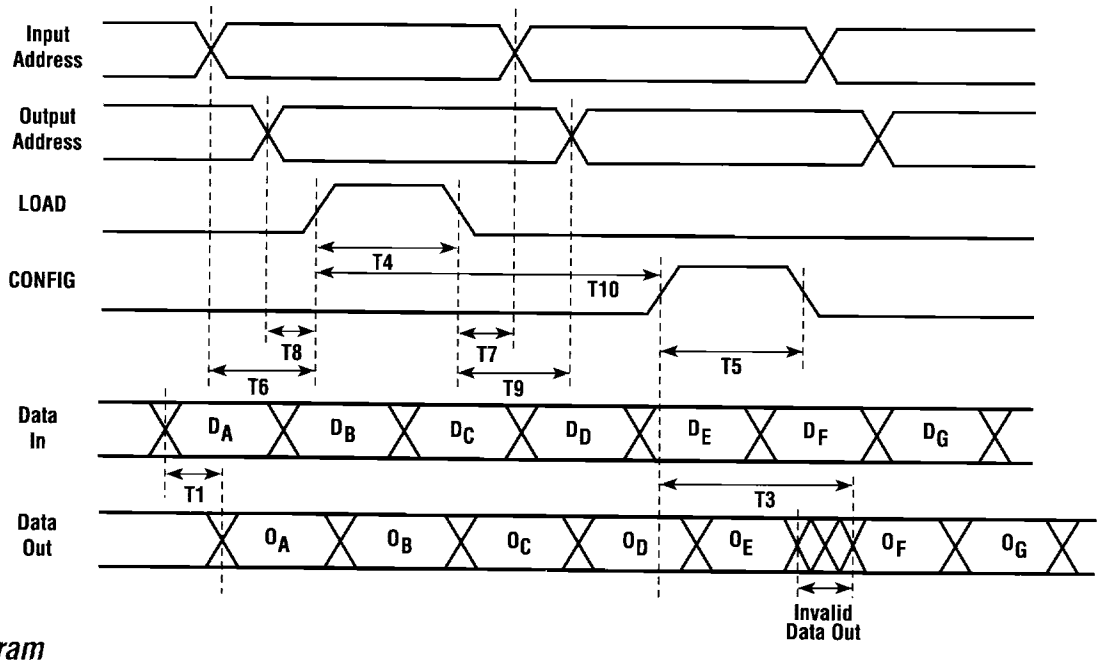
Notes: 1. Test conditions unless otherwise indicated: $V_{TT} = -2.0$ V, $R_{LOAD} = 50\,\Omega$ to V_{TT}.
2. Positive current is defined as flowing into the device and negative current as flowing out of the device. I_{CC} typically flows into the device and I_{EE} flows out of the device.
3. Input level is selected by the CNTRL_LVL input. Tieing CNTRL_LVL to GND selects TTL levels, leaving CNTRL_LVL OPEN selects CMOS levels.

AC Characteristics[1]

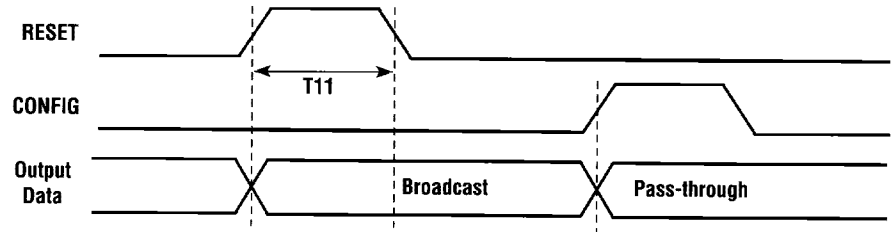
Symbol	Parameter	Min	Typ	Max	Units	Notes
F_C[1]	Maximum Input Frequency	800			Mbit/s	
T_1	Data In (Di) to Data Out (Oi) Delay		1500		ps	
T_2	Propagation Delay Match (one input to all outputs)		±280		ps	
T_3	CONFIG to Data Out (Oi) Delay			5	ns	
T_4	LOAD Pulse Width	10			ns	
T_5	CONFIG Pulse Width	10			ns	
T_6	IAi to LOAD High Setup Time	0			ns	
T_7	LOAD to IAi Low Hold Time	7			ns	
T_8	OAi to LOAD High Setup Time	7			ns	
T_9	LOAD to OAi Low Hold Time	7			ns	
T_{10}	Load ↑ to CONFIG ↑	0			ns	
T_{11}	RESET Pulse Width	10			ns	
$T_{R,F}$	Output Rise or Fall Time		300	400	ps	2

Notes: 1. Test conditions: $V_{TT} = -2.0$ V, $R_{LOAD} = 50\,\Omega$ to V_{TT}; ECL inputs: $V_{IH} = -1.1$ V; $V_{IL} = -1.5$ V; CMOS inputs: $V_{IH} = 3.5$ V, $V_{IL} = 1.5$ V; ECL Outputs: $V_{OH} \geq -1.0$ V, $V_{OL} \leq -1.6$ V; ECL inputs rise and fall times ≤ 1 ns; CMOS inputs rise and fall times ≤ 20 ns
2. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

Timing Diagram

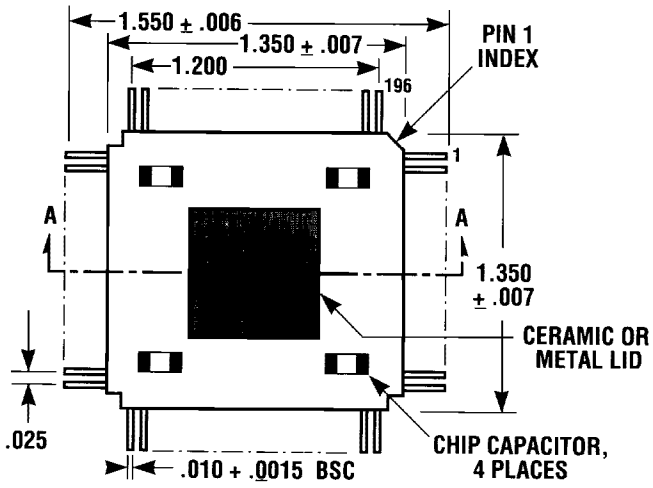


Timing Diagram

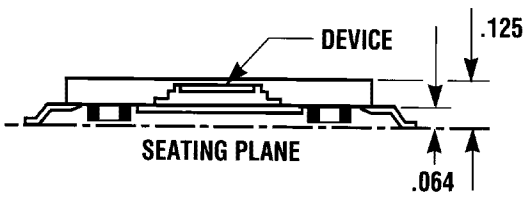


Notes: 1. LOAD input must remain LOW to insure correct programming of the switch.
2. "Broadcast" is defined as data input 0 to all data outputs (0..31).
3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, etc.

196-Pin Ceramic Package – Bottom View



Section A-A



TQ8032 Pinout

Pin #	*SMA #*	*Signal Name*
2	1	
3	2	NI7
4	3	I7
6	4	NI6
7	5	I6
8	6	NI5
9	7	I5
11	8	NI4
12	9	I4
13	10	NI3
14	11	I3
16	12	NI2
17	13	I2
18	14	NI1
19	15	I1
21	16	NI0
22	17	I0
23	18	
24	19	RESET
26	20	
27	21	
28	22	O0
29	23	NO0
31	24	O1
32	25	NO1
33	26	O2
34	27	NO2
36	28	O3
37	29	NO3
38	30	O4
39	31	NO4
41	32	O5
42	33	NO5
43	34	O6
44	35	NO6
46	36	O7
47	37	NO7
48	38	CNTRL_LVL
51	39	

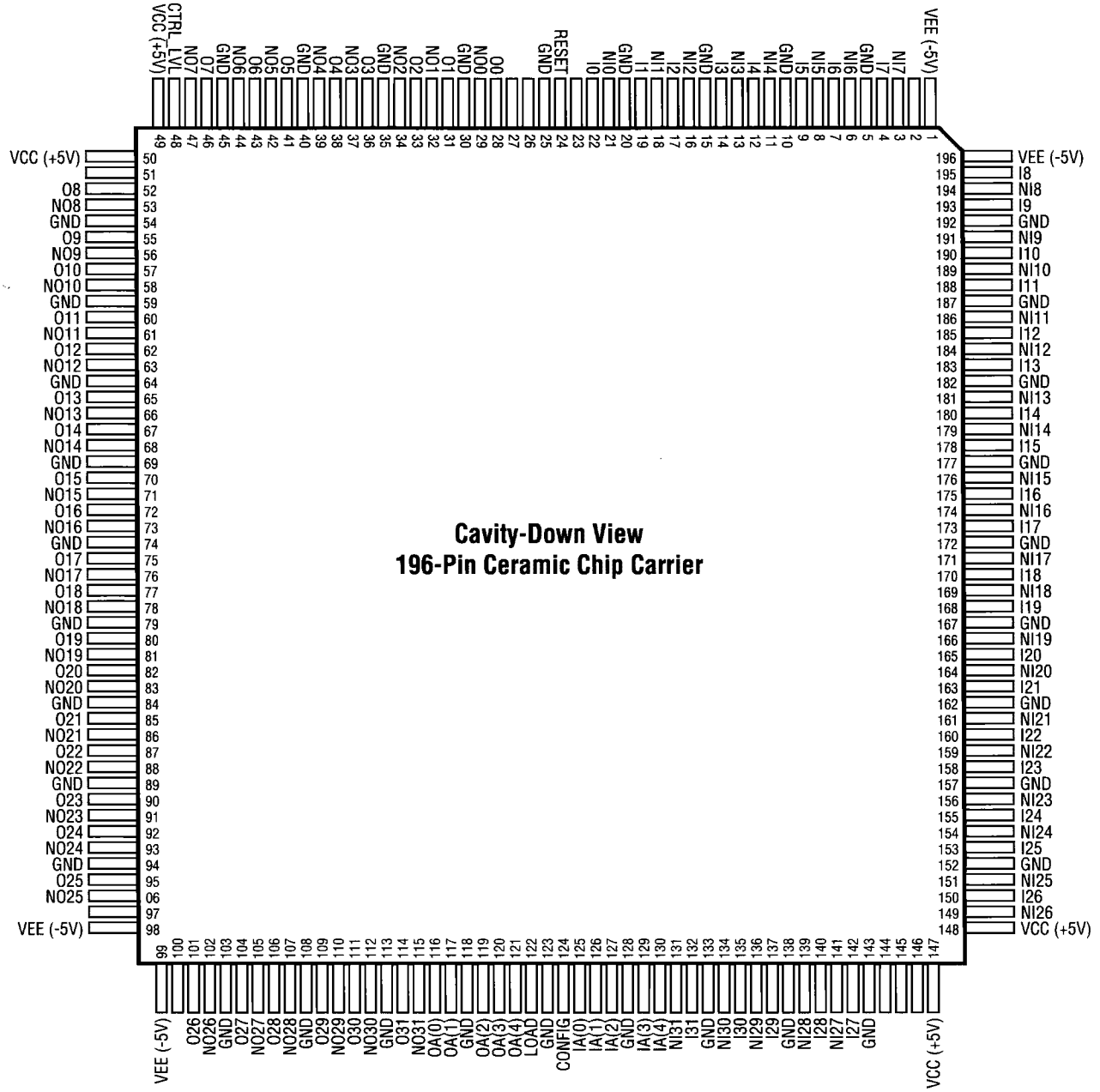
Pin #	*SMA #*	*Signal Name*
53	41	NO8
55	42	O9
56	43	NO9
57	44	O10
58	45	NO10
60	46	O11
61	47	NO11
62	48	O12
63	49	NO12
65	50	O13
66	51	NO13
67	52	O14
68	53	NO14
70	54	O15
71	55	NO15
72	56	O16
73	57	NO16
75	58	O17
76	59	NO17
77	60	O18
78	61	NO18
80	62	O19
81	63	NO19
82	64	O20
83	65	NO20
85	66	O21
86	67	NO21
87	68	O22
88	69	NO22
90	70	O23
91	71	NO23
92	72	O24
93	73	NO24
95	74	O25
96	75	NO25
97	76	
100	77	
101	78	O26
102	79	NO26
104	80	O27

TQ8032 Pinout (cont.)

Pin #	SMA #	Signal Name
105	81	NO27
106	82	O28
107	83	NO28
109	84	O29
110	85	NO29
111	86	O30
112	87	NO30
114	88	O31
115	89	NO31
116	90	OA(0)
117	91	OA(1)
119	92	OA(2)
120	93	OA(3)
121	94	OA(4)
122	95	LOAD
124	96	CONFIG
125	97	IA(0)
126	98	IA(1)
127	99	IA(2)
129	100	IA(3)
130	101	IA(4)
131	102	NI31
132	103	I31
134	104	NI30
135	105	I30
136	106	NI29
137	107	I29
139	108	NI28
140	109	I28
141	110	NI27
142	111	I27
144	112	
145	113	
146	114	
149	115	NI26
150	116	I26
151	117	NI25
153	118	I25
154	119	NI24
155	120	I24
156	121	NI23
158	122	I23
159	123	NI22
160	124	I22
161	125	NI21
163	126	I21
164	127	NI20
165	128	I20
166	129	NI19
168	130	I19
169	131	NI18
170	132	I18
171	133	NI17
173	134	I17
174	135	NI16
175	136	I16
176	137	NI15
178	138	I15
179	139	NI14
180	140	I14
181	141	NI13
183	142	I13
184	143	NI12
185	144	I12
186	145	NI11
188	146	I11
189	147	NI10
190	148	I10
191	149	NI9
193	150	I9
194	151	NI8
195	152	I8
1, 98, 99, 196		VEE (-5 V)
49, 50, 147, 148		VCC (+5 V)
5, 10, 15, 20, 25, 30, 35, 40, 45, 54, 59, 64, 69, 74, 79, 84, 89, 94, 103, 108, 113, 118, 123, 128, 133, 138, 143, 152, 157, 162, 167, 172, 177, 182, 187, 192		GND

Note: All grounds are common.

TQ8032 Pinout



Ordering Information

TQ8032 – ____ M = 196-Pin Ceramic Package
D = Die

For more information contact nearest Sales Office or TriQuint's Customer Service Department:

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TriQuint SEMICONDUCTOR

Reorder Number TQ8032.A *Revision A.8, October 4, 1993*