SRAM MODULE

128K x 32 SRAM
LOW VOLTAGE

FEATURES
- High speed: 15, 20 and 25ns
- High-density 512KB design
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- Low profile
- Upgradable to a 256K x 32 module

OPTIONS — MARKING
- Timing
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- 2V data retention (optional) — L
- Part Number Example: MT4LS12832RM-15 L

PIN ASSIGNMENT (Front View)

64-Pin SIMM

64-Pin ZIP

PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

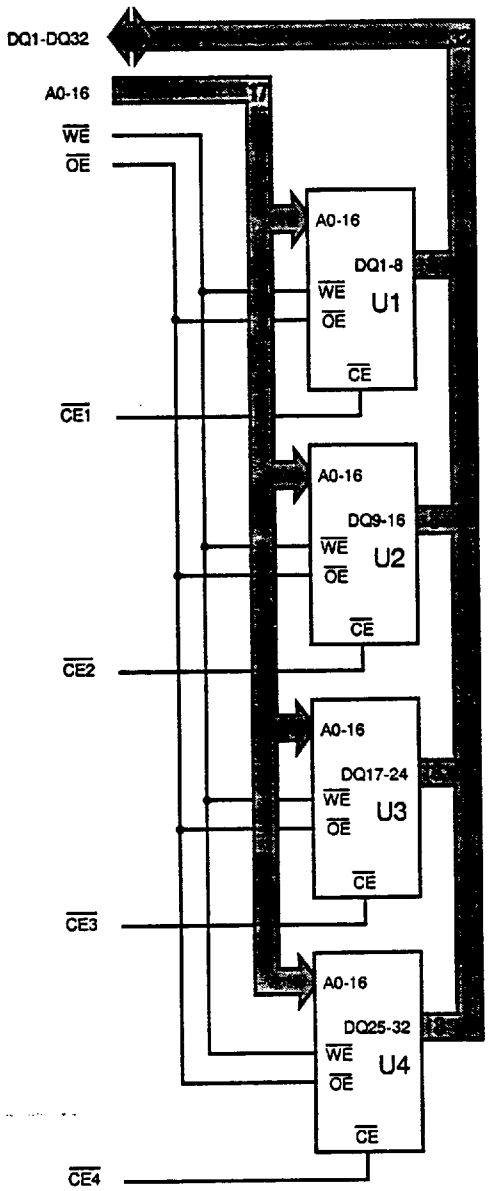
The MT4LS12832R is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four revolutionary pinout, low voltage 128K x 8 fast SRAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion. The "L" version provides a significant reduction in CMOS standby current (I_{SB2}) over the standard version.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's four bytes independently.

The Micron SRAM family uses a high-speed, low- power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible. This 3.3V module is ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive this module without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5LC128K8D4DJ

PRESENCE-DETECT
PD0 = No Connect
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage temperature ..... -55°C to +125°C
Power dissipation 4W
Short circuit output current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	A0-A16, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-4	4	µA	
		$\overline{CE1}$-$\overline{CE4}$	I_{LI2}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	DQ1-DQ32	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			Vcc	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	VER	TYP	MAX -15	MAX -20	MAX -25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	Icc	ALL	660	920	720	640	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	ALL	140	200	160	140	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	ALL	2	20	20	20	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A16, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_{I1}	25	pF	4
Input Capacitance: $\overline{CE1}$-$\overline{CE4}$		C_{I2}	6	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	15		20		25		ns	
Address access time	^tAA		15		20		25	ns	
Chip Enable access time	^tACE		15		20		25	ns	
Output hold from address change	^tOH	4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25	ns	
Output Enable access time	^tAOE		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		8		8	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	15		20		25		ns	
Chip Enable to end of write	^tCW	12		13		15		ns	
Address valid to end of write	^tAW	10		12		14		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	10		12		14		ns	
WRITE pulse width	$^tWP2$	10		12		14		ns	
Data setup time	^tDS	8		10		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

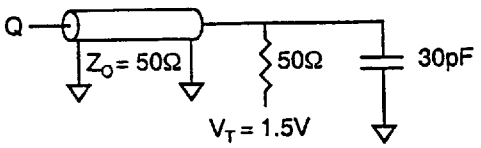


Fig. 1 OUTPUT LOAD EQUIVALENT

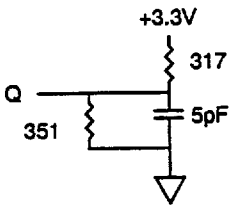


Fig. 2 OUTPUT LOAD EQUIVALENT

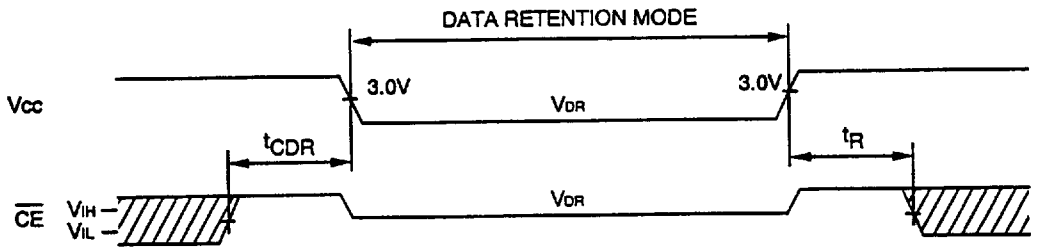
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \geq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200$ msec.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded and $f = \frac{1}{{}^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$=READ cycle time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.
15. The output will be in the High-Z state if output enable is high.

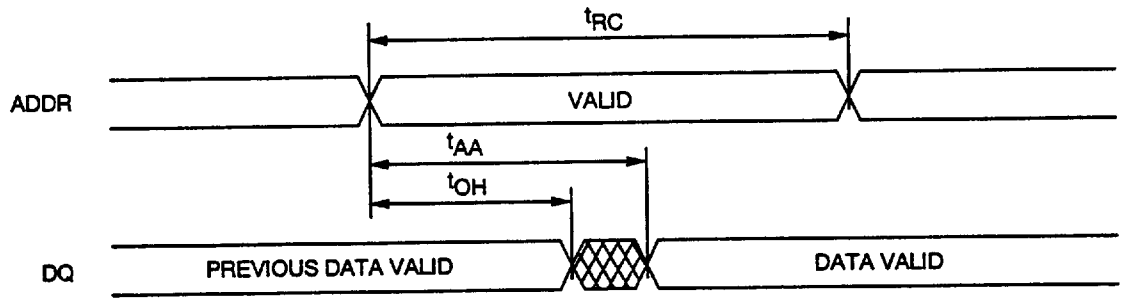
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq$ (Vcc -0.2V) $V_{IN} \geq$ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		280	1,200	µA	14
Chip Deselect to Data Retention Time			${}^tCDR$	0			ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

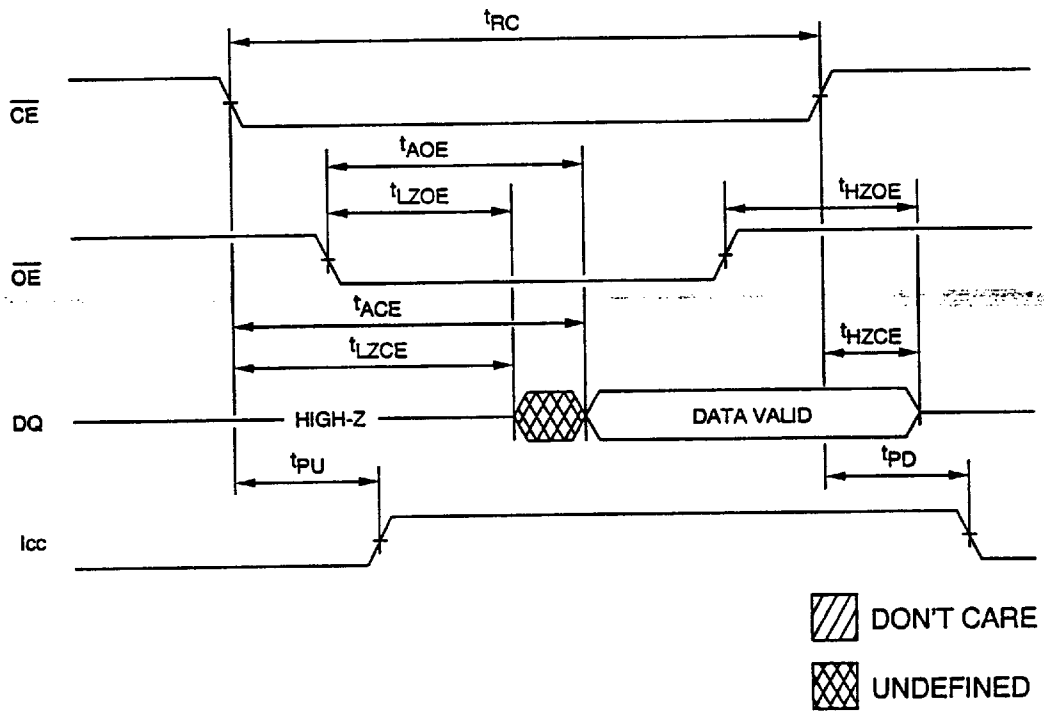
LOW Vcc DATA RETENTION WAVEFORM



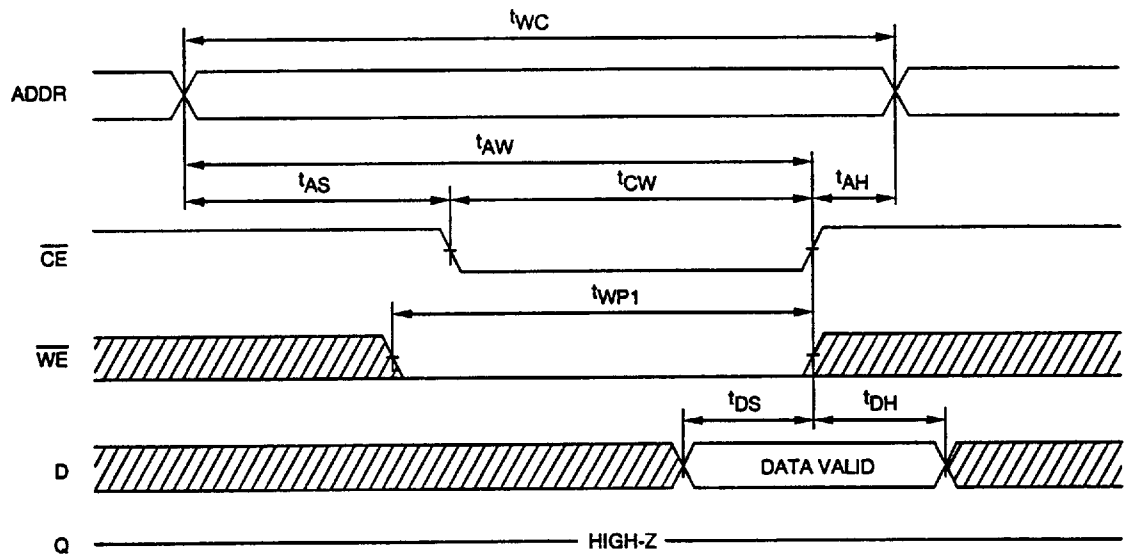
READ CYCLE NO. 1 [8, 9]



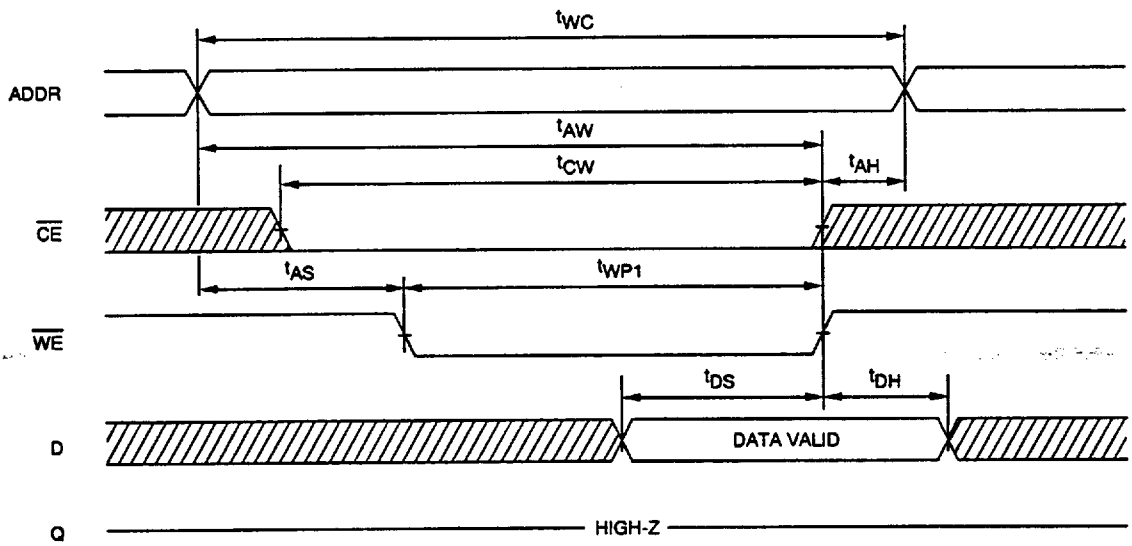
READ CYCLE NO. 2 [7, 8, 10]

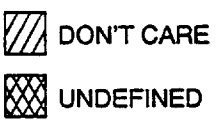


WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



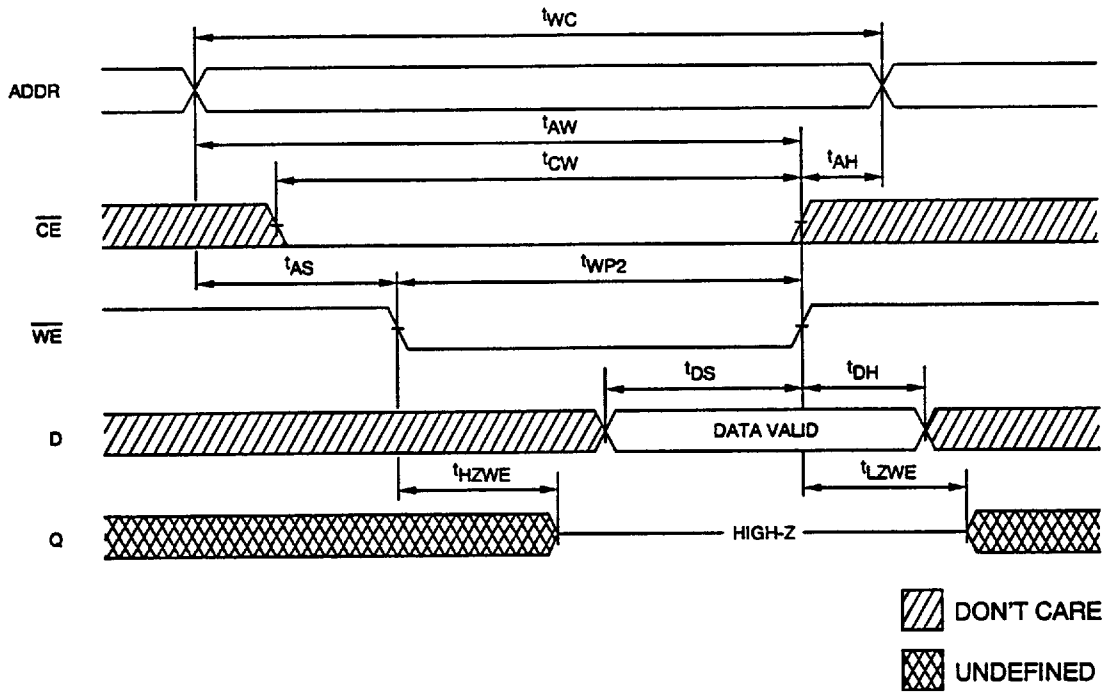
WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)





NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 15]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).